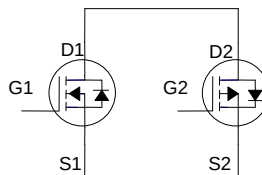


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	40V	-40V
$R_{DS(on)} (MAX.)$	35m Ω	44m Ω
I_D	12A	-9A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V _{GS}	N-CH	P-CH	V
			±20	±20	
Continuous Drain Current	T _C = 25 °C	I _D	12	-9	A
	T _C = 100 °C		8	-6	
Pulsed Drain Current ¹		I _{DM}	48	-36	
Power Dissipation	T _C = 25 °C	P _D	21		W
	T _C = 100 °C		8.3		
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		42	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$ $V_{GS} = 0V, I_D = -250\mu A$	N-CH	40		V	
			P-CH	-40			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$ $V_{DS} = V_{GS}, I_D = -250\mu A$	N-CH	1.8	2.3	3.2	
			P-CH	-1.8	-2.3	-3.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$ $V_{DS} = 0V, V_{GS} = \pm 20V$	N-CH			± 100	nA
			P-CH			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32V, V_{GS} = 0V$ $V_{DS} = -32V, V_{GS} = 0V$	N-CH			1	μA
			P-CH			-1	
		$V_{DS} = 30V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$ $V_{DS} = -30V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$	N-CH			25	
			P-CH			-25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$ $V_{DS} = -5V, V_{GS} = -10V$	N-CH	12			A
			P-CH	-9			
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 10A$ $V_{GS} = -10V, I_D = -8A$	N-CH		30	35	mΩ
			P-CH		38	44	
		$V_{GS} = 7V, I_D = 8A$ $V_{GS} = -7V, I_D = -6A$	N-CH		40	50	
			P-CH		50	70	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 10A$ $V_{DS} = -5V, I_D = -8A$	N-CH		19		S
			P-CH		11		
DYNAMIC							
Input Capacitance	C_{iss}	N-CH $V_{GS} = 0V, V_{DS} = 20V, f = 1MHz$ P-CH $V_{GS} = 0V, V_{DS} = -20V, f = 1MHz$	N-CH		515		pF
Output Capacitance	C_{oss}		P-CH		745		
			N-CH		77		
Reverse Transfer Capacitance	C_{rss}		P-CH		78		
			N-CH		53		
			P-CH		58		

Total Gate Charge ^{1,2}	Q _g	N-CH V _{DS} = 20V, V _{GS} = 10V, I _D = 15A P-CH V _{DS} = -20V, V _{GS} = -10V, I _D = -10A	N-CH		13.1		nC
Gate-Source Charge ^{1,2}	Q _{gs}		P-CH		11.5		
Gate-Drain Charge ^{1,2}	Q _{gd}		N-CH		1.9		
			P-CH		2.5		
			N-CH		4.1		
			P-CH		2.8		
Turn-On Delay Time ^{1,2}	t _{d(on)}	N-CH V _{DS} = 10V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω P-CH V _{DS} = -10V, I _D = -1A, V _{GS} = -10V, R _{GS} = 6Ω	N-CH		2.5		nS
Rise Time ^{1,2}	t _r		P-CH		7		
			N-CH		7.5		
Turn-Off Delay Time ^{1,2}	t _{d(off)}		P-CH		10		
			N-CH		12		
Fall Time ^{1,2}	t _f		P-CH		20		
		N-CH		4			
		P-CH		12			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)							
Continuous Current	I _S		N-CH			12	A
			P-CH			-9	
Pulsed Current ³	I _{SM}		N-CH			48	
			P-CH			-36	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V	N-CH			1.3	V
			P-CH			-1.3	

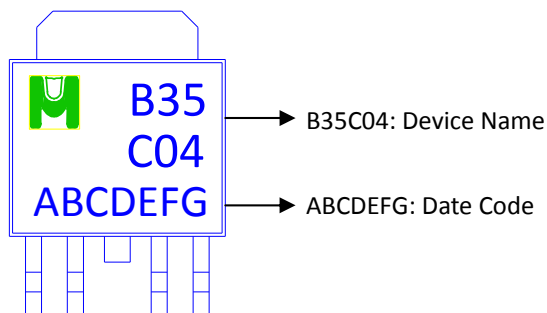
¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

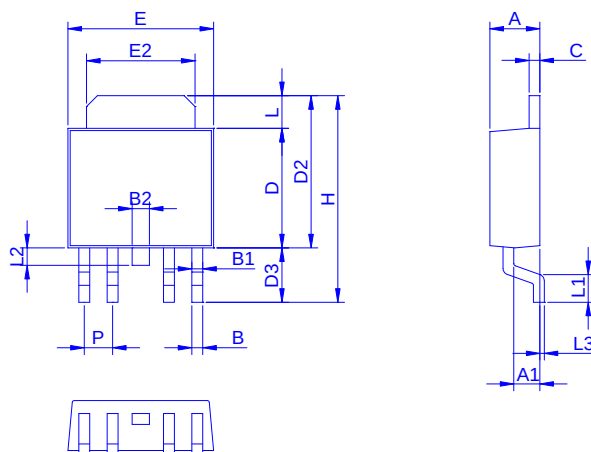
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB35C04A for DPAK (TO-252)

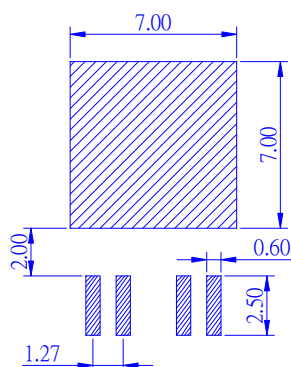


Outline Drawing



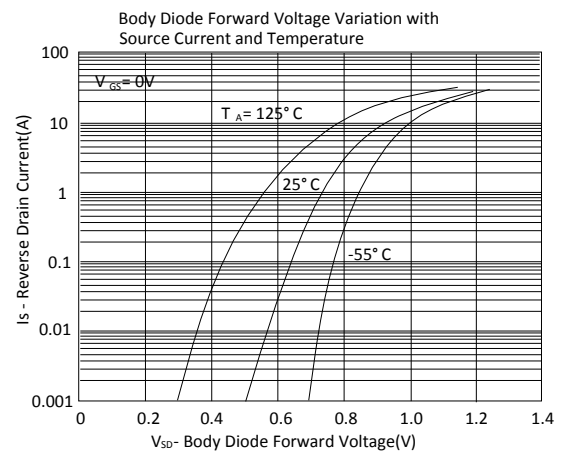
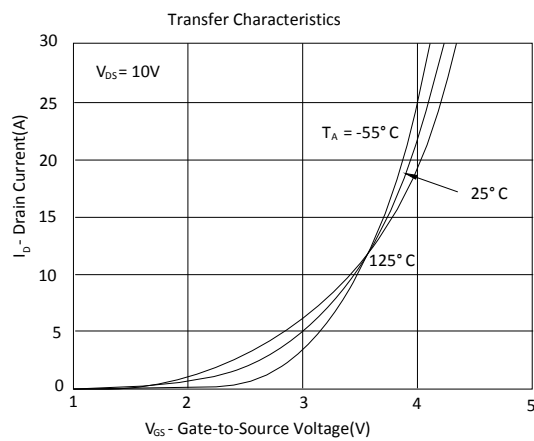
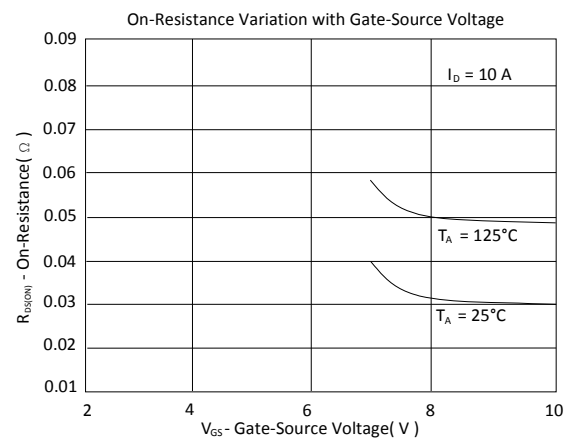
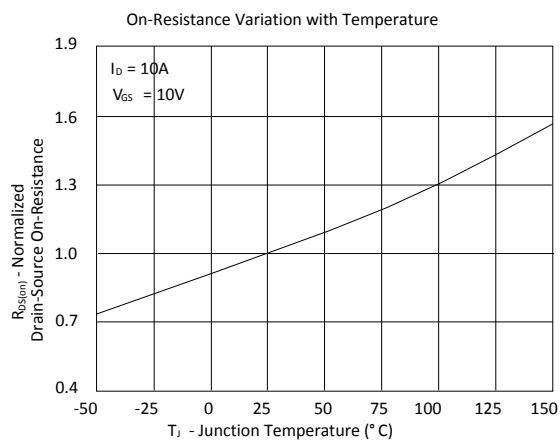
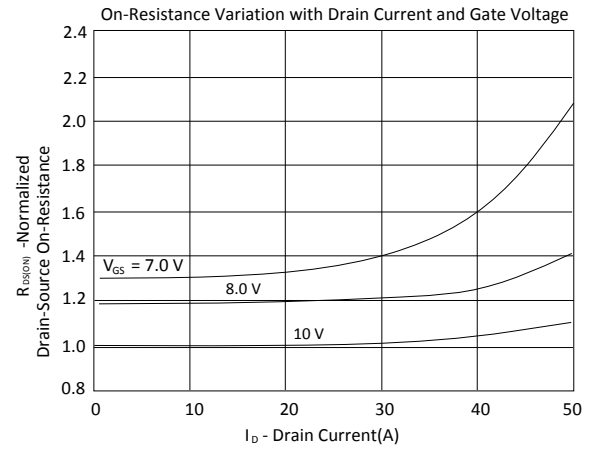
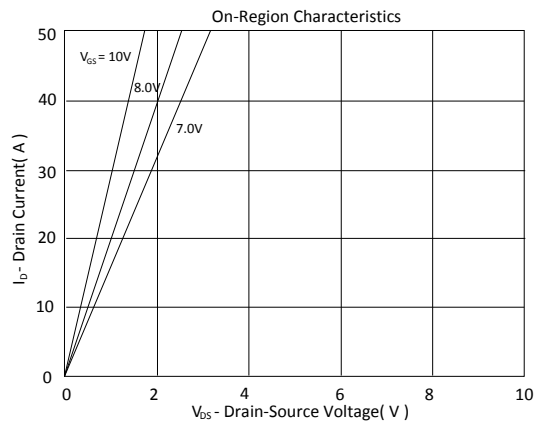
Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	1.10	0.30	0.55	0.40	0.40	5.30	6.70	2.20	6.30	4.80	9.20	1.30	0.90	0.50	0.00	1.17
Max.	2.50	1.30	0.70	0.75	0.80	0.60	5.70	7.30	3.00	6.70	5.45	10.15	1.70	1.50	1.10	0.30	1.37

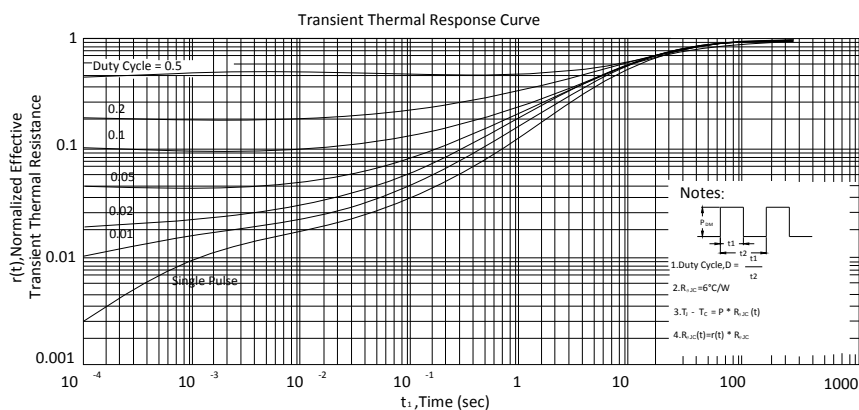
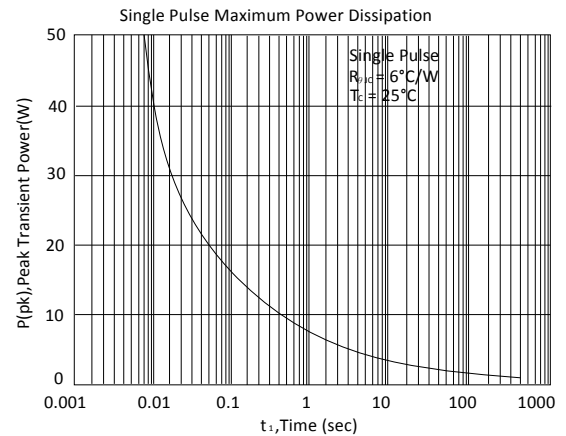
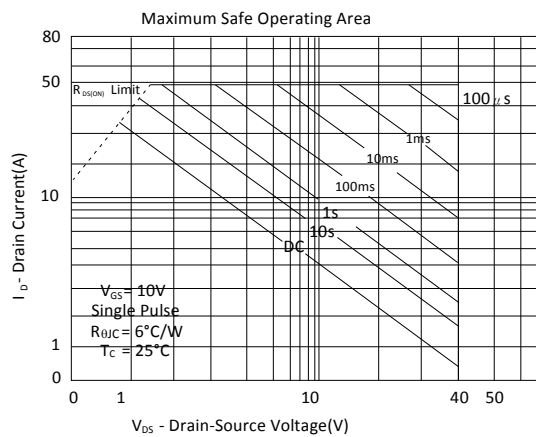
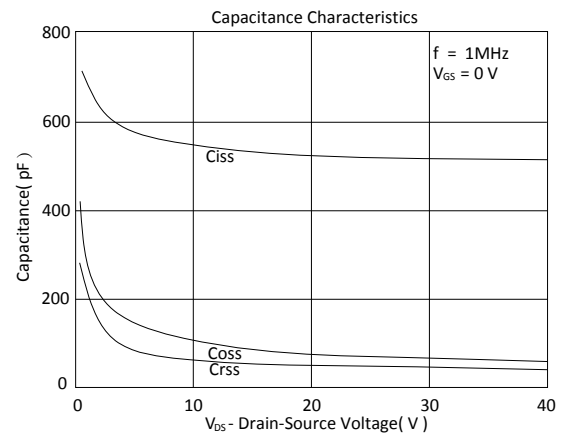
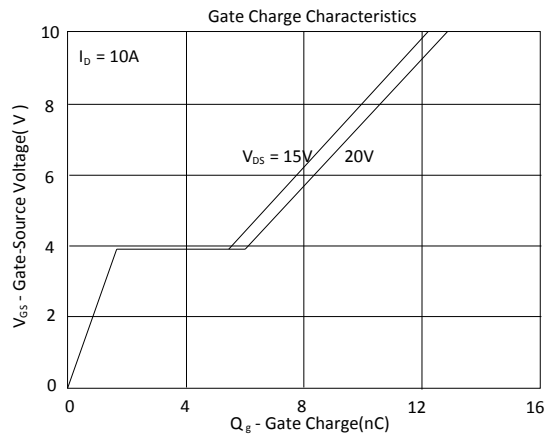
Footprint





N-Channel







P-Channel

