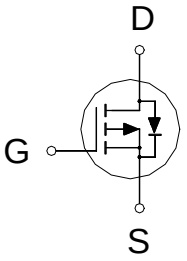
杰力科技股份有限公司
Excelliance MOS Corporation

EMB50P03VAT

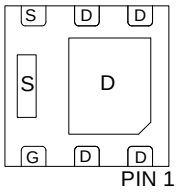
P-Channel Logic Level Enhancement Mode Field Effect Transistor

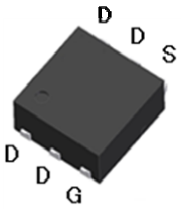
Product Summary:

BV_{DSS}	-30V
$R_{DSON\ (MAX.)}$	50mΩ
I_D	-4.5A



Bottom View





Pb-Free Lead Plating & Halogen Free

GP
GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	-4.5	A
	T_A = 70 °C		-3.5	
Pulsed Drain Current[1]		I_{DM}	-18	
Power Dissipation	T_A = 25 °C	P_D	2.08	W
	T_A = 70 °C		1.33	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		12	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		60	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]60°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-4.5			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -4.5A		42	50	mΩ
		V_{GS} = -4.5V, I_D = -3.5A		66	85	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -4.5A		16		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		820		pF
Output Capacitance	C_{oss}			122		
Reverse Transfer Capacitance	C_{rss}			97		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		5.0		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = -10V, V_{GS} = -10V, I_D = -4.5A		9		nC
Gate-Source Charge[1,2]	Q_{gs}			2.2		
Gate-Drain Charge[1,2]	Q_{gd}			2.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -10V, I_D = -1A, V_{GS} = -10V, R_{GS} = 6Ω		12		nS
Rise Time[1,2]	t_r			16		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			34		
Fall Time[1,2]	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-4.5	A
Pulsed Current[3]	I_{SM}				-18	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V

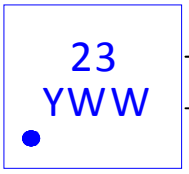
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

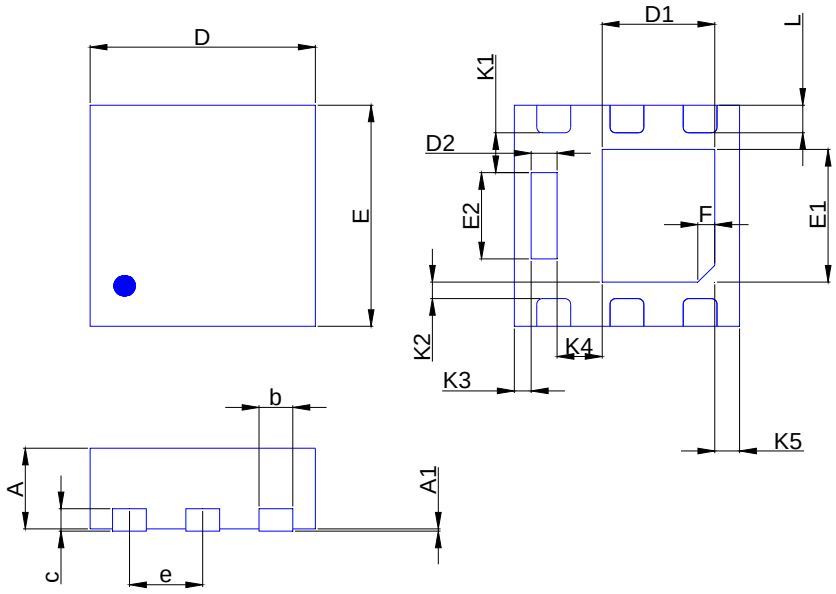
Device Name: EMB50P03VAT for EDFN 2 x 2



→ 23: Device Name, 23 for EMB50P03VAT

→ YWW: Date Code

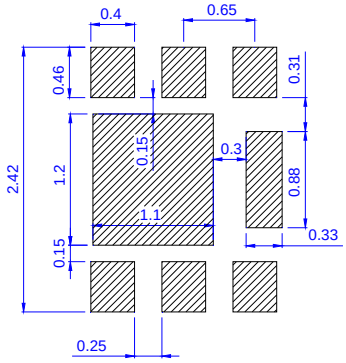
Outline Drawing



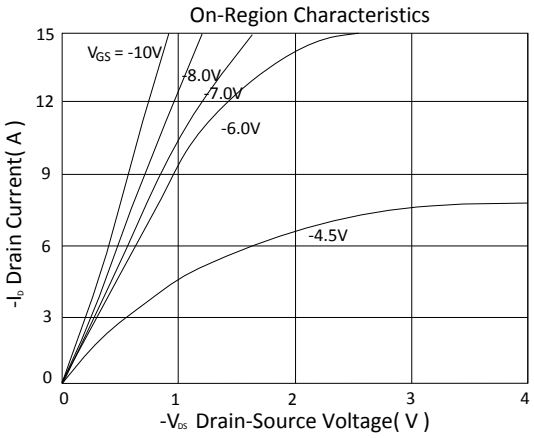
Dimension in mm

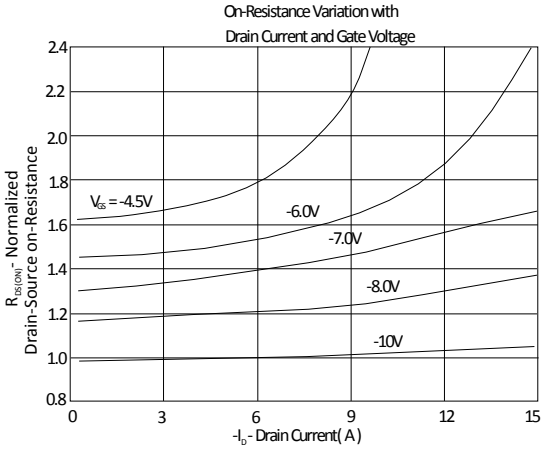
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.50	0.00	0.25		1.9	1.0	0.13	1.9	1.1	0.65				0.306	0.10	0.2	0.10	0.27	0.17
Typ.		0.02	0.30	0.1	2.0	1.1	0.25	2.0	1.2	0.75	0.65	0.15	45°	0.356	0.15	0.25	0.15		0.22
Max.	0.65	0.05	0.35		2.1	1.2	0.35	2.1	1.3	0.88				0.406	0.20	0.3	0.20		0.27

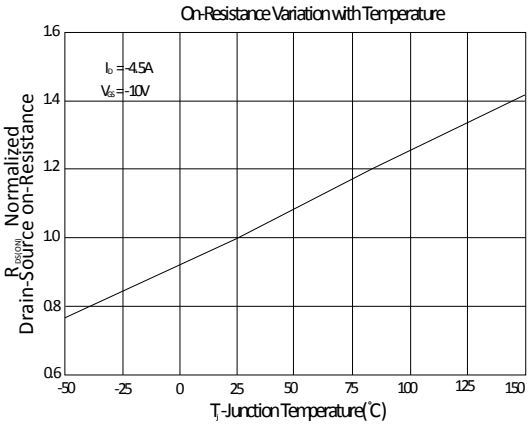
Recommended minimum pads

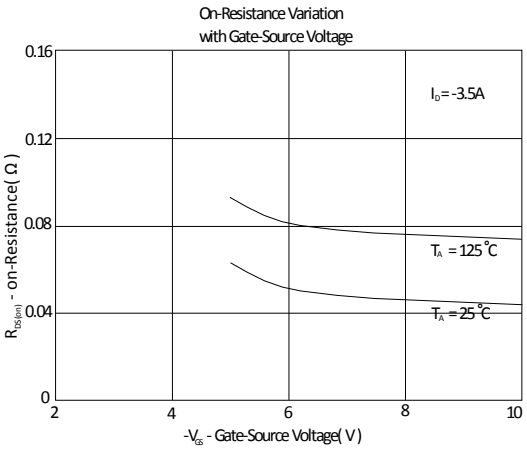


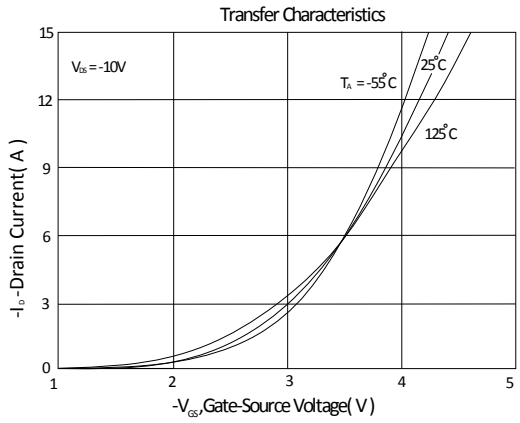
TYPICAL CHARACTERISTICS

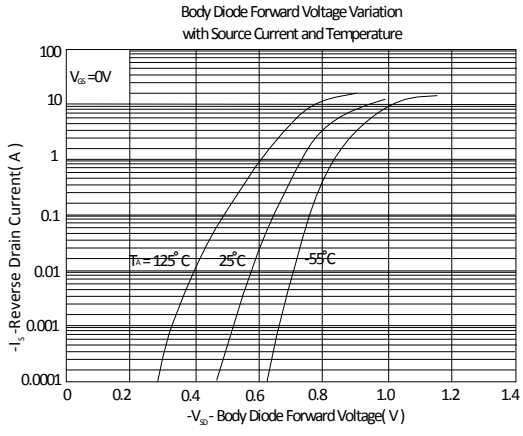




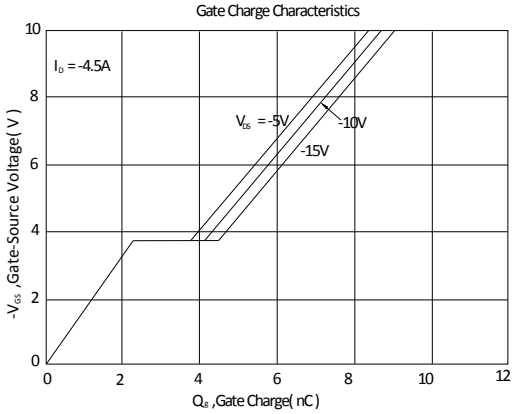




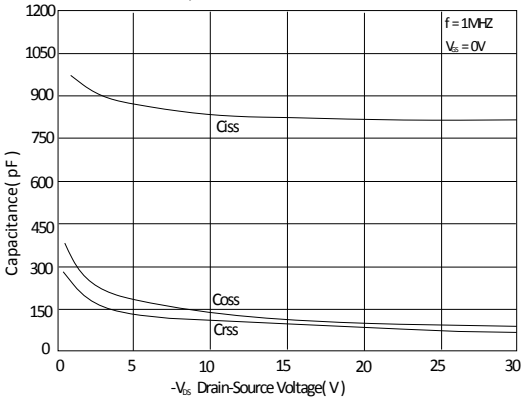




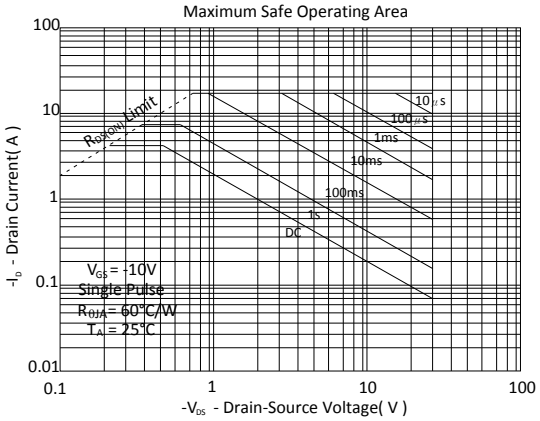
Gate Charge Characteristics



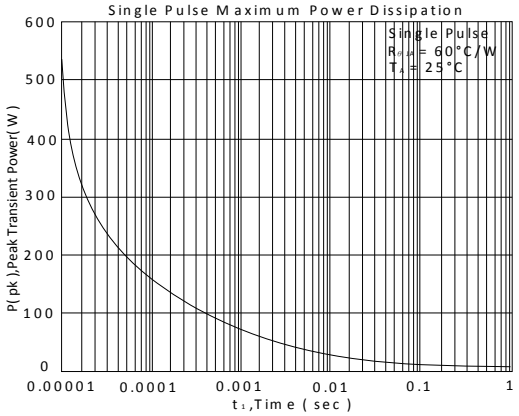
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve