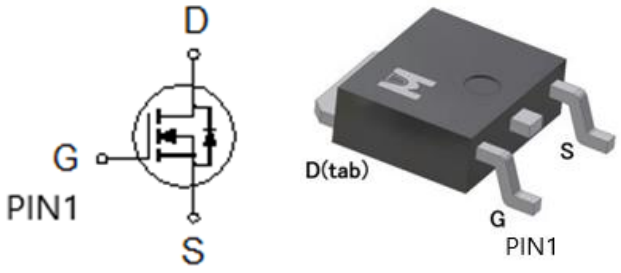
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH
BV_{DSS}	100V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	100mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	150mΩ
I_D @T_C=25°C	17A



N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	17	A
	T_C = 100 °C		11	
Pulsed Drain Current[1]		I_{DM}	68	
Avalanche Current	L = 0.01mH	I_{AS}	2.5	
Avalanche Energy	L = 1.0mH	E_{AS}	3.0	mJ
Repetitive Avalanche Energy[2]	L = 0.5mH	E_{AR}	1.5	
Power Dissipation	T_C = 25 °C	P_D	50	W
	T_C = 100 °C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		75	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]75°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.8	3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V			1	μA
		V_{DS} = 70V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	17			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 8A		80	100	mΩ
		V_{GS} = 4.5V, I_D = 5A		105	150	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 8A		8		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		213.8		pF
Output Capacitance	C_{oss}			71.5		
Reverse Transfer Capacitance	C_{rss}			11.7		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		1.0		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 80V, V_{GS} = 10V, I_D = 8A		6.4		nC
Gate-Source Charge[1,2]	Q_{gs}			0.6		
Gate-Drain Charge[1,2]	Q_{gd}			2.4		
Turn-On Delay Time[1,2]	$t_{d(on)}$	Vdd=50V, ID=14A, Rg=6.8 ohm, Vgs=10V		4.6		nS
Rise Time[1,2]	t_r			4.3		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			12.9		
Fall Time[1,2]	t_f			1.7		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				17	A
Pulsed Current[3]	I_{SM}				68	
Forward Voltage[1]	V_{SD}	I_F = 1A, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	IF=14A, di/dt=100 A/uS		50.5		nS
Reverse Recovery Charge	Q_{rr}			35.7		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

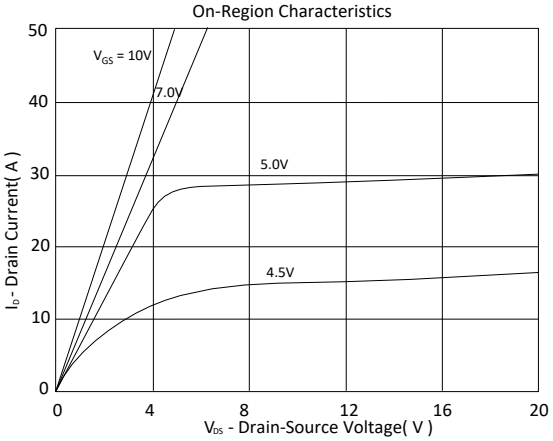
[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

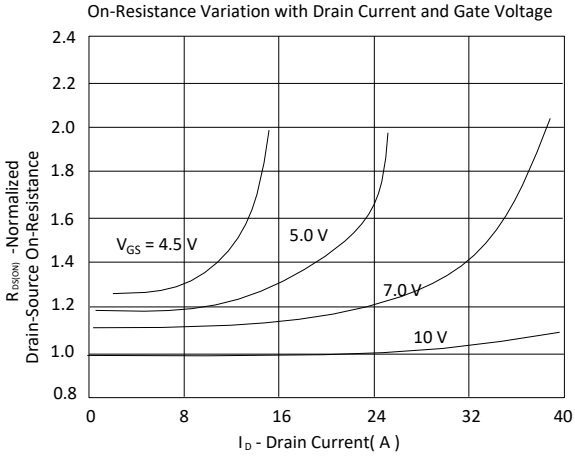
EMC will review datasheet by quarter, and update new version.

TYPICAL CHARACTERISTICS

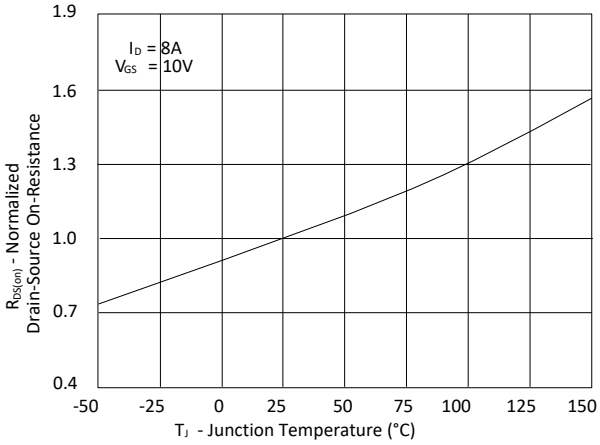
On-Region Characteristics



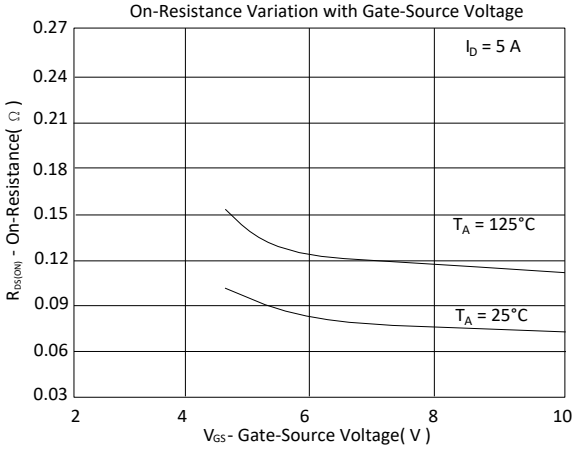
On-Resistance Variation with Drain Current and Gate Voltage



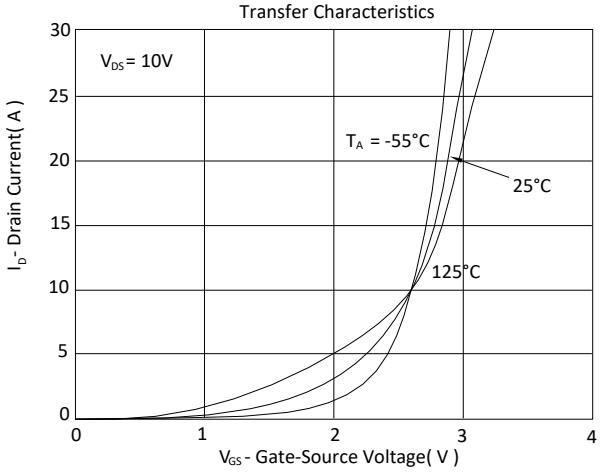
On-Resistance Variation with Temperature



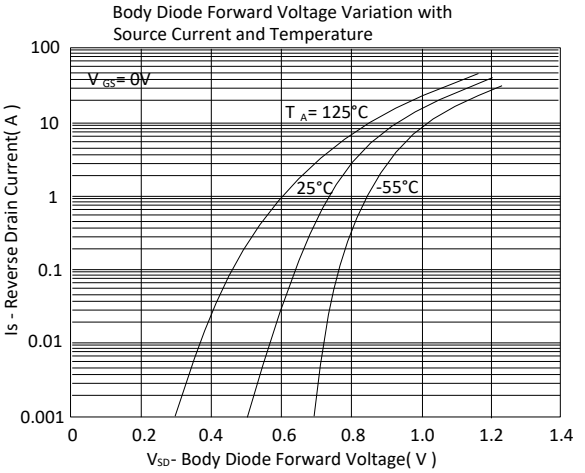
On-Resistance Variation with Gate-Source Voltage

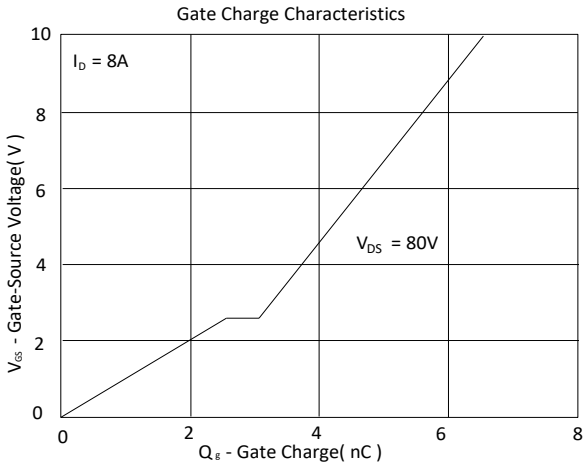


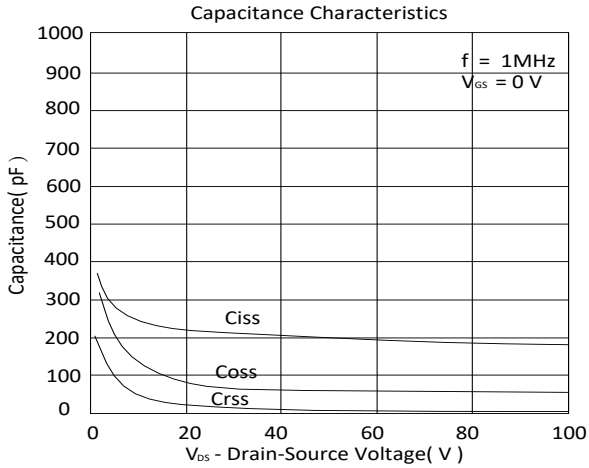
Transfer Characteristics

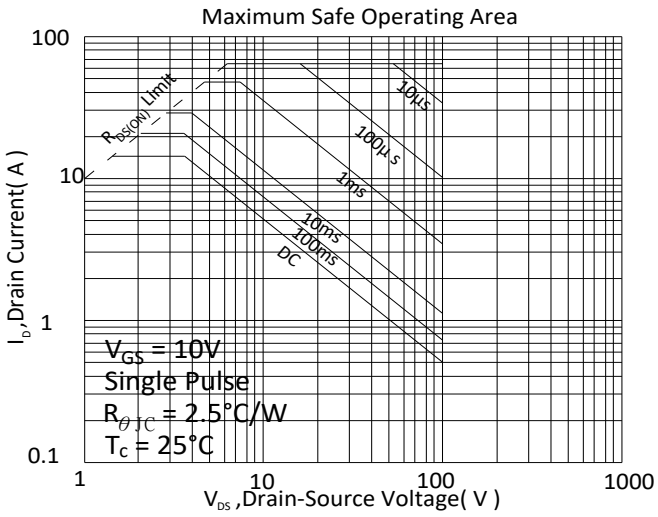


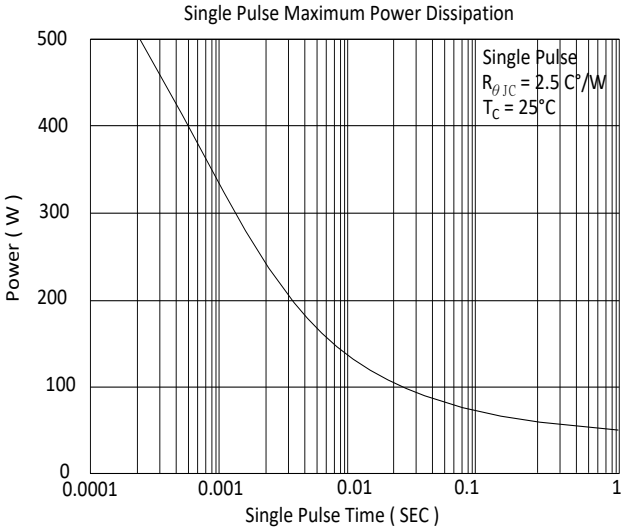
Body Diode Forward Voltage Variation with Source Current and Temperature

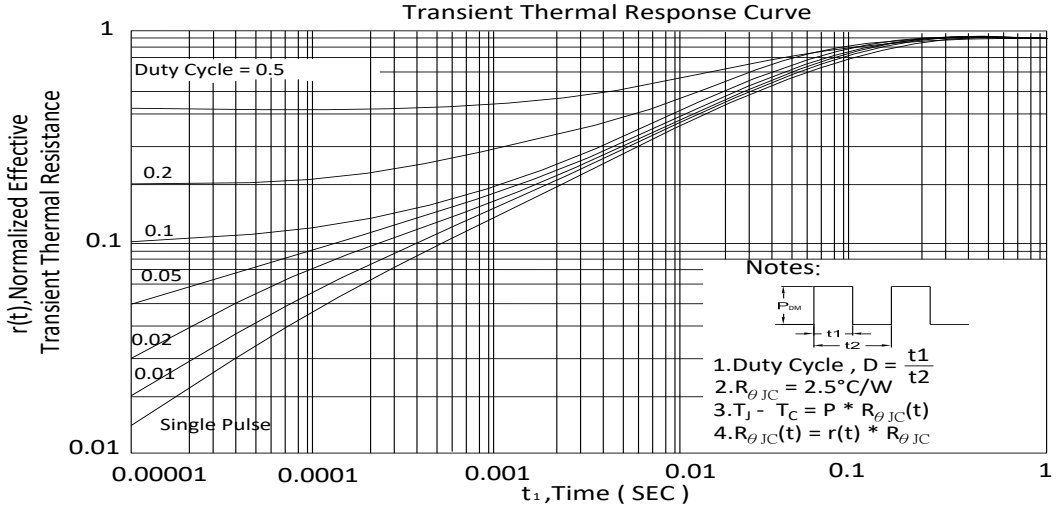



Gate Charge Characteristics
I_D = 8A
V_{DS} = 80V
V_{GS} - Gate-Source Voltage(V)
Q_g - Gate Charge(nC)


Capacitance Characteristics
f = 1MHz
V_{GS} = 0 V
Ciss
Coss
Crss
Capacitance(pF)
V_{DS} - Drain-Source Voltage(V)

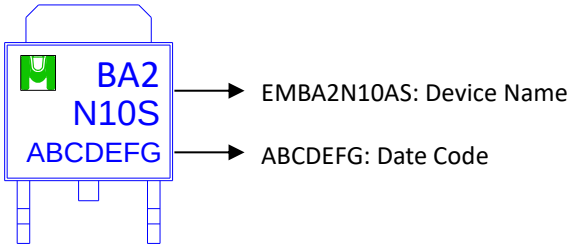

Maximum Safe Operating Area
$R_{DS(ON)}$ Limit
10μs
100μs
1ms
10ms
100ms
DC
V_{GS} = 10V
Single Pulse
$R_{\theta JC}$ = 2.5°C/W
T_C = 25°C
I_D,Drain Current(A)
V_{DS} ,Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
$R_{\theta JC}$ = 2.5 C°/W
T_C = 25°C
Power (W)
Single Pulse Time (SEC)

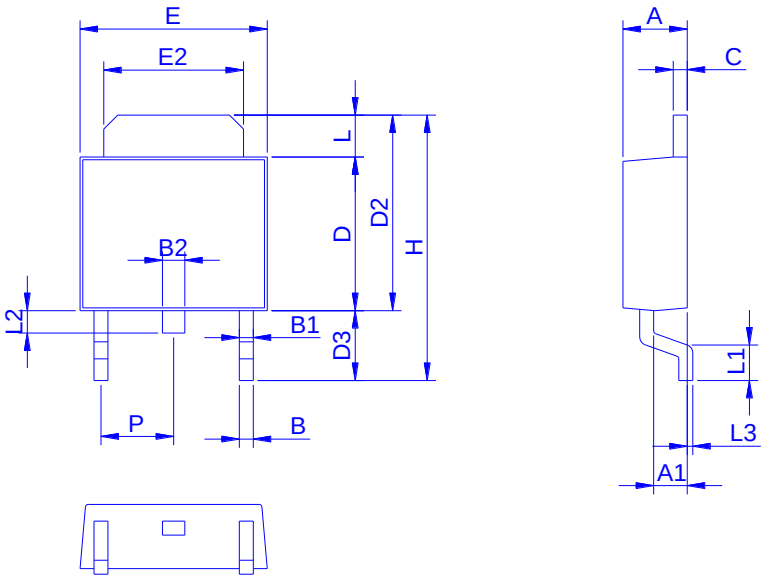

Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle , D = t1/t2
2.$R_{\theta JC}$ = 2.5°C/W
3.T_J - T_C = P * $R_{\theta JC}$(t)
4.$R_{\theta JC}$(t) = r(t) * $R_{\theta JC}$
r(t),Normalized Effective Transient Thermal Resistance
t_1,Time (SEC)

Ordering & Marking Information:

Device Name: EMBA2N10AS for DPAK (TO252-2)

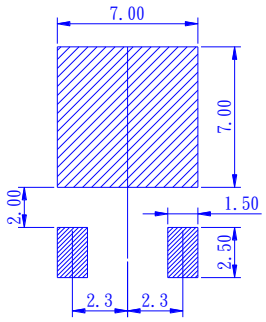


Outline Drawing

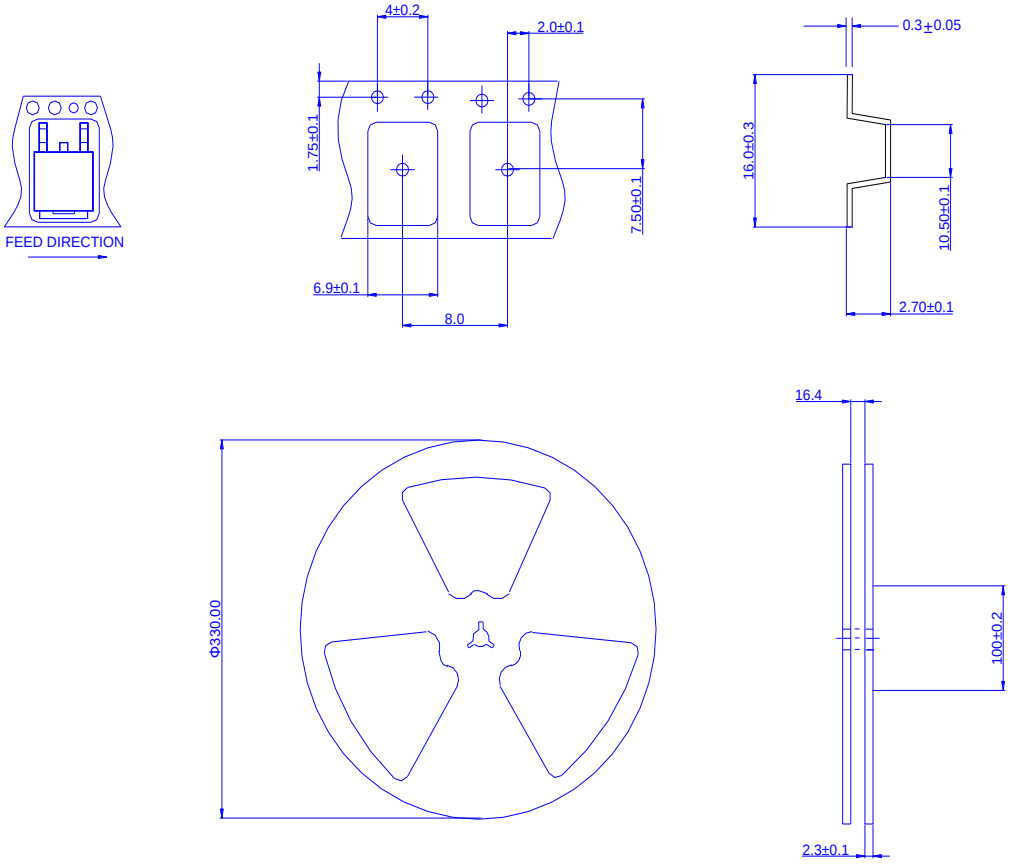


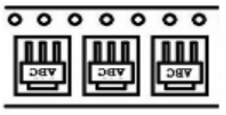
Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint



◆ Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)



產品別	TO252-2
Reel 尺寸	13”
編帶方式	FEED DIRECTION 
前空格	35
後空格	35
裝箱數	
滿捲數量	2.5K
捲/內盒比	1：1
內盒滿箱數	2.5K
內/外箱比	10：1