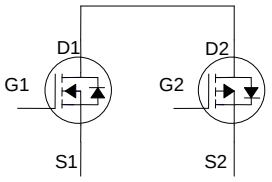
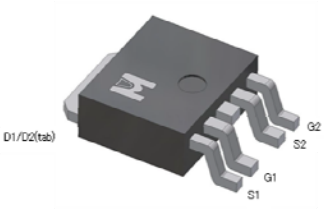
N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	100V	-100V
$R_{DSON\ (MAX.)}$	150mΩ	250mΩ
I_D	3A	-2.5A





Pb-Free Lead Plating & Halogen Free

GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	N-CH	P-CH	V
			±20	±20	
Continuous Drain Current	T_C = 25 °C	I_D	3	-2.5	A
	T_C = 100 °C		2.1	-1.8	
Pulsed Drain Current[1]		I_{DM}	12	-10	
Power Dissipation	T_C = 25 °C	P_D	10		W
	T_C = 100 °C		4		
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		12	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	N-CH	100			V
		V_{GS} = 0V, I_D = -250μA	P-CH	-100			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	N-CH	1.0	2.0	3.0	
		V_{DS} = V_{GS}, I_D = -250μA	P-CH	-1.0	-1.5	-3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	N-CH			±100	nA
		V_{DS} = 0V, V_{GS} = ±20V	P-CH			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V	N-CH			1	μA
		V_{DS} = -80V, V_{GS} = 0V	P-CH			-1	
		V_{DS} = 70V, V_{GS} = 0V, T_J = 125 °C	N-CH			25	
		V_{DS} = -70V, V_{GS} = 0V, T_J = 125 °C	P-CH			-25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	N-CH	3			A
		V_{DS} = -5V, V_{GS} = -10V	P-CH	-2.5			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2A	N-CH		125	150	mΩ
		V_{GS} = -10V, I_D = -1.5A	P-CH		210	250	
		V_{GS} = 5V, I_D = 1.5A	N-CH		168	225	
		V_{GS} = -5V, I_D = -1A	P-CH		280	375	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 2A	N-CH		8		S
		V_{DS} = -5V, I_D = -1.5A	P-CH		7		
DYNAMIC							
Input Capacitance	C_{iss}	N-CH	N-CH		1030		pF
		V_{GS} = 0V, V_{DS} = 20V, f = 1MHz	P-CH		2018		
Output Capacitance	C_{oss}	P-CH	N-CH		50		
		V_{GS} = 0V, V_{DS} = -20V, f = 1MHz	P-CH		82		
Reverse Transfer Capacitance	C_{rss}		N-CH		42		
			P-CH		61		

Total Gate Charge[1,2]	Q_g	N-CH V_{DS} = 80V, V_{GS} = 10V, I_D = 2A P-CH V_{DS} = -80V, V_{GS} = -10V, I_D = -1.5A	N-CH		23		nC
			P-CH		31		
Gate-Source Charge[1,2]	Q_{gs}		N-CH		2.3		
			P-CH		6.3		
Gate-Drain Charge[1,2]	Q_{gd}		N-CH		6.1		
			P-CH		4.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	N-CH V_{DS} = 50V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω P-CH V_{DS} = -50V, I_D = -1A, V_{GS} = -10V, R_{GS} = 6Ω	N-CH		12		nS
			P-CH		12		
Rise Time[1,2]	t_r		N-CH		20		
			P-CH		55		
Turn-Off Delay Time[1,2]	$t_{d(off)}$		N-CH		25		
			P-CH		40		
Fall Time[1,2]	t_f		N-CH		25		
			P-CH		40		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		N-CH			3	A
			P-CH			-2.5	
Pulsed Current[3]	I_{SM}		N-CH			12	
			P-CH			-10	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V	N-CH			1.3	V
			P-CH			-1.3	

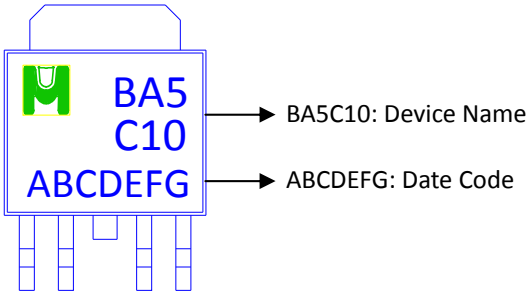
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

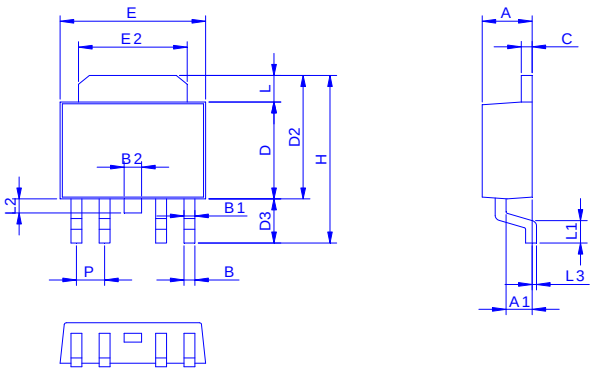
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMBA5C10A for DPAK (TO-252)



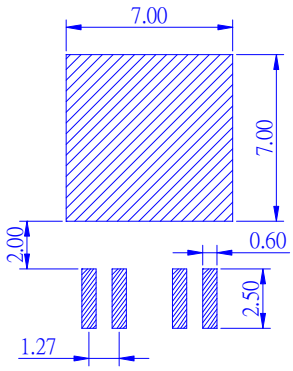
Outline Drawing



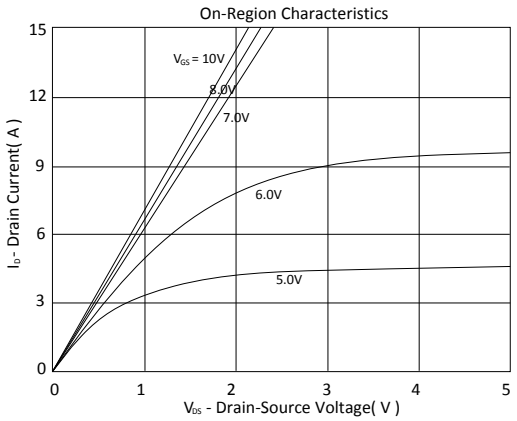
Dimension in mm

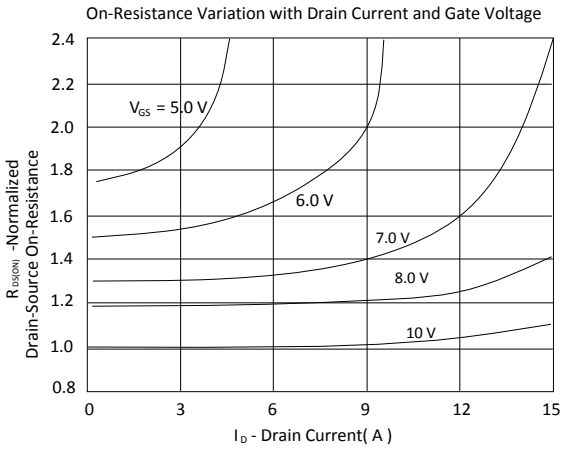
Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	1.10	0.30	0.55	0.40	0.40	5.30	6.70	2.20	6.30	4.80	9.20	1.30	0.90	0.50	0.00	1.17
Max.	2.50	1.30	0.70	0.75	0.80	0.60	5.70	7.30	3.00	6.70	5.45	10.15	1.70	1.50	1.10	0.30	1.37

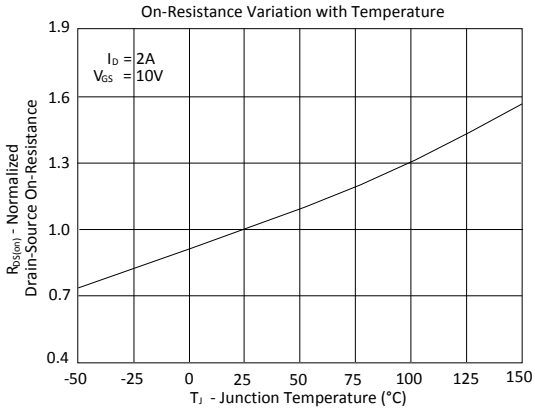
Footprint

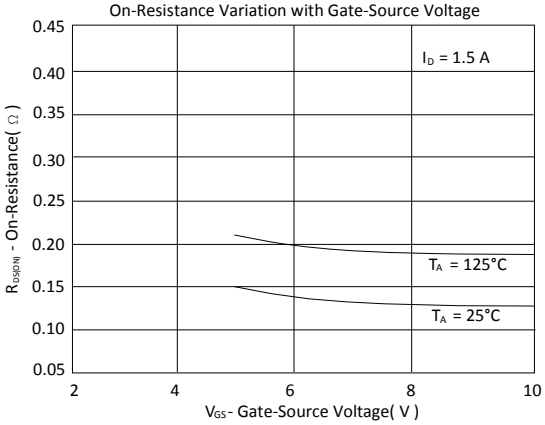


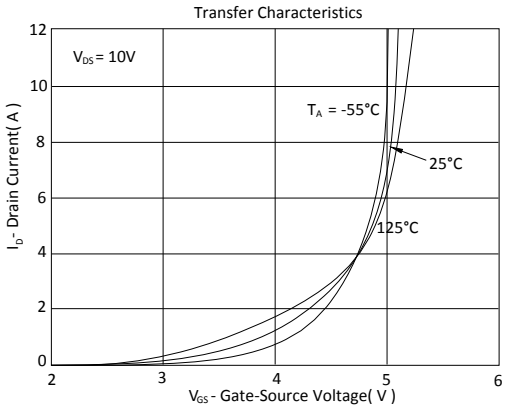
N-Channel

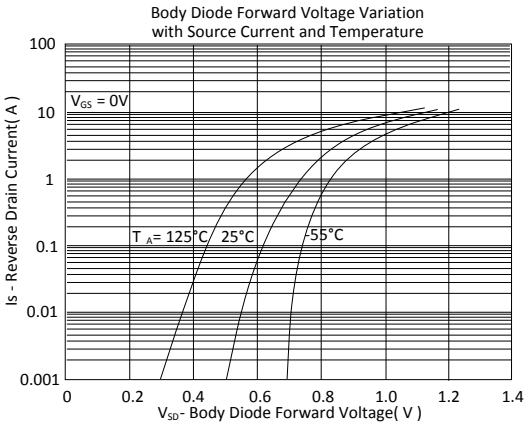

On-Region Characteristics
V_{GS} = 10V
8.0V
7.0V
6.0V
5.0V
I_D - Drain Current(A)
V_{DS} - Drain-Source Voltage(V)


On-Resistance Variation with Drain Current and Gate Voltage
V_{GS} = 5.0 V
6.0 V
7.0 V
8.0 V
10 V
$R_{DS(ON)}$ -Normalized
Drain-Source On-Resistance
I_D - Drain Current(A)

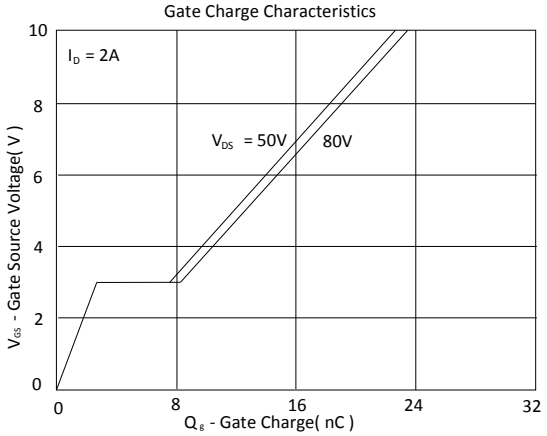

On-Resistance Variation with Temperature
I_D = 2A
V_{GS} = 10V
$R_{DS(on)}$ - Normalized
Drain-Source On-Resistance
T_J - Junction Temperature (°C)


On-Resistance Variation with Gate-Source Voltage
I_D = 1.5 A
T_A = 125°C
T_A = 25°C
$R_{DS(ON)}$ - On-Resistance(Ω)
V_{GS} - Gate-Source Voltage(V)

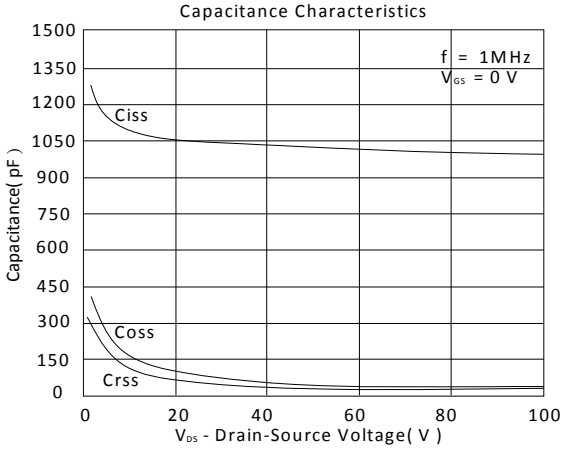

Transfer Characteristics
V_{DS} = 10V
T_A = -55°C
25°C
125°C
I_D - Drain Current(A)
V_{GS} - Gate-Source Voltage(V)


Body Diode Forward Voltage Variation
with Source Current and Temperature
V_{GS} = 0V
T_A= 125°C
25°C
-55°C
Is - Reverse Drain Current(A)
V_{SD} - Body Diode Forward Voltage(V)

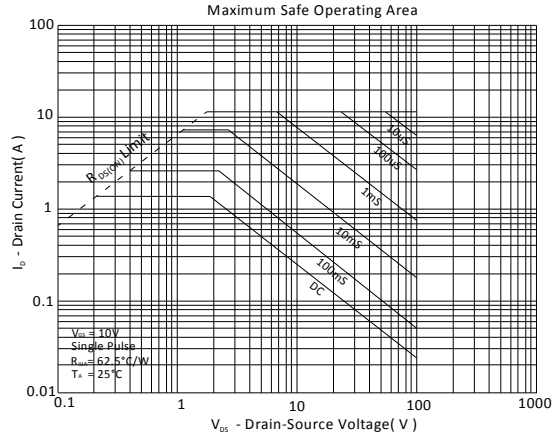
Gate Charge Characteristics



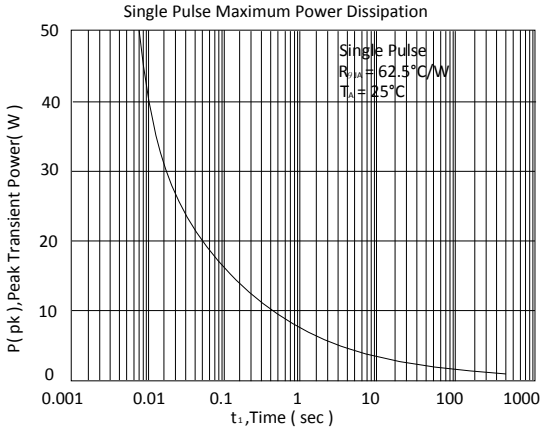
Capacitance Characteristics



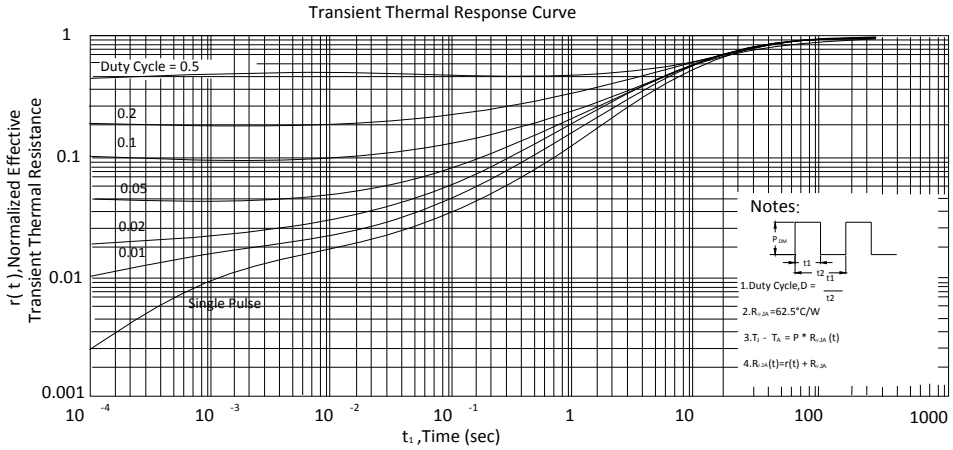
Maximum Safe Operating Area



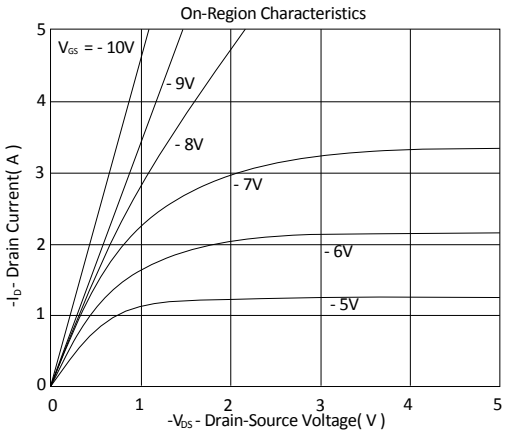
Single Pulse Maximum Power Dissipation

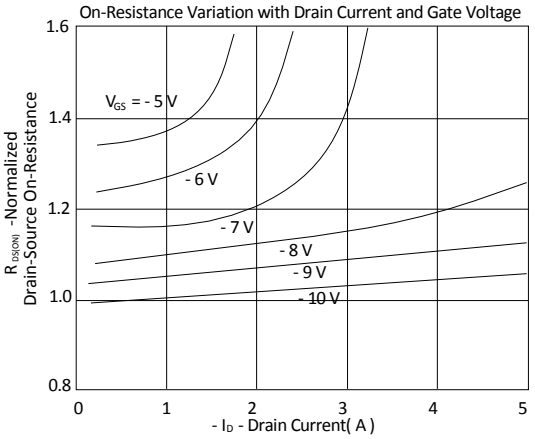


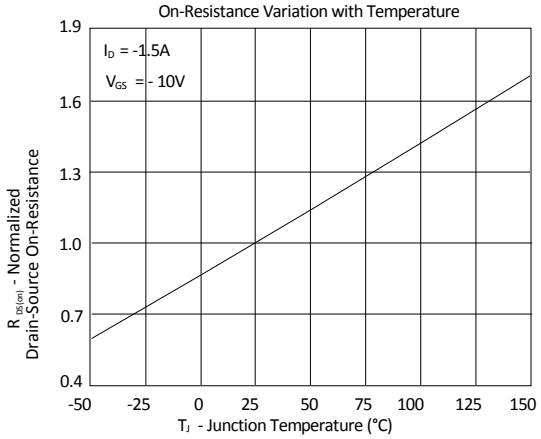
Transient Thermal Response Curve

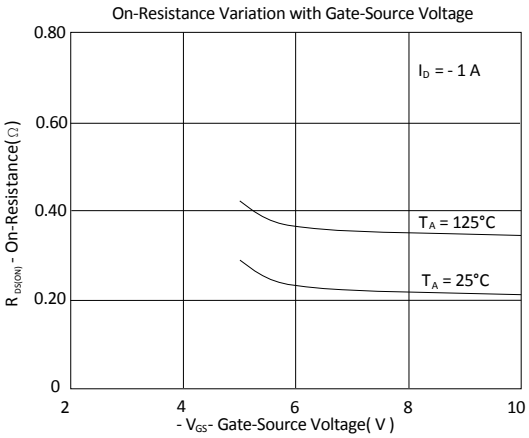


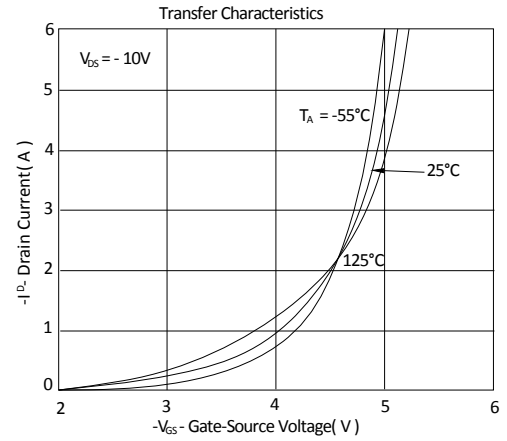
P-Channel

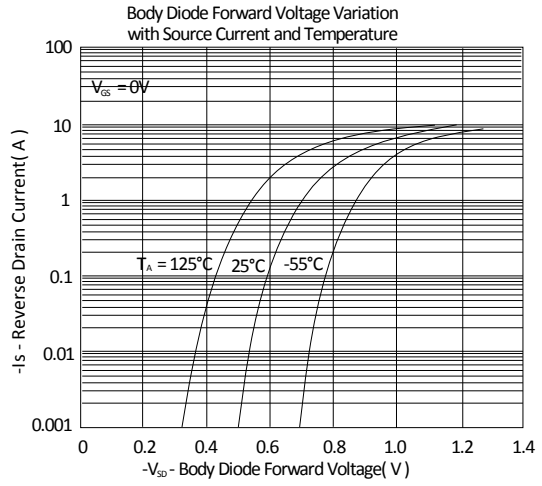

On-Region Characteristics
V_{GS} = - 10V
- 9V
- 8V
- 7V
- 6V
- 5V
$-I_D$- Drain Current(A)
$-V_{DS}$ - Drain-Source Voltage(V)

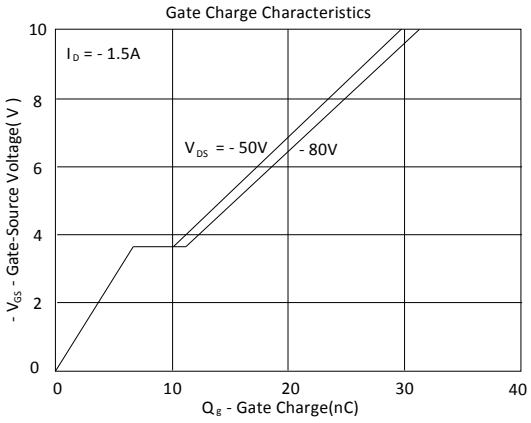

On-Resistance Variation with Drain Current and Gate Voltage
V_{GS} = - 5 V
- 6 V
- 7 V
- 8 V
- 9 V
- 10 V
$R_{DS(ON)}$ -Normalized
Drain-Source On-Resistance
- I_D - Drain Current(A)

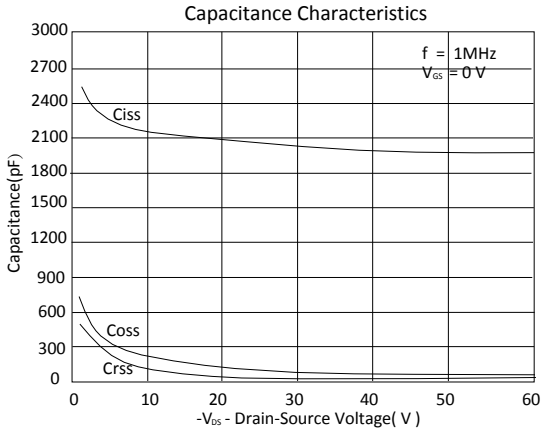

On-Resistance Variation with Temperature
I_D = -1.5A
V_{GS} = - 10V
$R_{DS(on)}$ - Normalized
Drain-Source On-Resistance
T_J - Junction Temperature (°C)

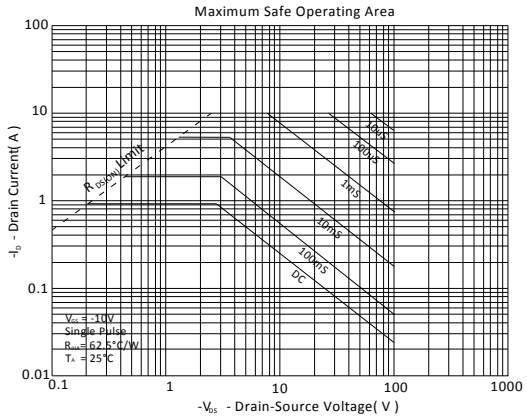

On-Resistance Variation with Gate-Source Voltage
I_D = - 1 A
T_A = 125°C
T_A = 25°C
$R_{DS(ON)}$ - On-Resistance(Ω)
- V_{GS}- Gate-Source Voltage(V)

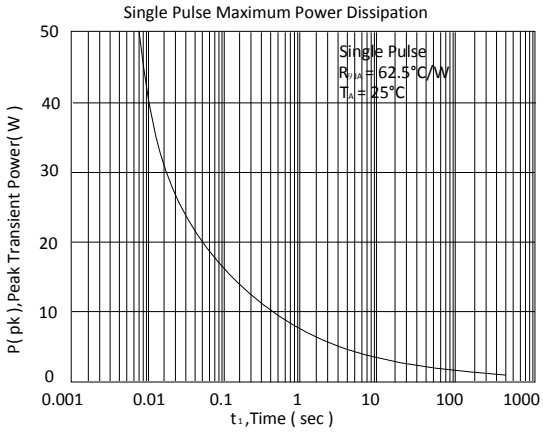

Transfer Characteristics
V_{DS} = - 10V
T_A = -55°C
25°C
125°C
$-I^{D}$- Drain Current(A)
$-V_{GS}$ - Gate-Source Voltage(V)

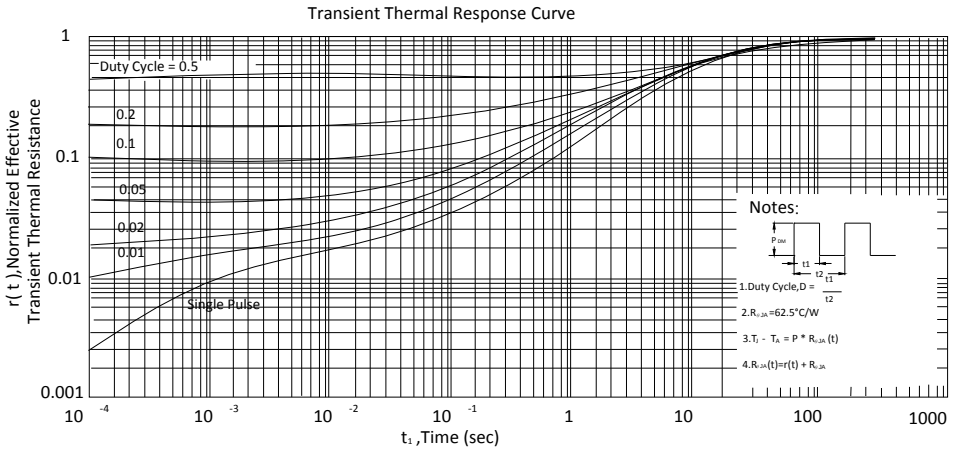

Body Diode Forward Voltage Variation
with Source Current and Temperature
V_{GS} = 0V
T_A = 125°C
25°C
-55°C
-Is - Reverse Drain Current(A)
$-V_{SD}$ - Body Diode Forward Voltage(V)


Gate Charge Characteristics
I D = - 1.5A
V DS = - 50V
- 80V
- VGS - Gate-Source Voltage(V)
Qg - Gate Charge(nC)


Capacitance Characteristics
f = 1MHz
VGS = 0 V
Ciss
Coss
Crss
Capacitance(pF)
-VDS - Drain-Source Voltage(V)


Maximum Safe Operating Area
RDS(on) Limit
10ms
100ms
1s
10s
100s
DC
VGS = -10V
Single Pulse
RθJA=62.5°C/W
TA = 25°C
-ID - Drain Current(A)
-VDS - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
RθJA=62.5°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D = t1/t2
2.RθJA=62.5°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) + RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)