

N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DS(on)} (MAX.)$	500m Ω
I_D	0.9A



UIS 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	0.9	A
	$T_A = 100\text{ }^{\circ}\text{C}$		0.55	
Pulsed Drain Current ¹		I_{DM}	3.6	
Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	1.04	W
	$T_A = 100\text{ }^{\circ}\text{C}$		0.66	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient ³	$R_{\theta JA} (T \leq 10\text{sec})$		83	$^{\circ}\text{C} / \text{W}$
	$R_{\theta JA} (\text{Steady State})$		120	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³The device mounted on a 1 in² pad of 2 oz copper.

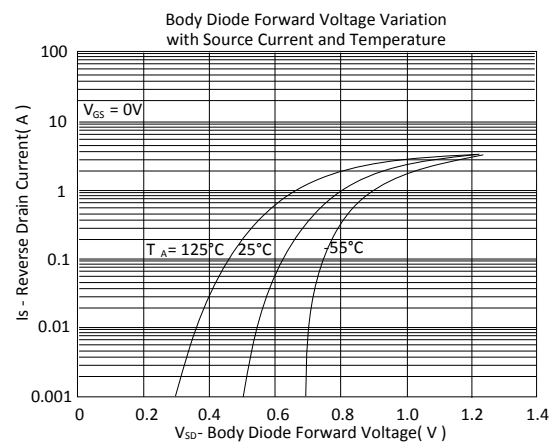
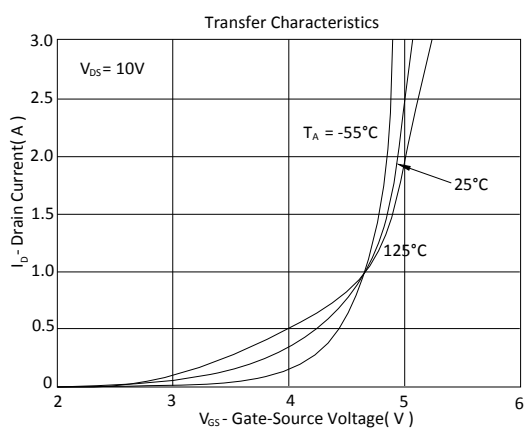
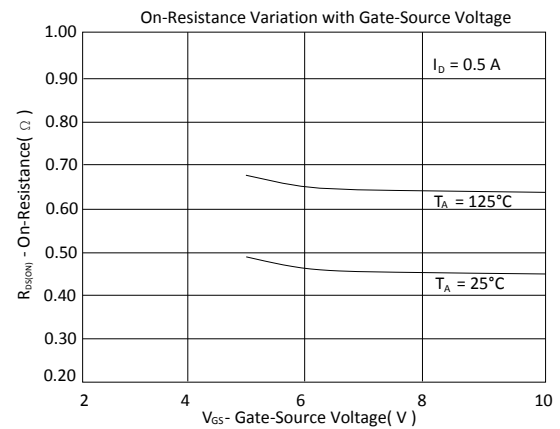
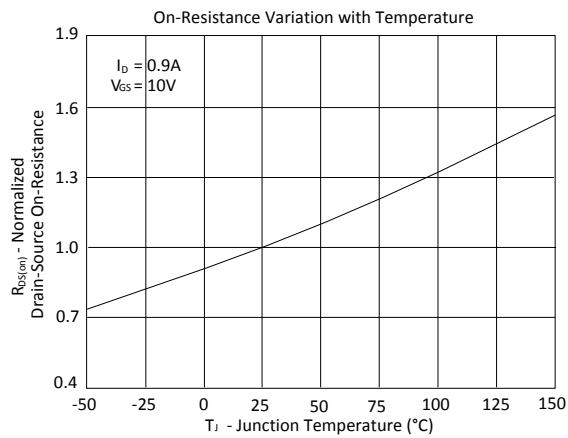
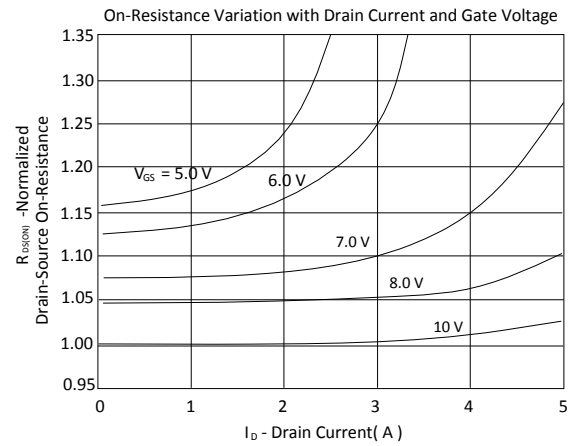
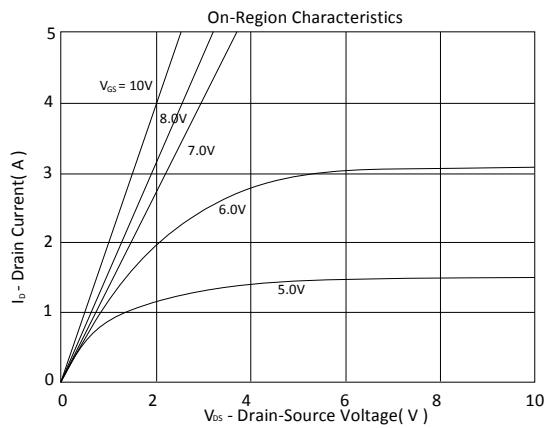
ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

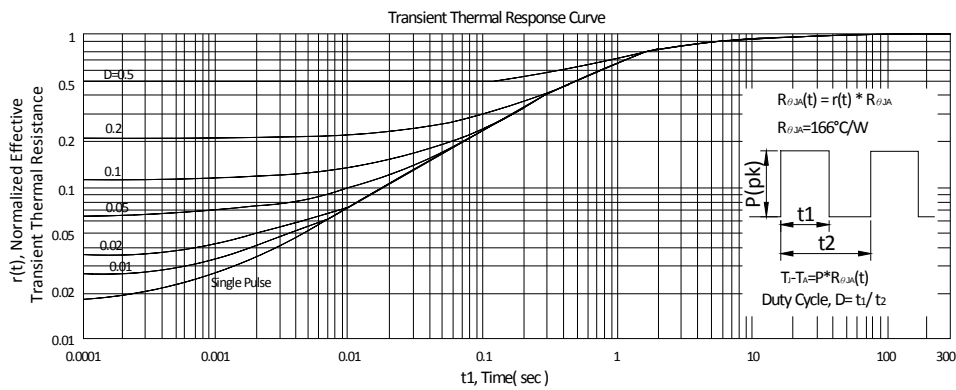
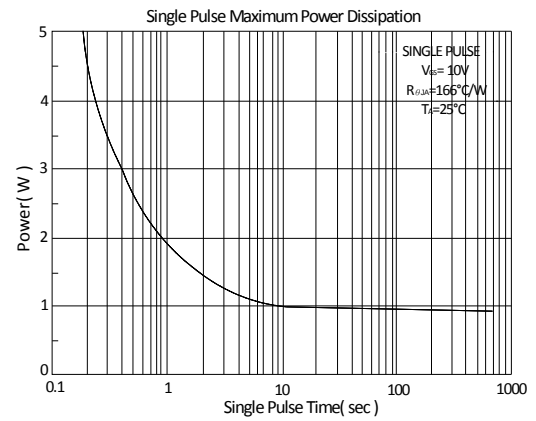
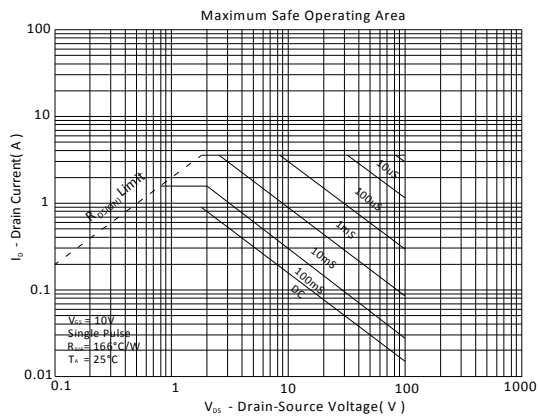
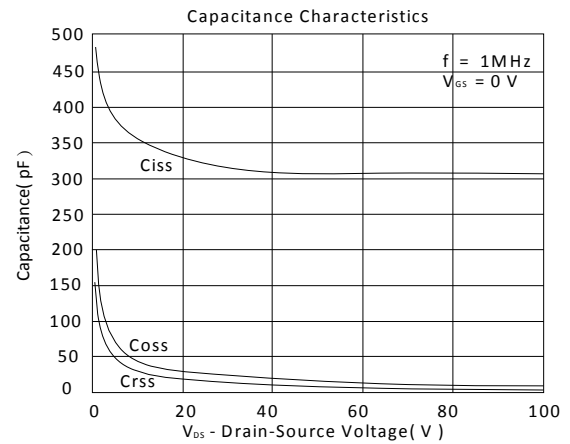
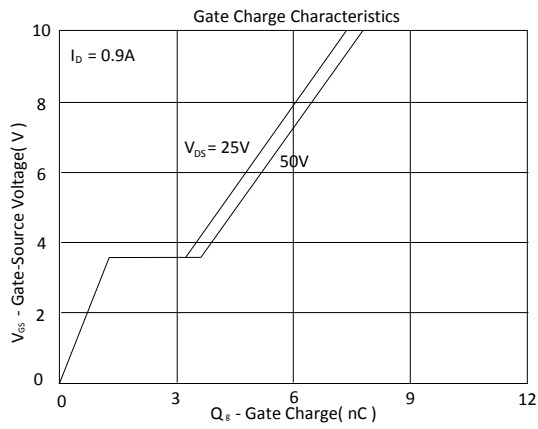
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	2	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V$			1	μA
		$V_{DS} = 70V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	0.9			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 0.9A$		450	500	m Ω
		$V_{GS} = 5V, I_D = 0.5A$		485	570	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 0.9A$		2		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 50V, f = 1MHz$		328		pF
Output Capacitance	C_{oss}			35		
Reverse Transfer Capacitance	C_{rss}			21		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 50V, V_{GS} = 10V,$ $I_D = 0.9A$		7.6		nC
Gate-Source Charge ^{1,2}	Q_{gs}			1.1		
Gate-Drain Charge ^{1,2}	Q_{gd}			2.7		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 50V,$ $I_D = 0.9A, V_{GS} = 10V, R_{GS} = 6\Omega$		12		nS
Rise Time ^{1,2}	t_r			15		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			25		
Fall Time ^{1,2}	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I_S				0.9	A
Pulsed Current ³	I_{SM}				3.6	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	t_{rr}			30		nS
Reverse Recovery Charge	Q_{rr}			60		nC

¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

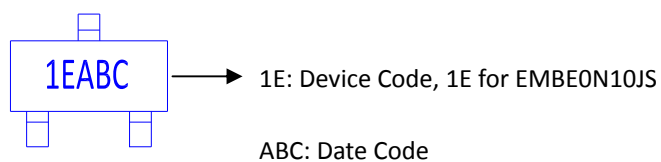
³Pulse width limited by maximum junction temperature.



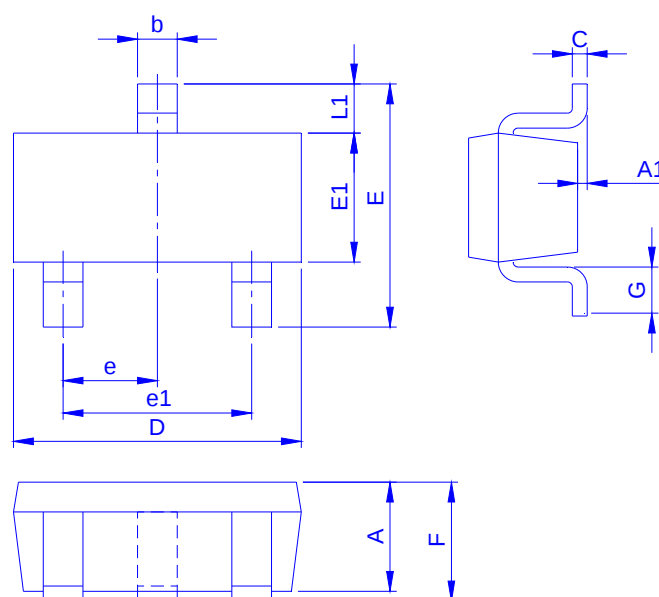


Ordering & Marking Information:

Device Name: EMBE0N10JS for SOT-23



Outline Drawing



Dimension in mm

Dimension	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.70	0	0.3	0.08	2.80	2.25	1.2	0.90		0.80	0.3	0.50
Typ.					2.90			0.95	1.9			
Max.	1.15	0.1	0.5	0.20	3.02	3.00	1.7	1.00		1.25	0.6	0.75

Footprint

