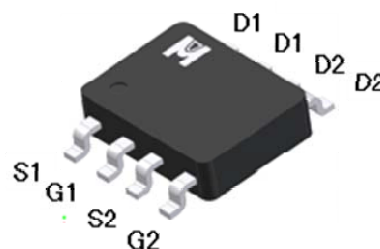
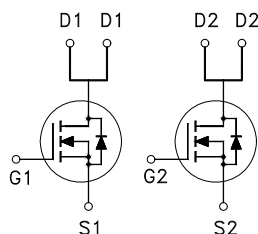


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	250V
$R_{DS(on)} (MAX.)$	1.7Ω
I_D	0.5A



R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	0.5	A
	$T_A = 100^\circ\text{C}$		0.3	
Pulsed Drain Current ¹		I_{DM}	2	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³62.5 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	250			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.0		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200V, V_{GS} = 0V$			1	μA	
		$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ C$			25		
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	0.5			A	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 0.25A$		1.35	1.7	m Ω	
		$V_{GS} = 5V, I_D = 0.15A$		1.5	2.0		
Forward Transconductance ¹	g_{fs}	$V_{DS} = 50V, I_D = 0.25A$		2.0		S	
DYNAMIC							
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		680		pF	
Output Capacitance	C_{oss}			15			
Reverse Transfer Capacitance	C_{rss}			13			
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		3.0		Ω	
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 200V, V_{GS} = 10V, I_D = 0.25A$		17.8		nC	
Gate-Source Charge ^{1,2}	Q_{gs}			2.2			
Gate-Drain Charge ^{1,2}	Q_{gd}			4.4			
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 125V, I_D = 0.1A, V_{GS} = 10V, R_G = 6\Omega$		10		nS	
Rise Time ^{1,2}	t_r			40			
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			12			
Fall Time ^{1,2}	t_f			20			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)							
Continuous Current	I_S				0.5	A	
Pulsed Current ³	I_{SM}				2		
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V	

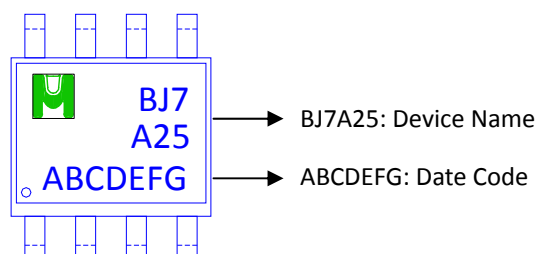
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

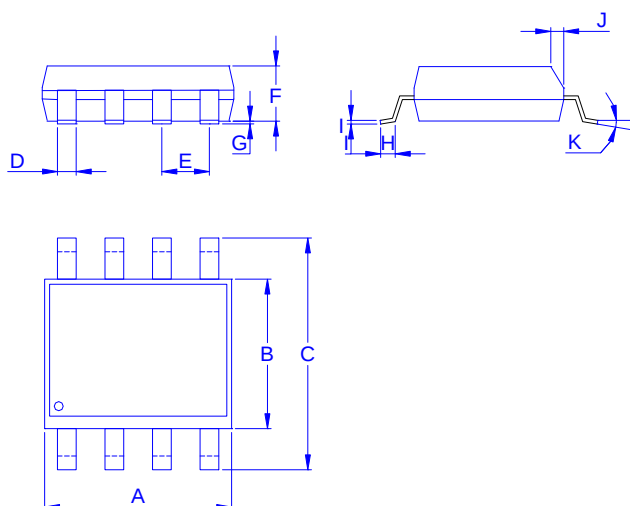
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMBJ7A25G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°



TYPICAL CHARACTERISTICS

