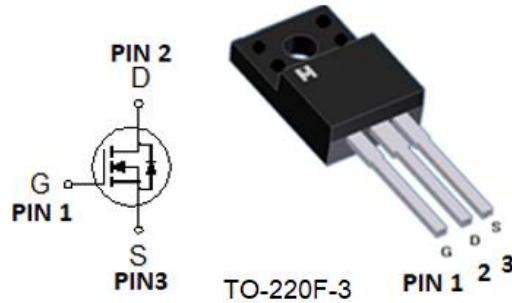


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	75V
R _{DS(on)} (MAX.)	4.4mΩ
I _D	86A

Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±30	V
Continuous Drain Current	T _C = 25 °C	I _D	86	A
	T _C = 100 °C		54	
Pulsed Drain Current ¹		I _{DM}	200	
Avalanche Current		I _{AS}	90	
Avalanche Energy	L = 0.1mH, I _D =90A, R _G =25Ω	E _{AS}	405	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	202	
Power Dissipation	T _C = 25 °C	P _D	56	W
	T _C = 100 °C		22	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=38V, L=0.1mH, V_G=10V, I_L=40A, Rated V_{DS}=75V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		2.2	°C / W
Junction-to-Ambient	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³Pulsed drain current rating is package limited.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	75			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 30V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V, V_{GS} = 0V$			1	μA
		$V_{DS} = 50V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	86			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 24A$		3.9	4.4	m Ω
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 24A$		60		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 40V, f = 1MHz$		5526		pF
Output Capacitance	C_{oss}			584		
Reverse Transfer Capacitance	C_{rss}			33		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.8		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 40V, V_{GS} = 10V,$ $I_D = 24A$		59		nC
Gate-Source Charge ^{1,2}	Q_{gs}			38		
Gate-Drain Charge ^{1,2}	Q_{gd}			9.7		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 40V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		75		nS
Rise Time ^{1,2}	t_r			140		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			100		
Fall Time ^{1,2}	t_f			160		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				86	A
Pulsed Current ³	I_{SM}				200	
Forward Voltage ¹	V_{SD}	$I_F = 24A, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 24A, di_F/dt = 100A / \mu S$		70		nS
Reverse Recovery Charge	Q_{rr}			250		nC

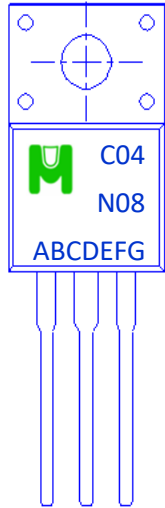
¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMC04N08F for TO-220F



→ C04N08: Device Name

→ ABCDEFG: Date Code

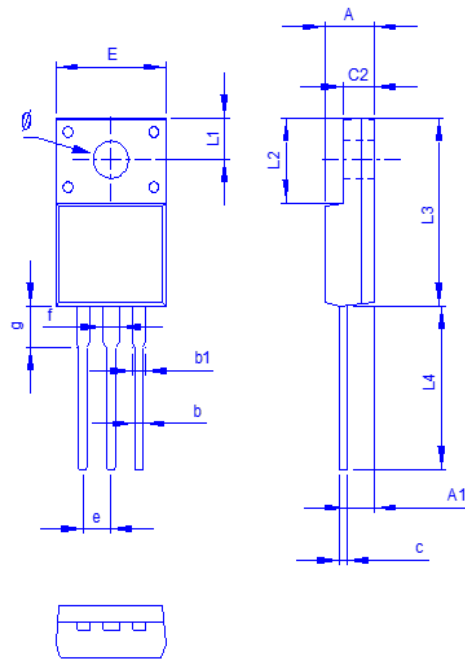
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

Outline Drawing

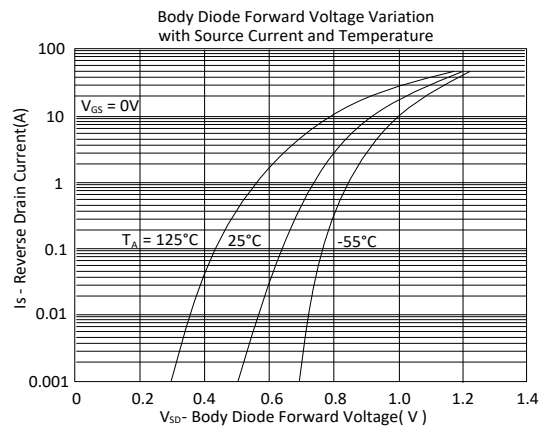
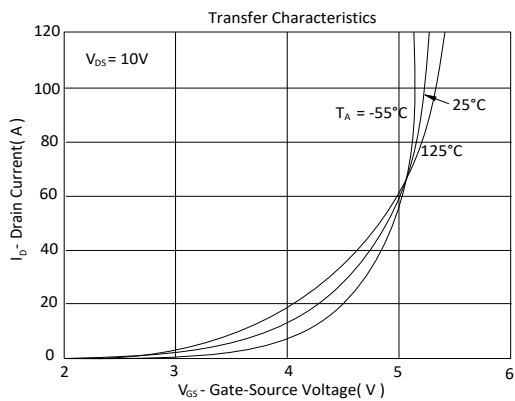
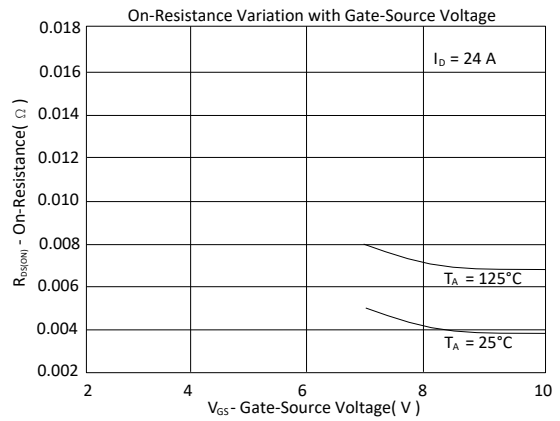
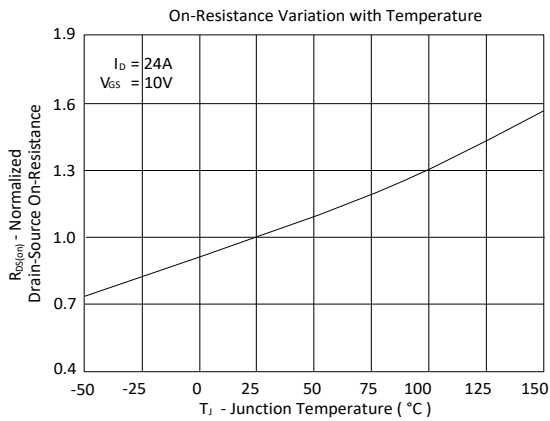
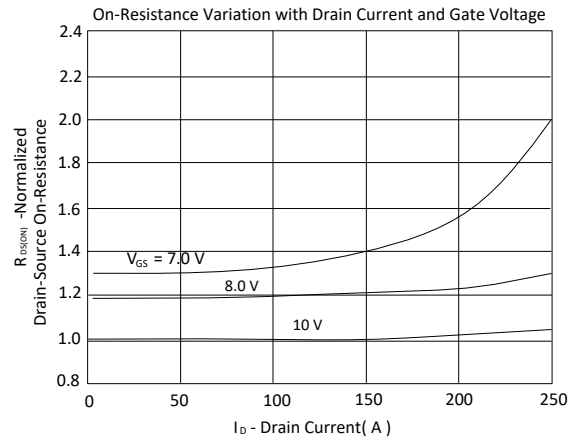
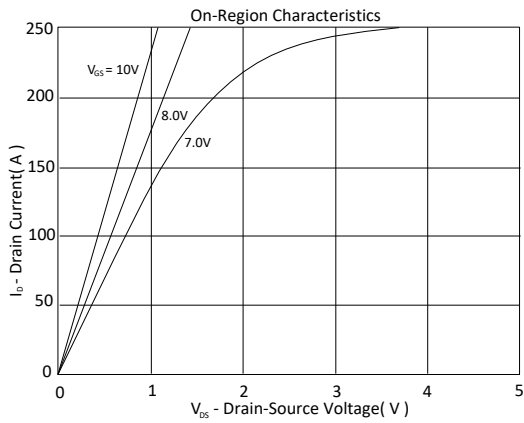


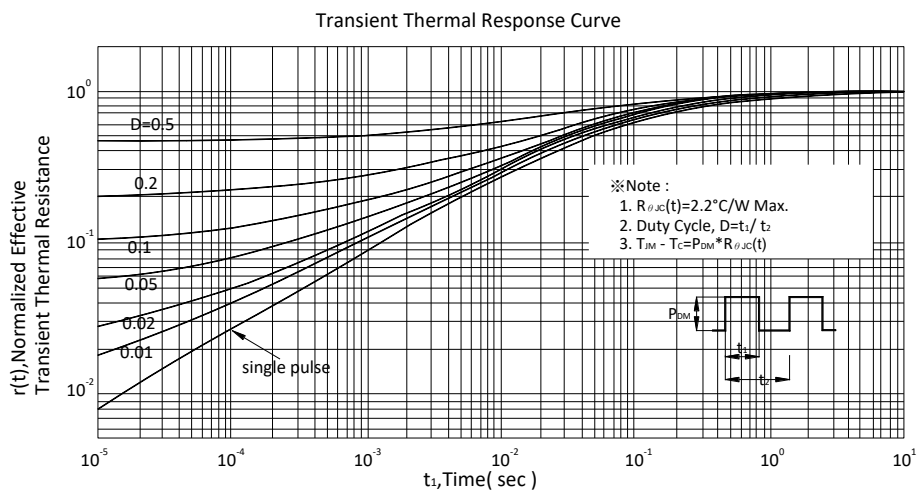
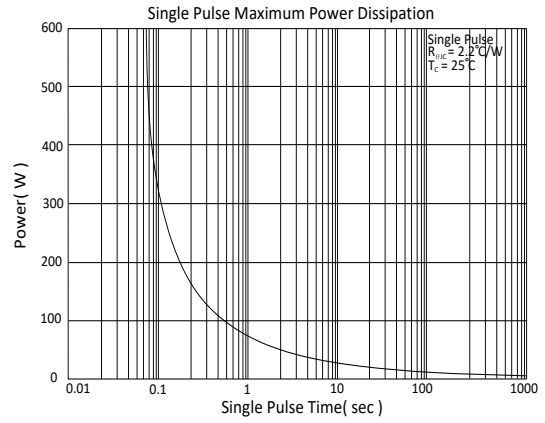
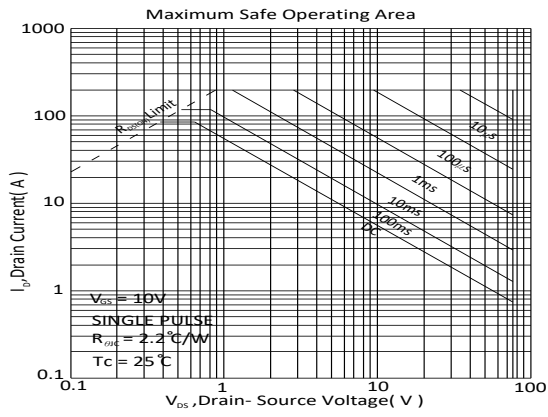
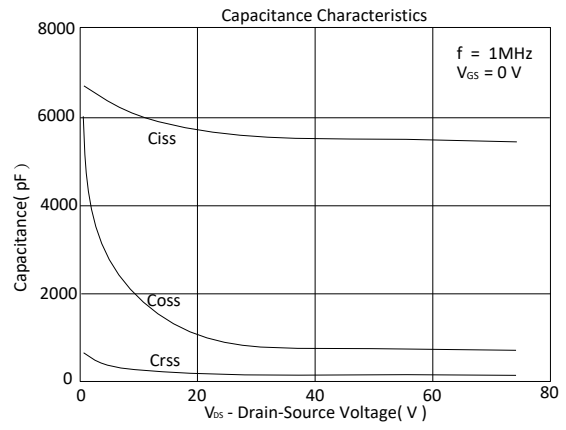
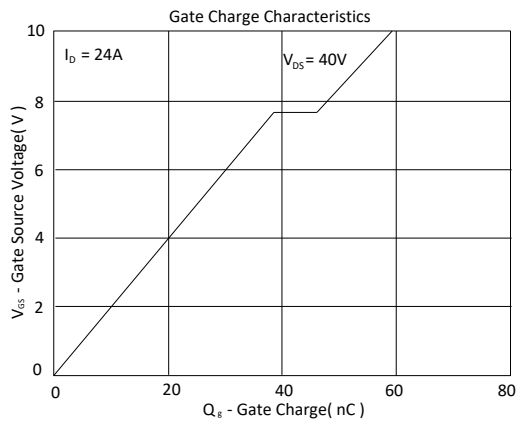
Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L1	L2	L3	L4	ϕ	e	f	g
Min.	4.3	2.49	0.5	1.1	0.4	2.34	9.96	2.7	6.48	14.8	12.65	3	2.44	1.17	2.93
Typ.	4.5	2.59	0.8	1.3	0.5	2.54	10.1	3.25	6.68	15.87	12.98	3.1	2.54	1.28	3.03
Max.	4.9	2.96	0.95	1.6	0.75	3.2	10.36	3.45	6.9	16.2	13.5	3.38	2.64	1.75	4



TYPICAL CHARACTERISTICS







◆ Tube Information: 50pcs/Tube (1000pcs/Box)

