EMC1412

Multiple Channel 1°C Temperature Sensor with Beta Compensation

Features

- Programmable SMBus Address
- Support for diodes requiring the BJT/transistor model including advanced processor geometries
- Automatically determines external diode type and optimal settings
- Resistance Error Correction
- External Temperature Monitor:
  - ±1°C Maximum Accuracy (+20°C < T_{DIODE} < +110°C)
  - 0.125°C resolution
  - Supports up to 2.2 nF Diode Filter Capacitor
- Internal Temperature Monitor:
  - ±1°C Accuracy
  - 0.125°C Resolution
- 3.3V Supply Voltage
- Programmable temperature limits for $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$
- Available in small 8-pin 2 mm x 3 mm TDFN RoHS compliant package
- Available in small 8-pin MSOP RoHS compliant package

Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded Applications

Description

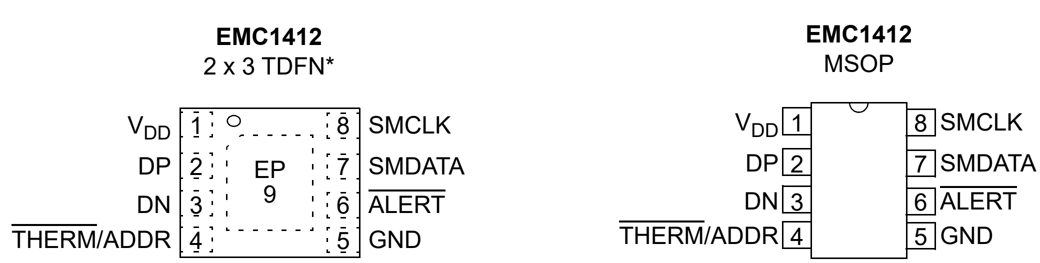
The EMC1412 is a high accuracy, low cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

The EMC1412 monitors two temperature channels (one external and one internal). It provides ±1°C accuracy for both external and internal diode temperatures.

Resistance Error Correction automatically eliminates the temperature error caused by series resistance, allowing greater flexibility in routing thermal diodes.

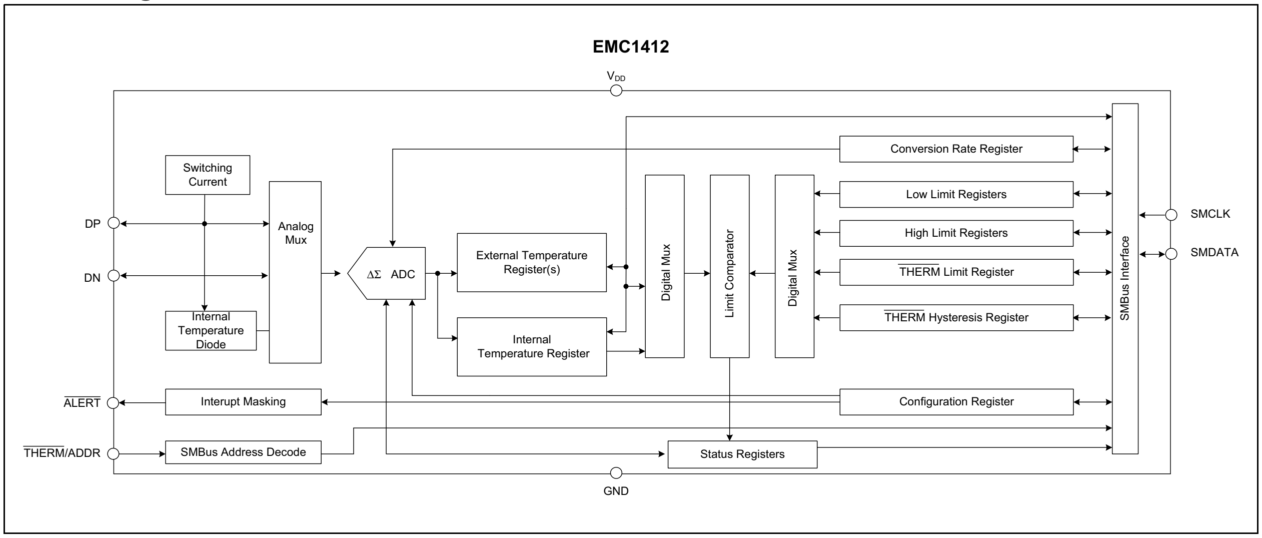
Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements, regardless of the processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application. These advanced features plus ±1°C measurement accuracy provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

Package Type



*Includes Exposed Thermal Pad (EP); see Table 3-1.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Supply Voltage (V_{DD}) .... -0.3V to +4.0V
Voltage on 5V tolerant pins (V_{5VT_PIN}) .... -0.3V to +5.5V
Voltage on 5V tolerant pins ($|V_{5VT\_PIN} - V_{DD}|$) (Note) .... 0V to +3.6V
Voltage on any other pin to Ground .... -0.3V to (V_{DD} + 0.3V)
ESD Rating, All pins HBM 2000V
Operating Temperature Range .... -40°C to +125°C
Storage Temperature Range .... -55°C to +150°C
Lead Temperature Range .... Refer to JEDEC Spec. J-STD-020

Note: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{ALERT}}$, and $\overline{\text{THERM}}$), the pull-up voltage must not exceed 3.6V when the device is unpowered.

Note: **† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, 3.0V ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C, all typical values are at T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	—
Supply Current	I_{DD}	—	430	850	µA	1 conversion/second, dynamic averaging disabled
		—	930	1200	µA	4 conversions/second, dynamic averaging enabled
		—	1120	—	µA	≥16 conversions/second, dynamic averaging enabled
Standby Supply Current	I_{DD_OS}	—	170	230	µA	Device in Standby mode, no SMBus communications, $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins not asserted.
Internal Temperature Monitor						
Temperature Accuracy	—	—	±0.25	±1	°C	-5°C < T_A < +100°C
		—		±2	°C	-40°C < T_A < +125°C
Temperature Resolution		—	0.125		°C	—
External Temperature Monitor						
Temperature Accuracy	—	—	±0.25	±1	°C	+20°C < T_{DIODE} < +110°C 0°C < T_A < +100°C
		—	±0.5	±2	°C	-40°C < T_{DIODE} < +127°C
Temperature Resolution	—	—	0.125	—	°C	—

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Electrical Characteristics: Unless otherwise specified, 3.0V ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C, all typical values are at T_A = 27°C.						
Timing and Capacitive Filter						
Conversion Time all Channels	t_{CONV}	—	190	—	ms	Default settings
Capacitive Filter	C_{FILTER}	—	2.2	2.7	nF	Connected across external diode
Resistance Error Correction	R_{SERIES}	—	—	100	Ω	In series with DP and DN lines
$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ Pins						
Output Low Voltage	V_{OL}	0.4	—	—	V	I_{SINK} = 8 mA
Leakage Current	I_{LEAK}	—	—	±5	µA	$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins Device powered or unpowered T_A < +85°C Pull-up voltage ≤ 3.6V

TABLE 1-2: SMBUS TIMING SPECIFICATION

Electrical Characteristics: Unless otherwise specified, 3.0V ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C, all typical values are at T_A = 27°C.

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
SMBus Interface						
Input High Voltage	V_{IH}	2.0	—	V_{DD}	V	5V Tolerant
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	5V Tolerant
Leakage Current	I_{LEAK}	—	—	±5	µA	Powered or unpowered T_A < +85°C
Hysteresis	—	—	420	—	mV	—
Input Capacitance	C_{IN}	—	5	—	pF	—
Output Low Sink Current	I_{OL}	8.2	—	15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	—
Spike Suppression	t_{SP}	—	—	50	ns	—
Bus free Time Start to Stop	t_{BUF}	1.3	—	—	µs	—
Hold Time: Start	$t_{HD:STA}$	0.6	—	—	µs	—
Setup Time: Start	$t_{SU:STA}$	0.6	—	—	µs	—
Setup Time: Stop	$t_{SU:STP}$	0.6	—	—	µs	—
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	—
Clock Low Period	t_{LOW}	1.3	—	—	µs	—
Clock High Period	t_{HIGH}	0.6	—	—	µs	—
Clock/Data Fall time	t_{FALL}	—	—	300	ns	Min = 20 + 0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}	—	—	300	ns	Min = 20 + 0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	per bus line

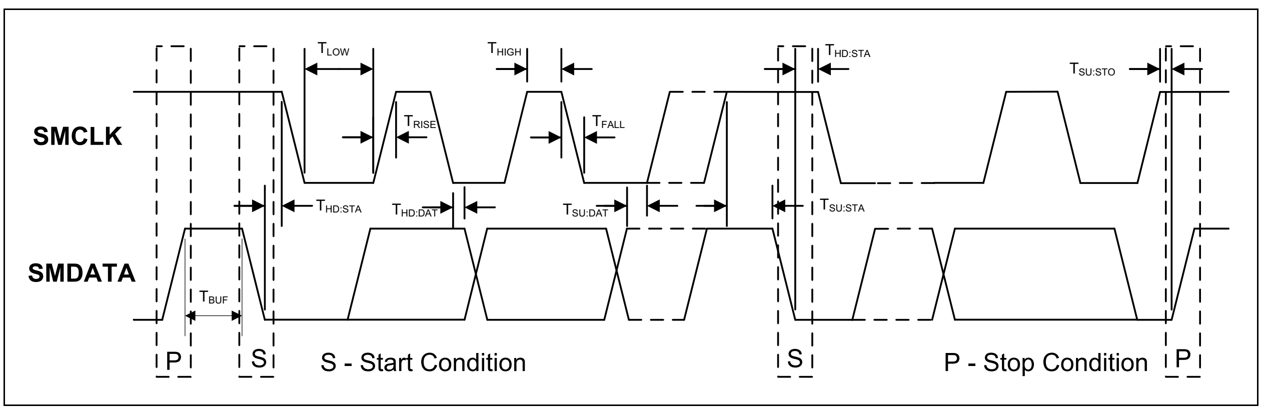


FIGURE 1-1: SMBus Timing.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

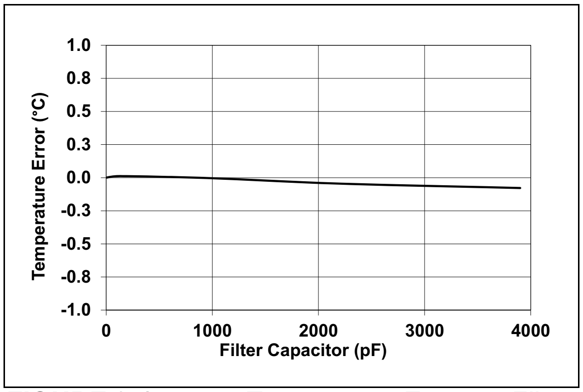


FIGURE 2-1: *Temperature Error vs. Filter Capacitor (**2N3904**, T_A = 27°C, T_{DIODE} = 27°C, V_{DD} = 3.3V).*

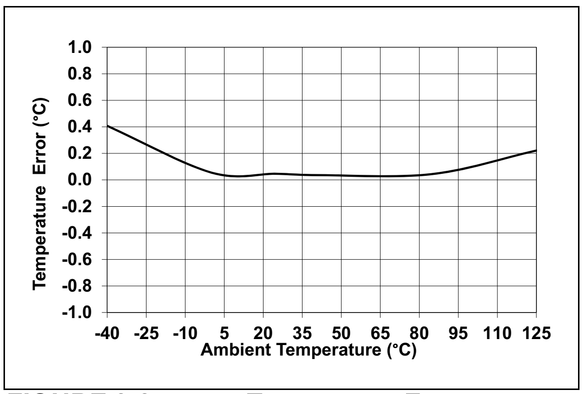


FIGURE 2-2: *Temperature Error vs. Ambient Temperature (2N3904, T_A = 42.5°C, V_{DD} = 3.3V).*

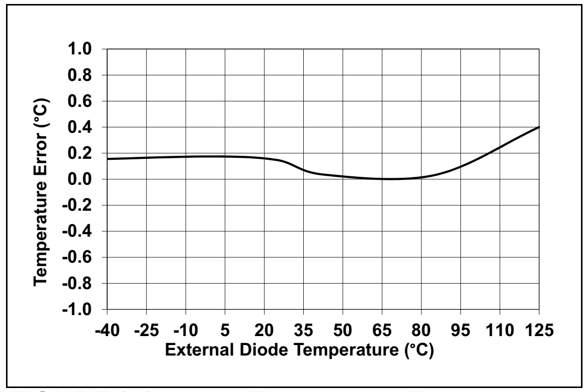


FIGURE 2-3: *Temperature Error vs. External Diode Temperature (**2N3904**, T_{DIODE} = 42.5°C, V_{DD} = 3.3V).*

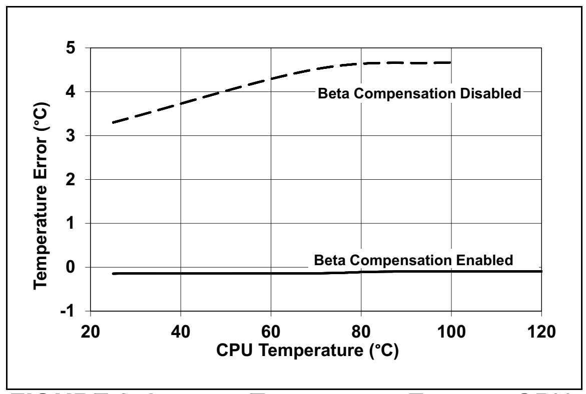


FIGURE 2-4: *Temperature Error vs. CPU Temperature; Typical 65 nm CPU from Major Vendor (T_A = 27°C, V_{DD} = 3.3V, BETA = 011, C_{FILTER} = 470 pF).*

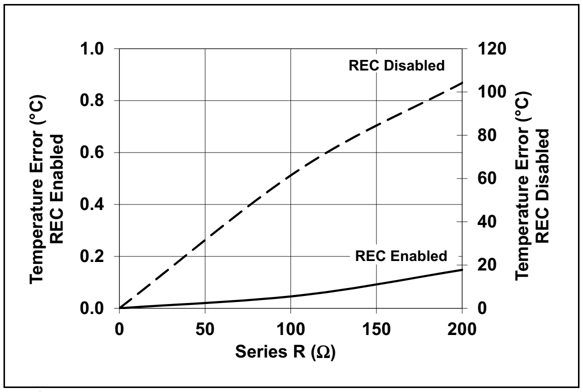


FIGURE 2-5: *Temperature Error vs. Series Resistance.*

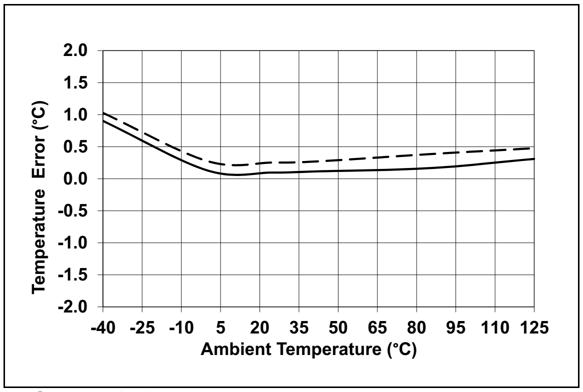


FIGURE 2-6: *Temperature Error vs. Ambient Temperature (**2N3904**, T_A = 27°C, V_{DD} = 3.3V).*

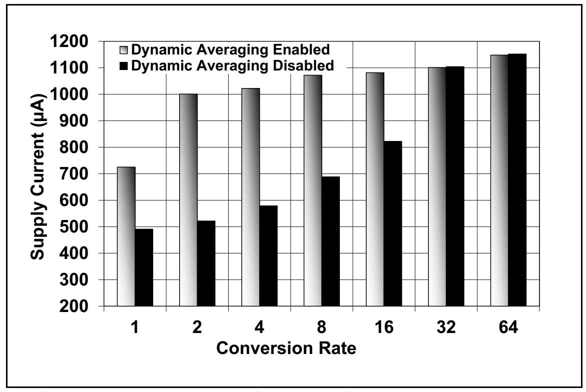


FIGURE 2-7: *Supply Current vs. Conversion Rate.*

3.0 PIN FUNCTION TABLE

The descriptions of the pins are shown in the table below.

TABLE 3-1: PIN FUNCTION TABLE (Note 1)

Pin Number		Pin Name	Pin Type	Description
8-Lead MSOP	8-Lead TDFN			
1	1	V_{DD}	Power	Power Supply
2	2	DP	AIO	External diode positive (anode) connection
3	3	DN	AIO	External diode negative (cathode) connection
4	4	$\overline{\text{THERM}}$/ADDR	OD (5V)	$\overline{\text{THERM}}$ - Critical $\overline{\text{THERM}}$ output signal. Requires pull-up resistor. ADDR - Selects SMBus address based on pull-up resistor
5	5	GND	Power	Ground pin
6	6	$\overline{\text{ALERT}}$	OD (5V)	Active low digital $\overline{\text{ALERT}}$ output signal. Requires pull-up resistor.
7	7	SMDATA	DIOD (5V)	SMBus Data input/output. Requires pull-up resistor.
8	8	SMCLK	DI (5V)	SMBus Clock input. Requires pull-up resistor.
—	9	EP	—	Exposed Thermal Pad. Not internally connected. Grounding is recommended.

Note 1: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$), the voltage difference between V_{DD} and the pull-up voltage must never exceed 3.6V.

3.1 Power Pins (V_{DD} and GND)

These pins are used to supply power to or ground the device.

3.2 Analog Input/Output (AIO) Pins (DP, DN)

These pins are used as inputs/outputs for analog signals.

3.3 Digital Input (DI) Pin (SMCLK)

This pin is used as a digital input. This pin is 5V tolerant (see Note 1).

3.4 Digital Input/Open-Drain Output (DIOD) Pin (SMDATA)

This pin is used as a digital input/output. When used as an output, it is open-drain and requires a pull-up resistor. This pin is 5V tolerant (see Note 1).

3.5 Open-Drain Digital Output (OD) Pins ($\overline{\text{THERM}}$/ADDR, $\overline{\text{ALERT}}$)

These pins are used as digital outputs. They are open-drain pins and require a pull-up resistor. These pins are 5V tolerant (see Note 1).

4.0 PRODUCT DESCRIPTION

The EMC1412 is an SMBus temperature sensor. The EMC1412 monitors one internal diode and one externally connected temperature diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1412 and using that data to control the speed of one or more fans.

The EMC1412 has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures exceeds user programmable limits. This allows the EMC1412 to be used as an independent thermal watchdog to warn the host of temperature hot spots without the direct control of the host. The second level of monitoring provides a non maskable interrupt on the $\overline{\text{THERM}}$ pin if the measured temperatures meet or exceed a second programmable limit.

The figure below shows a system level block diagram of the EMC1412.

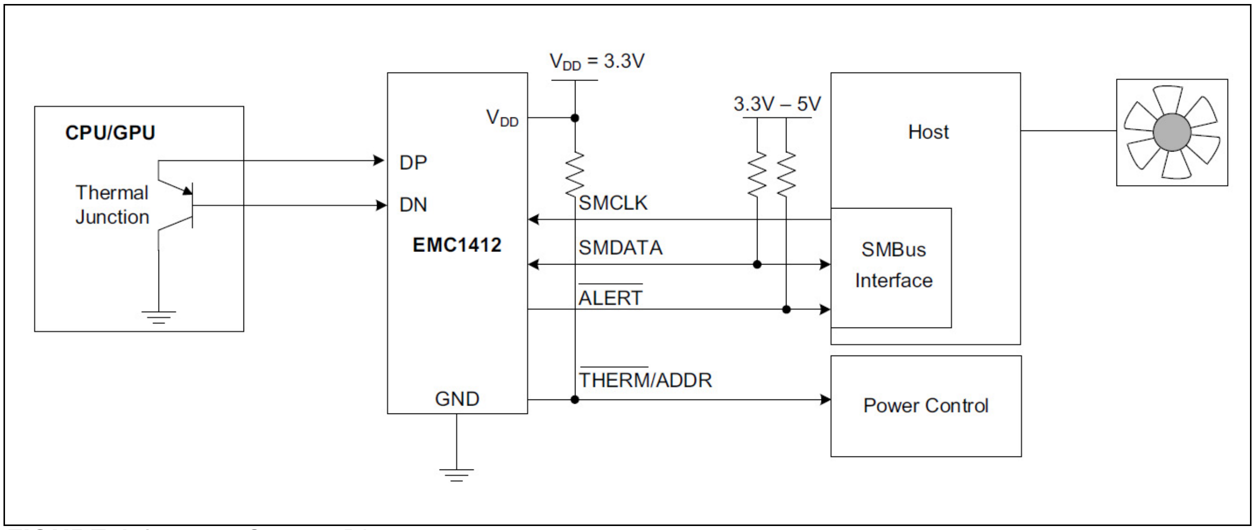


FIGURE 4-1: *System Diagram.*

4.1 Modes of Operation

The EMC1412 have two modes of operation:

- **Active** (Run) - In this mode of operation, the ADC is converting on all temperature channels at the programmed conversion rate. The temperature data is updated at the end of every conversion and the limits are checked. In Active mode, writing to the one-shot register will do nothing.
- **Standby** (Stop) - In this mode of operation, the majority of circuitry is powered down to reduce supply current. The temperature data is not updated and the limits are not checked. In this mode of operation, the SMBus is fully active and the part will return requested data. Writing to the oneshot register will enable the device to update all temperature channels. Once all the channels are updated, the device will return to the Standby mode.

4.1.1 CONVERSION RATES

The EMC1412 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in **Section 6.5 "Conversion Rate Register"** The default conversion rate is four conversions per second.

4.1.2 DYNAMIC AVERAGING

Dynamic averaging causes the EMC1412 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see **Section 6.4 "Configuration Register"**). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate.

The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in the table below.

TABLE 4-1: SUPPLY CURRENT VS. CONVERSION RATE FOR EMC1412

Conversion Rate	Average Supply Current		Averaging Factor (based on 11-bit operation)	
	Enabled (default)	Disabled	Enabled (default)	Disabled
1/16 seconds	660 µA	430 µA	16x	1x
1/8 sec	660 µA	430 µA	16x	1x
1/4 sec	660 µA	430 µA	16x	1x
1/2 sec	660 µA	430 µA	16x	1x
1/sec	660 µA	430 µA	16x	1x
2/sec	930 µA	475 µA	16x	1x
4/sec (default)	950 µA	510 µA	8x	1x
8/sec	1010 µA	630 µA	4x	1x
16/sec	1020 µA	775 µA	2x	1x
32/sec	1050 µA	1050 µA	1x	1x
64/sec	1100 µA	1100 µA	0.5x	0.5x

4.2 THERM Output

The THERM output is asserted independently of the ALERT output and cannot be masked. Whenever any of the measured temperatures exceed the user programmed Therm Limit values for the programmed number of consecutive measurements, the THERM output is asserted. Once it has been asserted, it will remain asserted until all measured temperatures drop below the Therm Limit minus the Therm Hysteresis (also programmable).

When the THERM pin is asserted, the THERM status bits will likewise be set. Reading these bits will not clear them until the THERM pin is deasserted. Once the THERM pin is deasserted, the THERM status bits will be automatically cleared.

4.3 ALERT Output

The ALERT pin is an open drain output and requires a pull-up resistor to V_{DD} and has two modes of operation: interrupt mode and comparator mode. The mode of the ALERT output is selected via the ALERT / COMP bit in the **Section 6.4 "Configuration Register"**.

4.3.1 ALERT PIN INTERRUPT MODE

When configured to operate in interrupt mode, the ALERT pin asserts low when an out of limit measurement (> high limit or < low limit) is detected on any diode or when a diode fault is detected. The ALERT pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the ALERT pin will remain asserted until the appropriate status bits are cleared.

The ALERT pin can be masked by setting the MASK_ALL bit. Once the ALERT pin has been masked, it will be de-asserted and remain de-asserted until the MASK_ALL bit is cleared by the user. Any interrupt conditions that occur while the ALERT pin is masked will update the Status Register normally. There are also individual channel masks (see **Section 6.10 "Channel Mask Register"**).

The ALERT pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more ALERT outputs can be hard-wired together.

4.3.2 ALERT PIN COMPARATOR MODE

When the ALERT pin is configured to operate in comparator mode, it will be asserted if any of the measured temperatures exceeds the respective high limit. The ALERT pin will remain asserted until all temperatures drop below the corresponding high limit minus the Therm Hysteresis value.

When the ALERT pin is asserted in comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the ALERT pin is deasserted. Once the ALERT pin is deasserted, the status bits will be automatically cleared.

The MASK_ALL bit will not block the ALERT pin in this mode; however, the individual channel masks (see **Section 6.10 "Channel Mask Register"**) will prevent the respective channel from asserting the ALERT pin.

4.4 Temperature Measurement

The EMC1412 can monitor the temperature of one externally connected diode. The external diode channel is configured with Resistance Error Correction and Beta Compensation based on user settings and system requirements.

The device contains programmable High, Low, and Therm limits for all measured temperature channels. If the measured temperature goes below the Low limit or above the High limit, the ALERT pin can be asserted (based on user settings). If the measured temperature meets or exceeds the Therm Limit, the THERM pin is asserted unconditionally, providing two tiers of temperature detection.

4.4.1 BETA COMPENSATION

The EMC1412 is configured to monitor the temperature of basic diodes (e.g., 2N3904) or CPU thermal diodes. It automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

4.4.2 RESISTANCE ERROR CORRECTION (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1412 automatically corrects up to 100 ohms of series resistance.

4.4.3 PROGRAMMABLE EXTERNAL DIODE IDEALITY FACTOR

The EMC1412 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement which must be corrected for. This correction is typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the EMC1412 provides a 6-bit register for each external diode where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

Note:	When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

4.5 Diode Faults

The EMC1412 detects an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT pin asserts (unless masked, see **Section 6.11 "Consecutive ALERT Register"** and the temperature data reads 00h in the MSB and LSB registers (note: the low limit will not be checked). A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP, or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the ALERT pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000°C (-64°C in extended range) resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal, with no alerts.

4.6 Consecutive Alerts

The EMC1412 contain multiple consecutive alert counters. One set of counters applies to the ALERT pin and the second set of counters applies to the THERM pin. Each temperature measurement channel has a separate consecutive alert counter for each of the ALERT and THERM pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

See **Section 6.11 "Consecutive ALERT Register"** for more details on the consecutive alert function.

4.7 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled (default) (see **Section 6.14 "Filter Control Register"**). The typical filter performance is shown in the figures below.

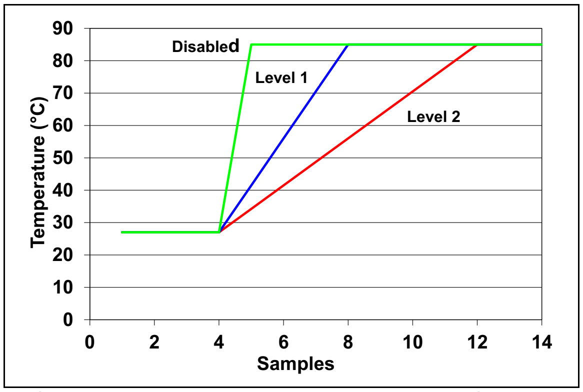


FIGURE 4-2: *Temperature Filter Step Response.*

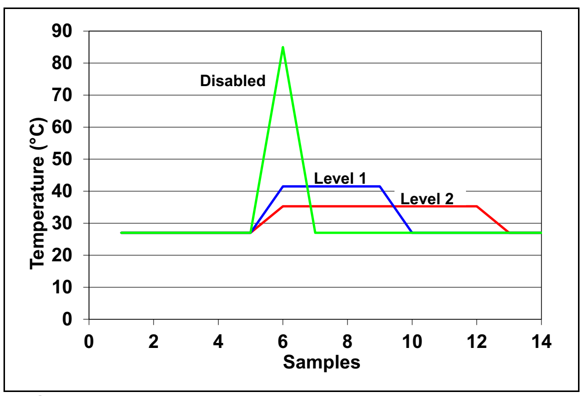


FIGURE 4-3: *Temperature Filter Impulse Response.*

4.8 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1412 has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

The table below shows the default and extended range formats.

TABLE 4-2: TEMPERATURE DATA FORMAT

Temperature (°C)	Default Range (0°C to +127°C)	Extended Range (-64°C to +191°C)
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 (**Note 2**)
-1	000 0000 0000	001 1111 1000
0	000 0000 0000 (**Note 1**)	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 (**Note 3**)	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
≥ 191.875	011 1111 1111	111 1111 1111 (**Note 4**)

Note 1: For default range, all temperatures < 0°C will be reported as 0°C.

2: For extended range, all temperatures < -64°C will be reported as -64°C.

3: For default range, all temperatures > +127.875°C will be reported as +127.875°C.

4: For extended range, all temperatures > +191.875°C will be reported as +191.875°C.

4.9 External Diode Connections

The EMC1412 can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode, or an AMD processor diode. The diodes can be connected as indicated in Figure 4-4.

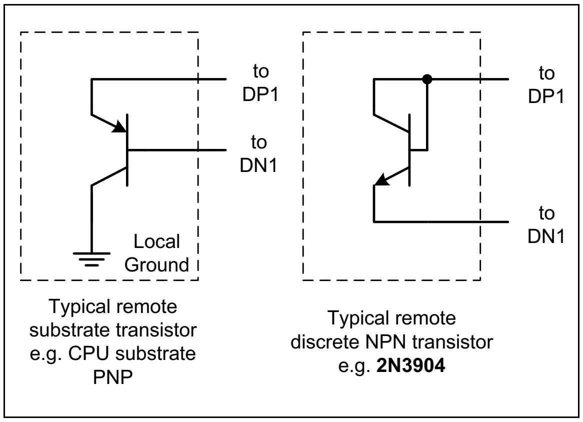


FIGURE 4-4: *Diode Configuration.*

NOTES:

5.0 SYSTEM MANAGEMENT BUS INTERFACE PROTOCOL

5.1 Communications Protocol

The EMC1412 communicates with a host controller, such as a Microchip embedded controller, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in the figure below.

For the first 15 ms after power-up the device may not respond to SMBus communications.

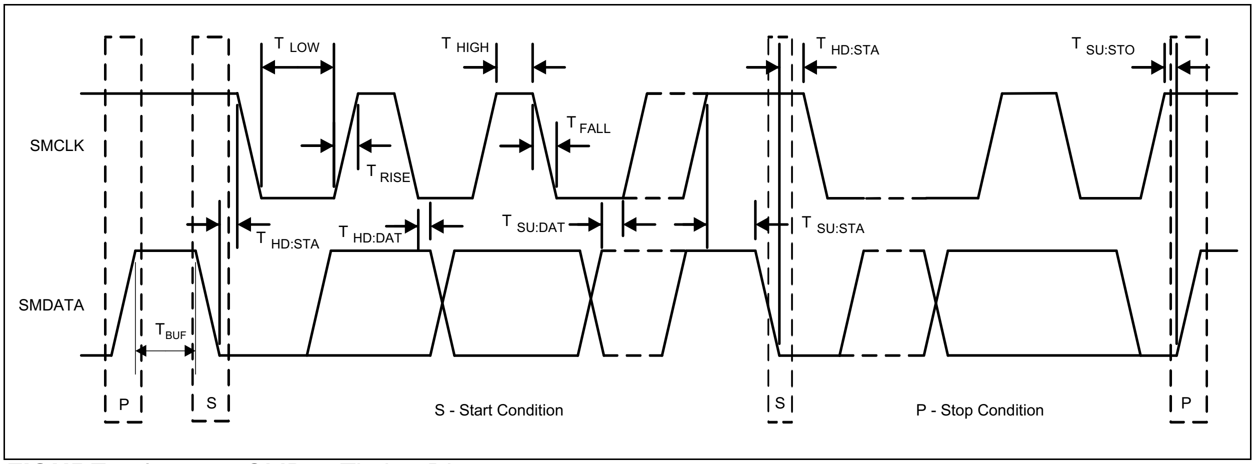


FIGURE 5-1: *SMBus Timing Diagram.*

5.2 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

5.3 SMBus Address and RD/$\overline{\text{WR}}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD / $\overline{\text{WR}}$ indicator bit. If this RD / $\overline{\text{WR}}$ bit is a logic ‘0’, the SMBus Host is writing data to the client device. If this RD / $\overline{\text{WR}}$ bit is a logic ‘1’, the SMBus Host is reading data from the client device.

The EMC1412-A SMBus slave address is determined by the pull-up resistor on the $\overline{\text{THERM}}$ pin as shown in the table below.

The Address decode is performed by pulling known currents from V_{DD} through the external resistor causing the pin voltage to drop based on the respective current / resistor relationship. This pin voltage is compared against a threshold that determines the value of the pull-up resistor.

TABLE 5-1: SMBUS ADDRESS DECODE

Pull-Up Resistor on THERM Pin (±5%)	SMBus Address
4.7 kΩ	1111_100(r/$\overline{\text{w}}$)b
6.8 kΩ	1011_100(r/$\overline{\text{w}}$)b
10 kΩ	1001_100(r/$\overline{\text{w}}$)b
15 kΩ	1101_100(r/$\overline{\text{w}}$)b
22 kΩ	0011_100(r/$\overline{\text{w}}$)b
33 kΩ	0111_100(r/$\overline{\text{w}}$)b

Note 1: The EMC1412-1 SMBus address is hardcoded to 1001_100(r/$\overline{\text{w}}$).

2: The EMC1412-2 SMBus address is hardcoded to 1001_101(r/$\overline{\text{w}}$).

5.4 $\overline{\text{THERM}}$ Pin Considerations

Because of the decode method used to determine the SMBus Address, it is important that the pull-up resistance on the $\overline{\text{THERM}}$ pin be within the tolerances shown in the table above. Additionally, the pull-up resistor on the $\overline{\text{THERM}}$ pin must be connected to the same 3.3V supply that drives the V_{DD} pin.

For 15 ms after power up, the $\overline{\text{THERM}}$ pin must not be pulled low or the SMBus address will not be decoded properly. If the system requirements do not permit these conditions, the $\overline{\text{THERM}}$ pin must be isolated from its hard-wired OR’d bus during this time.

One method of isolating this pin is shown in Figure 5-2.

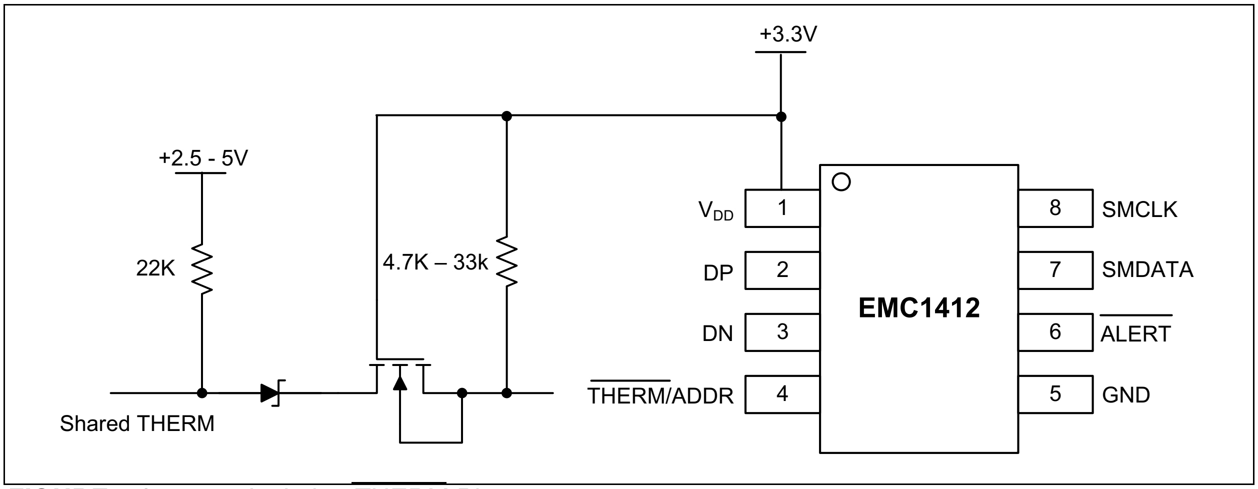


FIGURE 5-2: *Isolating THERM Pin.*

5.5 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

5.6 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8th bit of each byte that is transmitted. This applies to the Write Byte protocol.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent.

5.7 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the device detects an SMBus Stop bit and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

5.8 SMBus Timeout

The EMC1412 supports SMBus Timeout. If the clock line is held low for longer than 30 ms, the device will reset its SMBus protocol. This function can be enabled by setting the TIMEOUT bit in the Consecutive Alert Register (see **Section 4.6 "Consecutive Alerts"**).

5.9 SMBus and I2C Compatibility

The EMC1412 is compatible with SMBus and I2C. The major differences between SMBus and I2C devices are highlighted here. For more information, refer to the SMBus 2.0 and I2C specifications. For information on using the EMC1412 in an I2C system, refer to AN 14.0 Dedicated Slave Devices in I2C Systems.

1. EMC1412 supports I2C fast mode at 400kHz. This covers the SMBus max time of 100kHz.
2. Minimum frequency for SMBus communications is 10kHz.
3. The SMBus client protocol will reset if the clock is held at a logic '0' for longer than 30ms. This timeout functionality is disabled by default in the EMC1412 and can be enabled by writing to the TIMEOUT bit. I2C does not have a timeout.
4. I2C devices do not support the Alert Response Address functionality (which is optional for SMBus).

Attempting to communicate with the EMC1412 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

5.10 SMBus Protocols

The device supports Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below. All of the below protocols use the convention in the table below.

TABLE 5-2: PROTOCOL FORMAT

Data Sent to Device	Data Sent to the Host
# of bits sent	# of bits sent

5.10.1 WRITE BYTE

The Write Byte is used to write one byte of data to the registers, as shown in Table 5-3.

TABLE 5-3: WRITE BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

5.10.2 READ BYTE

The Read Byte protocol is used to read one byte of data from the registers as shown in the table below.

TABLE 5-4: READ BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XX	1	0 → 1

5.10.3 SEND BYTE

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in the table below.

TABLE 5-5: SEND BYTE PROTOCOL

START	Slave Address	WR	ACK	Register Address	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	0 →1

5.10.4 RECEIVE BYTE

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in the table below.

TABLE 5-6: RECEIVE BYTE PROTOCOL

START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 →0	YYYY_YYY	1	0	XXh	1	0 → 1

5.11 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in the table below.

TABLE 5-7: ALERT RESPONSE ADDRESS PROTOCOL

START	Alert Response Address	RD	ACK	Device Address	NACK	STOP
1 → 0	0001_100	1	0	YYYY_YYY	1	0 → 1

The EMC1412 will respond to the ARA in the following way:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

Note:	The ARA does not clear the Status Register and if the MASK bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

6.0 REGISTER DESCRIPTION

The registers shown in the table below are accessible through the SMBus. An entry of “-” indicates that the bit is not used and will always read ‘0’.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	R/W	Register Name	Function	Default Value
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode.	00h
01h	R	External Diode Data High Byte	Stores the integer data for External Diode.	00h
02h	R/C	Status	Stores the status bits for the Internal Diode and External Diodes.	00h
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h).	00h
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah).	06h (4/sec)
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh).	55h (+85°C)
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch).	00h (0°C)
07h	R/W	External Diode High Limit High Byte	Stores the integer portion of the high limit for External Diode (mirrored at register 0Dh).	55h (+85°C)
08h	R/W	External Diode Low Limit High Byte	Stores the integer portion of the low limit for External Diode (mirrored at register 0Eh).	00h (0°C)
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h).	00h
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h).	06h (4/sec)
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h).	55h (+85°C)
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h).	00h (0°C)
0Dh	R/W	External Diode High Limit High Byte	Stores the integer portion of the high limit for External Diode (mirrored at register 07h).	55h (+85°C)
0Eh	R/W	External Diode Low Limit High Byte	Stores the integer portion of the low limit for External Diode (mirrored at register 08h).	00h (0°C)
0Fh	W	One-Shot	A write to this register initiates a one-shot update.	00h
10h	R	External Diode Data Low Byte	Stores the fractional data for External Diode.	00h
11h	R/W	Scratchpad	Scratchpad register for software compatibility.	00h
12h	R/W	Scratchpad	Scratchpad register for software compatibility.	00h
13h	R/W	External Diode High Limit Low Byte	Stores the fractional portion of the high limit for External Diode.	00h
14h	R/W	External Diode Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode.	00h
19h	R/W	External Diode Therm Limit	Stores the 8-bit critical temperature limit for External Diode.	55h (+85°C)
1Fh	R/W	Channel Mask Register	Controls the masking of individual channels.	00h
20h	R/W	Internal Diode Therm Limit	Stores the 8-bit critical temperature limit for the Internal Diode.	55h (+85°C)

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	R/W	Register Name	Function	Default Value
21h	R/W	Therm Hysteresis	Stores the 8-bit hysteresis value that applies to all Therm limits.	0Ah (10°C)
22h	R/W	Consecutive ALERT	Controls the number of out-of-limit conditions that must occur before an interrupt is asserted.	70h
25h	R/W	External Diode Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode.	08h
27h	R/W	External Diode Ideality Factor	Stores the ideality factor for External Diode.	12h (1.008)
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode.	00h
40h	R/W	Filter Control	Controls the digital filter setting for the External Diode channel.	00h
FDh	R	Product ID (DSTEMP)	Stores a fixed value that identifies the device.	21h
FEh	R	Manufacturer ID	Stores a fixed value that represents Microchip.	5Dh
FFh	R	Revision	Stores a fixed value that represents the revision number.	04h

6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal “shadow” register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

6.2 Temperature Data Registers

As shown in the table below, all temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits.

TABLE 6-2: TEMPERATURE DATA REGISTERS

ADDR	R/W	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
00h	R	Internal Diode High Byte	128	64	32	16	8	4	2	1	00h
29h	R	Internal Diode Low Byte	0.5	0.25	0.125	—	—	—	—	—	00h
01h	R	External Diode High Byte	128	64	32	16	8	4	2	1	00h
10h	R	External Diode Low Byte	0.5	0.25	0.125	—	—	—	—	—	00h

6.3 Status Register

Name	Bits	Address	Type	Default
Status	8	02h	RC	00h

The Status Register reports the operating status of the Internal Diode and External Diode channels. When any of the bits are set (excluding the BUSY bit) either the ALERT or THERM pin is being asserted.

The ALERT and THERM pins are controlled by the respective consecutive alert counters (see **Section 6.11 "Consecutive ALERT Register"**) and will not be asserted until the programmed consecutive alert count has been reached. The status bits (except E1THERM and ITHERM) will remain set until read unless the ALERT pin is configured as a second THERM output (see **Section 4.3.2 "ALERT Pin Comparator Mode"**).

REGISTER 6-1: STATUS REGISTER (ADDRESS 02H)

RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0
BUSY	IHIGH	ILOW	EHIGH	ELOW	FAULT	ETHERM	ITHERM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
RC = Read-then-clear bit			

bit 7 **BUSY:** This bit indicates that the ADC is currently converting. This bit does not cause either the ALERT or THERM pins to be asserted.

bit 6 **IHIGH:** This bit is set when the Internal Diode channel exceeds its programmed high limit. When set, this bit will assert the ALERT pin.

bit 5 **ILOW:** This bit is set when the Internal Diode channel drops below its programmed low limit. When set, this bit will assert the ALERT pin.

bit 4 **EHIGH**: This bit is set when the External Diode channel exceeds its programmed high limit. When set, this bit will assert the ALERT pin.

bit 3 **ELOW**: This bit is set when the External Diode channel drops below its programmed low limit. When set, this bit will assert the ALERT pin.

bit 2 **FAULT**: This bit is asserted when a diode fault is detected. When set, this bit will assert the ALERT pin.

bit 1 **ETHERM**: This bit is set when the External Diode channel exceeds the programmed Therm Limit. When set, this bit will assert the THERM pin. This bit will remain set until the THERM pin is released at which point it will be automatically cleared.

bit 0 **ITHERM**: This bit is set when the Internal Diode channel exceeds the programmed Therm Limit. When set, this bit will assert the THERM pin. This bit will remain set until the THERM pin is released at which point it will be automatically cleared.

6.4 Configuration Register

Name	Bits	Address	Type	Default
Configuration	8	03h	R/W	00h
		09h		

The Configuration Register controls the basic operation of the device. This register is fully accessible at addresses 03h and 09h.

REGISTER 6-2: CONFIGURATION REGISTER (ADDRESSES 03H AND 09H)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
MASK_ALL	RUN/STOP	ALERT/COMP	RECD	—	RANGE	DAVG_DIS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MASK_ALL:** Masks the ALERT from asserting.
- 1 = The ALERT pin is not masked. If any of the appropriate status bits are set the ALERT pin will be asserted.
- 0 = The ALERT pin is masked. It will not be asserted for any interrupt condition unless it is configured in comparator mode. The Status Register will be updated normally. This is the default setting.

bit 6 **RUN/STOP:** Controls Active/Standby modes.
- 1 = The device is in Standby mode and not converting.
- 0 = The device is in Active mode and converting on all channels. This is the default setting.

bit 5 **ALERT/COMP:** Controls the operation of the ALERT pin.
- 1 = The ALERT pin acts in comparator mode as described in **Section 4.3.2 "ALERT Pin Comparator Mode"**. In this mode the MASK_ALL bit is ignored.
- 0 = The ALERT pin acts as described in **Section 4.3 "ALERT Output"**. This is the default setting.

bit 4 **RECD1:** Disables the Resistance Error Correction (REC) for External Diode 1.
- 1 = REC is disabled for External Diode 1.
- 0 = REC is enabled for External Diode 1. This is the default setting.

bit 3 **Unimplemented:** read as '0'

bit 2 **RANGE:** Configures the measurement range and data format of the temperature channels.
- 1 = The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see **Table 4-2**).
- 0 = The temperature measurement range is 0°C to +127.875°C and the data format is binary. This is the default setting.

bit 1 **DAVG_DIS:** Disables the dynamic averaging feature on all temperature channels.
- 1 = The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced as shown in **Table 4-1**.
- 0 = The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in **Table 4-1**. This is the default setting.

bit 0 **Unimplemented:** read as '0'

6.5 Conversion Rate Register

Name	Bits	Address	Type	Default
Conversion Rate	8	04h 04Ah	R/W	06h (4/sec)

The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

REGISTER 6-3: CONVERSION RATE REGISTER (ADDRESSES 04H AND 0AH)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CONV[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: read as '0'.

bit 3-0 **CONV[3:0]:** Determines the conversion rate.

0000 = 1/16 conversions per second
0001 = 1/8 conversions per second
0010 = 1/4 conversions per second
0011 = 1/2 conversions per second
0100 = one conversion per second
0101 = two conversions per second
0110 = four conversions per second (default)
0111 = eight conversions per second
1000 = 16 conversions per second
1001 = 32 conversions per second
1010 = 64 conversions per second
All other configurations set the device to one conversion per second.

6.6 Limit Registers

The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the ALERT pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the ALERT pin is asserted.

The data format for the limits must match the selected data format for the temperature so that if the extended temperature range is used, the limits must be programmed in the extended data format.

The limit registers with multiple addresses are fully accessible at either address.

When the device is in Standby mode, updating the limit registers will have no effect until the next conversion cycle occurs. This can be initiated via a write to the One-Shot Register or by clearing the RUN/STOP bit in the Configuration Register (see **Section 6.4 "Configuration Register"**).

TABLE 6-3: TEMPERATURE LIMIT REGISTERS

Addr.	R/W	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
05h 0Bh	R/W	Internal Diode High Limit	128	64	32	16	8	4	2	1	55h (+85°C)
06h 0Ch	R/W	Internal Diode Low Limit	128	64	32	16	8	4	2	1	00h (0°C)
07h 0Dh	R/W	External Diode High Limit High Byte	128	64	32	16	8	4	2	1	55h (+85°C)
13h	R/W	External Diode High Limit Low Byte	0.5	0.25	0.125	—	—	—	—	—	00h
08h 0Eh	R/W	External Diode Low Limit High Byte	128	64	32	16	8	4	2	1	00h (0°C)
14h	R/W	External Diode Low Limit Low Byte	0.5	0.25	0.125	—	—	—	—	—	00h

6.7 Scratchpad Registers

The Scratchpad Registers are Read/Write registers that are used for place holders to be software compatible with legacy programs. Reading from the registers will return what is written to them.

TABLE 6-4: SCRATCHPAD REGISTERS

Addr.	R/W	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
11h	R/W	Scratchpad	7	6	5	4	3	2	1	0	00h
12h	R/W	Scratchpad	7	6	5	4	3	2	1	0	00h

6.8 One-Shot Register

The One-Shot Register is used to initiate a one-shot command. Writing to the one-shot register when the device is in Standby mode and the BUSY bit in the Status Register is ‘0’ will immediately cause the ADC to update all temperature measurements. Writing to the One-Shot Register while the device is in Active mode will have no effect.

REGISTER 6-4: ONE-SHOT REGISTER (ADDRESS 0FH)

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
ONE_SHOT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **ONE_SHOT[7:0]:** Writing to this register initiates a single conversion cycle. Data is not stored and always reads 00h.

6.9 Therm Limit Registers

The Therm Limit Registers are used to determine whether a critical thermal event has occurred. If the measured temperature exceeds the Therm Limit, the $\overline{\text{THERM}}$ pin is asserted. The limit setting must match the chosen data format of the temperature reading registers.

Unlike the $\overline{\text{ALERT}}$ pin, the $\overline{\text{THERM}}$ pin cannot be masked. Additionally, the $\overline{\text{THERM}}$ pin will be released once the temperature drops below the corresponding threshold minus the Therm Hysteresis.

TABLE 6-5: THERM LIMIT REGISTERS

Addr.	R/W	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
19h	R/W	External Diode Therm Limit	128	64	32	16	8	4	2	1	55h (+85°C)
20h	R/W	Internal Diode Therm Limit	128	64	32	16	8	4	2	1	55h (+85°C)
21h	R/W	Therm Hysteresis	128	64	32	16	8	4	2	1	0Ah (10°C)

6.10 Channel Mask Register

The Channel Mask Register controls individual channel masking. When a channel is masked, the $\overline{\text{ALERT}}$ pin will not be asserted when the masked channel reads a diode fault or out-of-limit error. The channel mask does not mask the $\overline{\text{THERM}}$ pin.

REGISTER 6-5: CHANNEL MASK REGISTER (ADDRESS 1FH)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	EMASK	INTMASK
bit 7							bit 0

Legend:

REGISTER 6-5: CHANNEL MASK REGISTER (ADDRESS 1FH) (CONTINUED)

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 Unimplemented bits always read as ‘0’.

bit 1 **EMASK:** Masks the ALERT pin from asserting when the External Diode channel is out-of-limit or reports a diode fault.
- 1 = The External Diode channel will not cause the ALERT pin to be asserted if it is out-of-limit or reports a diode fault.
- 0 = The External Diode channel will cause the ALERT pin to be asserted if it is out-of-limit or reports a diode fault. This is the default setting.

bit 0 **INTMASK:** Masks the ALERT pin from asserting when the Internal Diode temperature is out-of-limit.
- 1 = The Internal Diode channel will not cause the ALERT pin to be asserted if it is out-of-limit.
- 0 = The Internal Diode channel will cause the ALERT pin to be asserted if it is out-of-limit. This is the default setting.

6.11 Consecutive ALERT Register

Name	Bits	Address	Type	Default
Consecutive ALERT	8	22h	R/W	70h

The Consecutive ALERT register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the ALERT or THERM pin is asserted. Additionally, the Consecutive ALERT register controls the SMBus Timeout functionality.

An out-of-limit condition (i.e. HIGH, LOW, or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if no out-of-limit condition or diode fault condition occurs in a consecutive reading.

When the ALERT pin is configured as an interrupt and when the consecutive alert counter reaches its programmed value, the following will occur: the STATUS bit(s) for that channel and the last error condition(s) (i.e. EHIGH) will be set to ‘1’, the ALERT pin will be asserted, the consecutive alert counter will be cleared and measurements will continue. When the ALERT pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature exceeds the High Limit. Additionally, once the consecutive alert counter reaches the programmed limit, the ALERT pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the Therm Hysteresis value.

For example, if the CALRT<2:0> bits are set for 4 consecutive alerts on an EMC1412 device, the high limits are set at +70°C and none of the channels are masked, then the ALERT pin will be asserted after the following five measurements:

- Internal Diode reads +71°C and the external diode reads +69°C. Consecutive alert counter for INT is incremented to 1.
- Both the Internal Diode and the External Diode read +71°C. Consecutive alert counter for INT is incremented to 2 and for EXT is set to 1.
- The External Diode reads +71°C and the Internal Diode reads +69°C. Consecutive alert counter for INT is cleared and EXT is incremented to 2.
- The Internal Diode reads +71°C and the external diode reads +71°C. Consecutive alert counter for INT is set to 1 and EXT is incremented to 3.
- The Internal Diode reads +71°C and the external diode reads +71°C. Consecutive alert counter for INT is incremented to 2 and EXT is incremented to 4. The appropriate status bits are set for EXT and the ALERT pin is asserted. EXT counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

REGISTER 6-6: CONSECUTIVE ALERT REGISTER (ADDRESS 22H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
TIMEOUT	CTHRM[6:4]			CALRT[3:1]			—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **TIMEOUT:** Determines whether the SMBus Timeout function is enabled.

1 = The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30 ms, the device will reset the SMBus protocol.

0 = The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol. This is the default setting.

bit 6-4 **CTHRM[6:4]:** Determines the number of consecutive measurements that must exceed the corresponding Therm Limit before the $\overline{\text{THERM}}$ pin is asserted. All temperature channels use this value to set the respective counters. The consecutive Therm counter is incremented whenever any measurement exceed the corresponding Therm Limit.

If the temperature drops below the Therm Limit, the counter is reset. If a number of consecutive measurements above the Therm Limit occur, the $\overline{\text{THERM}}$ pin is asserted low.

Once the $\overline{\text{THERM}}$ pin has been asserted, the consecutive therm counter will not reset until the corresponding temperature drops below the Therm Limit minus the Therm Hysteresis value.

000 = The $\overline{\text{THERM}}$ pin will be asserted after one out-of-limit measurement.

001 = The $\overline{\text{THERM}}$ pin will be asserted after two consecutive out-of-limit measurements.

011 = The $\overline{\text{THERM}}$ pin will be asserted after three consecutive out-of-limit measurements.

111 = The $\overline{\text{THERM}}$ pin will be asserted after four consecutive out-of-limit measurements. This is the default setting.

bit 3-1 **CALRT[3:1]:** Determines the number of consecutive measurements that must have an out-of-limit condition or diode fault before the $\overline{\text{ALERT}}$ pin is asserted. All temperature channels use this value to set the respective counters.

000 = The $\overline{\text{ALERT}}$ pin will be asserted after one out-of-limit measurement or diode fault. This is the default setting.

001 = The $\overline{\text{ALERT}}$ pin will be asserted after two consecutive out-of-limit measurements or diode faults.

011 = The $\overline{\text{ALERT}}$ pin will be asserted after three consecutive out-of-limit measurements or diode faults.

111 = The $\overline{\text{ALERT}}$ pin will be asserted after four consecutive out-of-limit measurements or diode faults.

bit 0 Unimplemented bits always read as ‘0’.

6.12 Beta Configuration Register

This register is used to set the Beta Compensation factor that is used for the external diode channel.

Name	Bits	Address	Type	Default
Beta Configuration	8	25h	R/W	08h

REGISTER 6-7: BETA CONFIGURATION REGISTER (ADDRESS 25H)

U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	—	ENABLE	BETA[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 Unimplemented bits always read as ‘0’.

bit 3 **ENABLE1:** Enables or disables the Beta Compensation factor auto-detection function.

1 = The Beta Compensation factor auto-detection circuitry is enabled. At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETA1[2:0] bits will be automatically updated to indicate the current setting.

0 = The Beta Compensation Factor auto-detection circuitry is disabled.

bit 2-0 **BETA[2:0]:** These bits always reflect the current beta configuration settings. If auto-detection circuitry is enabled, these bits will be updated automatically and writing to these bits will have no effect. If the auto-detection circuitry is disabled, these bits will determine the beta configuration setting that is used for their respective channels (**Note 1**).

000 = Indicates a minimum beta compensation factor of 0.11. This is the default configuration.
001 = Indicates a minimum beta compensation factor of 0.18
010 = Indicates a minimum beta compensation factor of 0.25
011 = Indicates a minimum beta compensation factor of 0.33
100 = Indicates a minimum beta compensation factor of 0.43
101 = Indicates a minimum beta compensation factor of 1.00
110 = Indicates a minimum beta compensation factor of 2.33
111 = Disabled

Note 1: Care should be taken when setting the BETA[2:0] bits when the auto-detection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, the circuit may introduce measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as an AMD processor diode), the BETA[2:0] bits should be set to ‘111b’.

6.13 External Diode Ideality Factor Register

This register stores the ideality factors that are applied to the external diodes. Table 6-6 defines each setting and the corresponding ideality factor. Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors; therefore, it is not recommended that these settings be updated without consulting Microchip.

REGISTER 6-8: EXTERNAL DIODE IDEALITY FACTOR REGISTER (ADDRESS 27H)

U-0	U-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
—	—	IDEALITY[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented bits always read as ‘0’.

bit 5-0 **IDEALITY[5:0]:** These bits set the ideality factor for the External Diode channel.
Table 6-6 shows the ideality factor configuration using the diode model for temperature measurement.
Table 6-7 shows the ideality factor configuration under the BJT transistor model.

TABLE 6-6: IDEALITY FACTOR LOOK-UP TABLE (DIODE MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9949	18h	1.0159	28h	1.0371
09h	0.9962	19h	1.0172	29h	1.0384
0Ah	0.9975	1Ah	1.0185	2Ah	1.0397
0Bh	0.9988	1Bh	1.0200	2Bh	1.0410
0Ch	1.0001	1Ch	1.0212	2Ch	1.0423
0Dh	1.0014	1Dh	1.0226	2Dh	1.0436
0Eh	1.0027	1Eh	1.0239	2Eh	1.0449
0Fh	1.0040	1Fh	1.0253	2Fh	1.0462
10h	1.0053	20h	1.0267	30h	1.0475
11h	1.0066	21h	1.0280	31h	1.0488
12h (default)	1.0080	22h	1.0293	32h	1.0501
13h	1.0093	23h	1.0306	33h	1.0514
14h	1.0106	24h	1.0319	34h	1.0527
15h	1.0119	25h	1.0332	35h	1.0540
16h	1.0133	26h	1.0345	36h	1.0553
17h	1.0146	27h	1.0358	37h	1.0566

For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to the table below when using a CPU substrate transistor.

TABLE 6-7: SUBSTRATE DIODE IDEALITY FACTOR LOOK-UP TABLE (BJT MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9869	18h	1.0079	28h	1.0291
09h	0.9882	19h	1.0092	29h	1.0304
0Ah	0.9895	1Ah	1.0105	2Ah	1.0317
0Bh	0.9908	1Bh	1.0120	2Bh	1.0330
0Ch	0.9921	1Ch	1.0132	2Ch	1.0343
0Dh	0.9934	1Dh	1.0146	2Dh	1.0356
0Eh	0.9947	1Eh	1.0159	2Eh	1.0369
0Fh	0.9960	1Fh	1.0173	2Fh	1.0382
10h	0.9973	20h	1.0187	30h	1.0395
11h	0.9986	21h	1.0200	31h	1.0408
12h (default)	1.0000	22h	1.0213	32h	1.0421
13h	1.0013	23h	1.0226	33h	1.0434
14h	1.0026	24h	1.0239	34h	1.0447
15h	1.0039	25h	1.0252	35h	1.0460
16h	1.0053	26h	1.0265	36h	1.0473
17h	1.0066	27h	1.0278	37h	1.0486

Note 1: When measuring a 65 nm Intel CPU, the Ideality Setting should be the default 12h. When measuring a 45 nm Intel CPU, the Ideality Setting should be 15h.

6.14 Filter Control Register

Name	Bits	Address	Type	Default
Filter Configuration	8	40h	R/W	00h

The Filter Configuration Register controls the digital filter on the External Diode channel.

REGISTER 6-9: FILTER CONTROL REGISTER (ADDRESS 40H)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	FILTER[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2 Unimplemented bits always read as ‘0’.

bit 1-0 **FILTER[1:0]:** Controls the level of digital filtering that is applied to the External Diode temperature measurement. See **Figure 4-2** and **Figure 4-3** for examples on the filter behavior.

`00` = Averaging is disabled
`01` = Level 1 Averaging is enabled
`10` = Level 1 Averaging is enabled
`11` = Level 2 Averaging is enabled

6.15 Product ID Register

The Product ID Register holds a unique value that identifies the device.

TABLE 6-8: PRODUCT ID REGISTER

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit2	Bit0	Default
FDh	Product ID	R	0	0	1	0	0	0	0	0	20h

6.16 Manufacturer ID Register

The Manufacturer ID register contains an 8-bit word that identifies Microchip as the manufacturer of the EMC1412.

TABLE 6-9: MANUFACTURER ID REGISTER

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit2	Bit0	Default
FEh	MCHP ID	R	0	1	0	1	1	1	0	1	5Dh

6.17 Revision Register

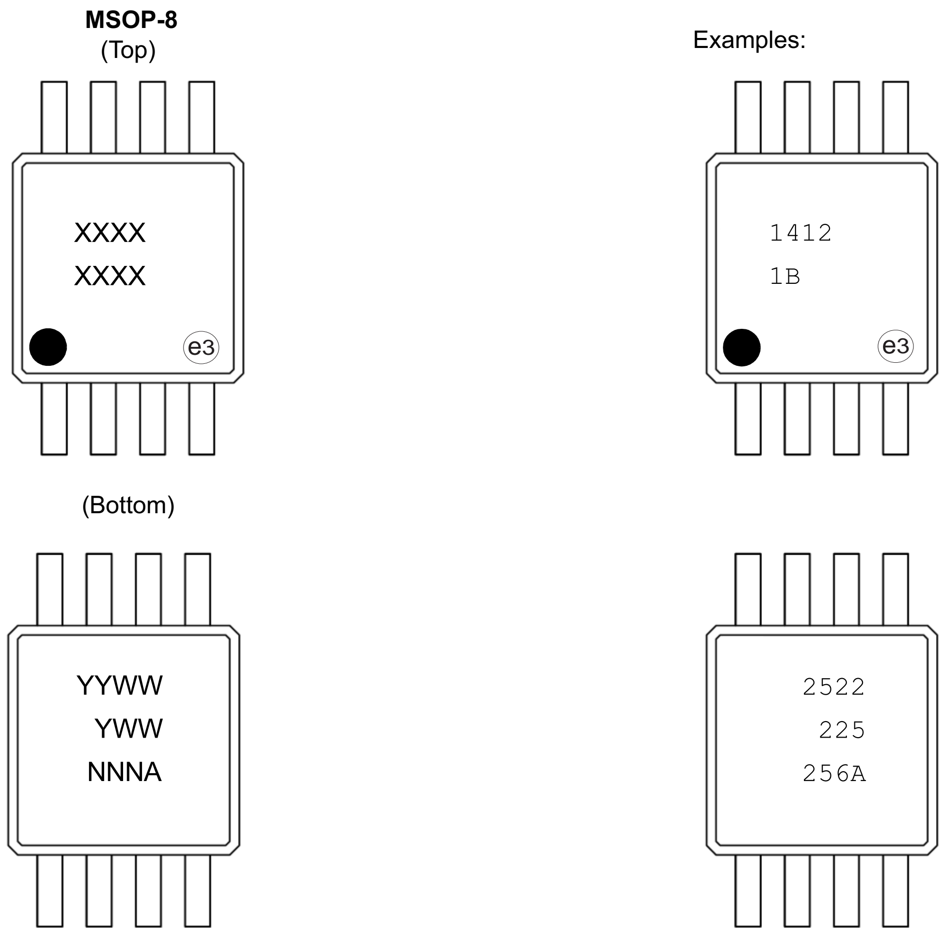
The Revision register contains an 8-bit word that identifies the die revision.

TABLE 6-10: REVISION REGISTER

Register Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit2	Bit0	Default
FFh	Revision	R	0	0	0	0	0	1	0	0	04h

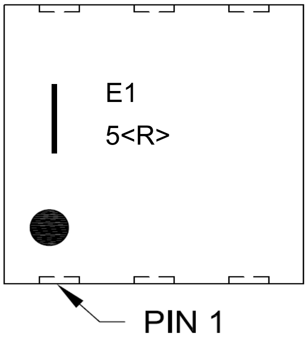
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

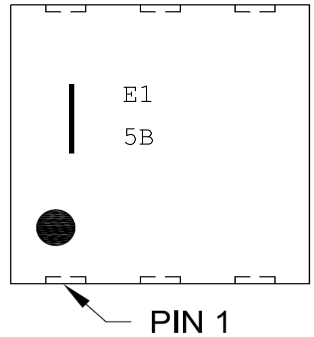


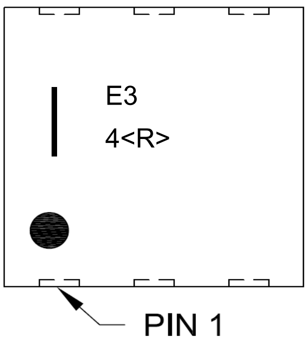
Legend:	XX...X	Device-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

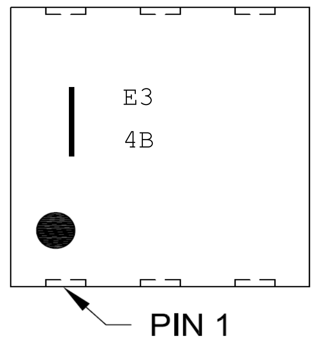
TDFN-8



Example:

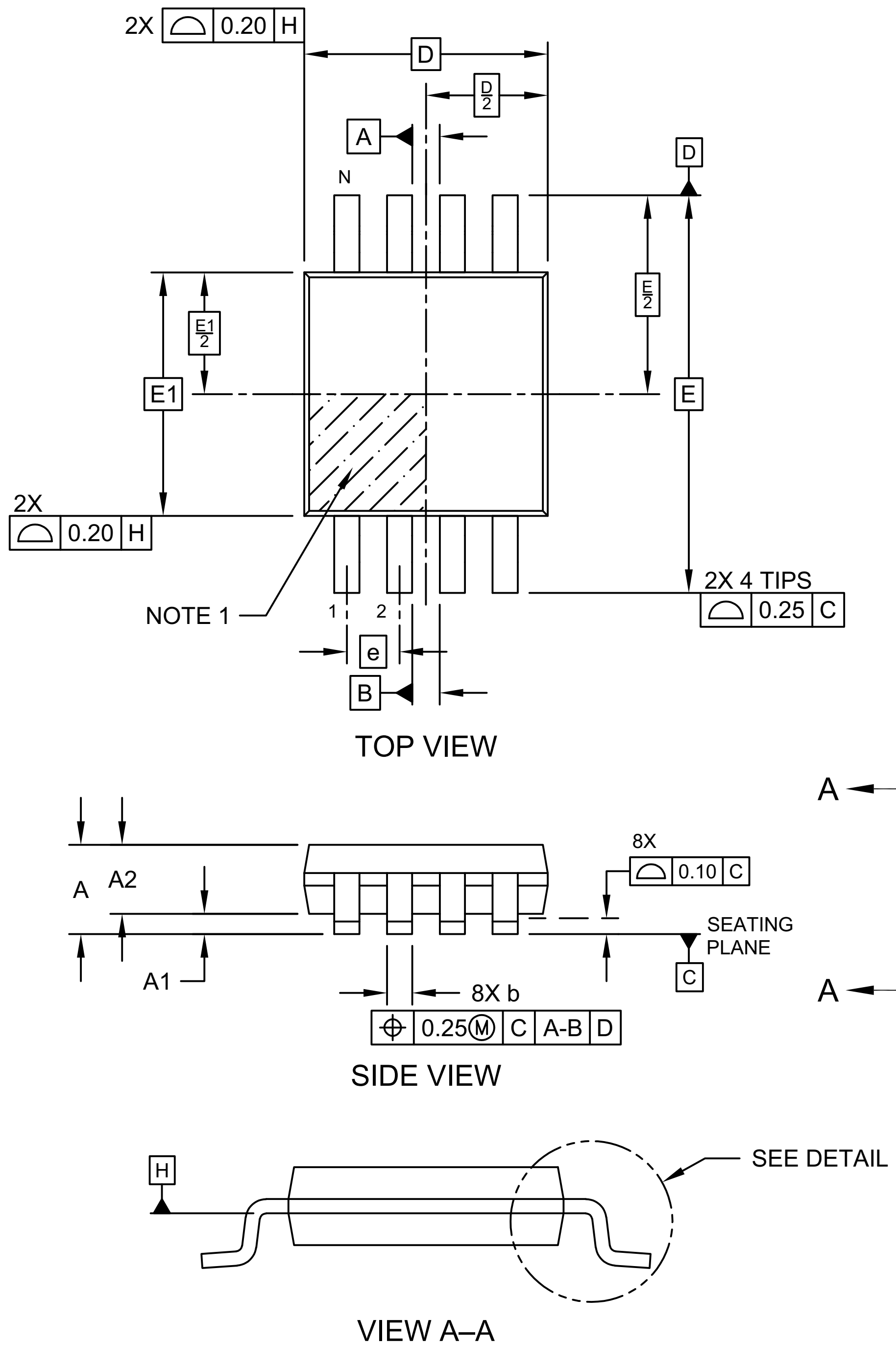






8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

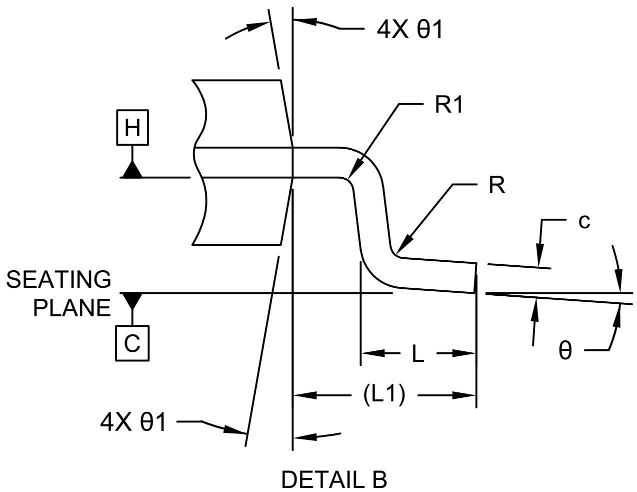
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

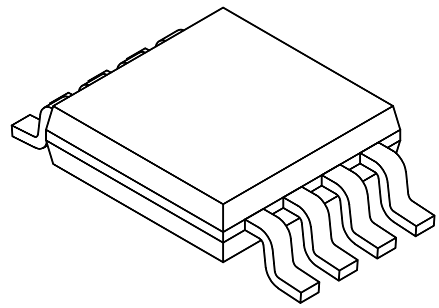


Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D	3.00 BSC		
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

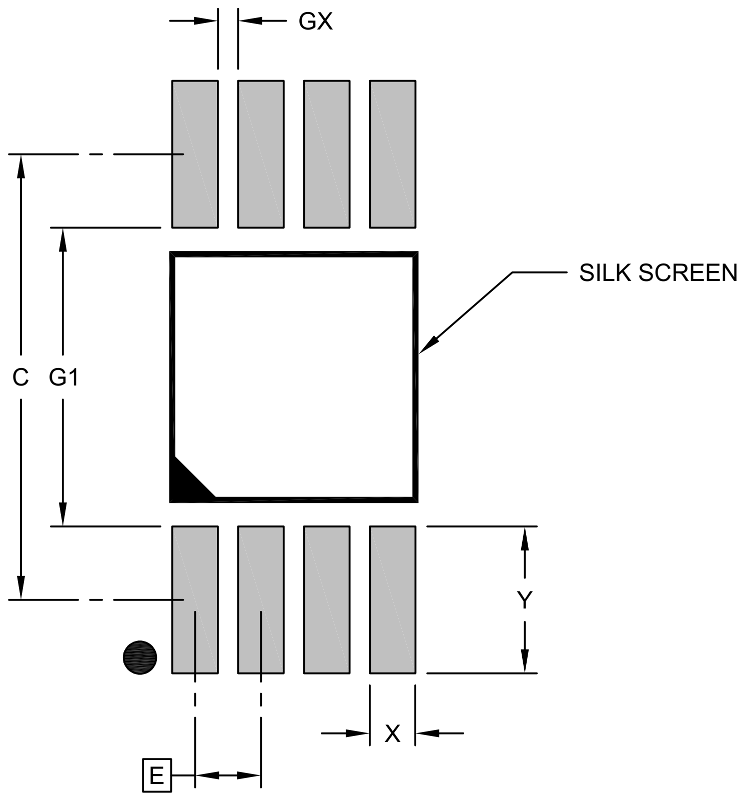
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

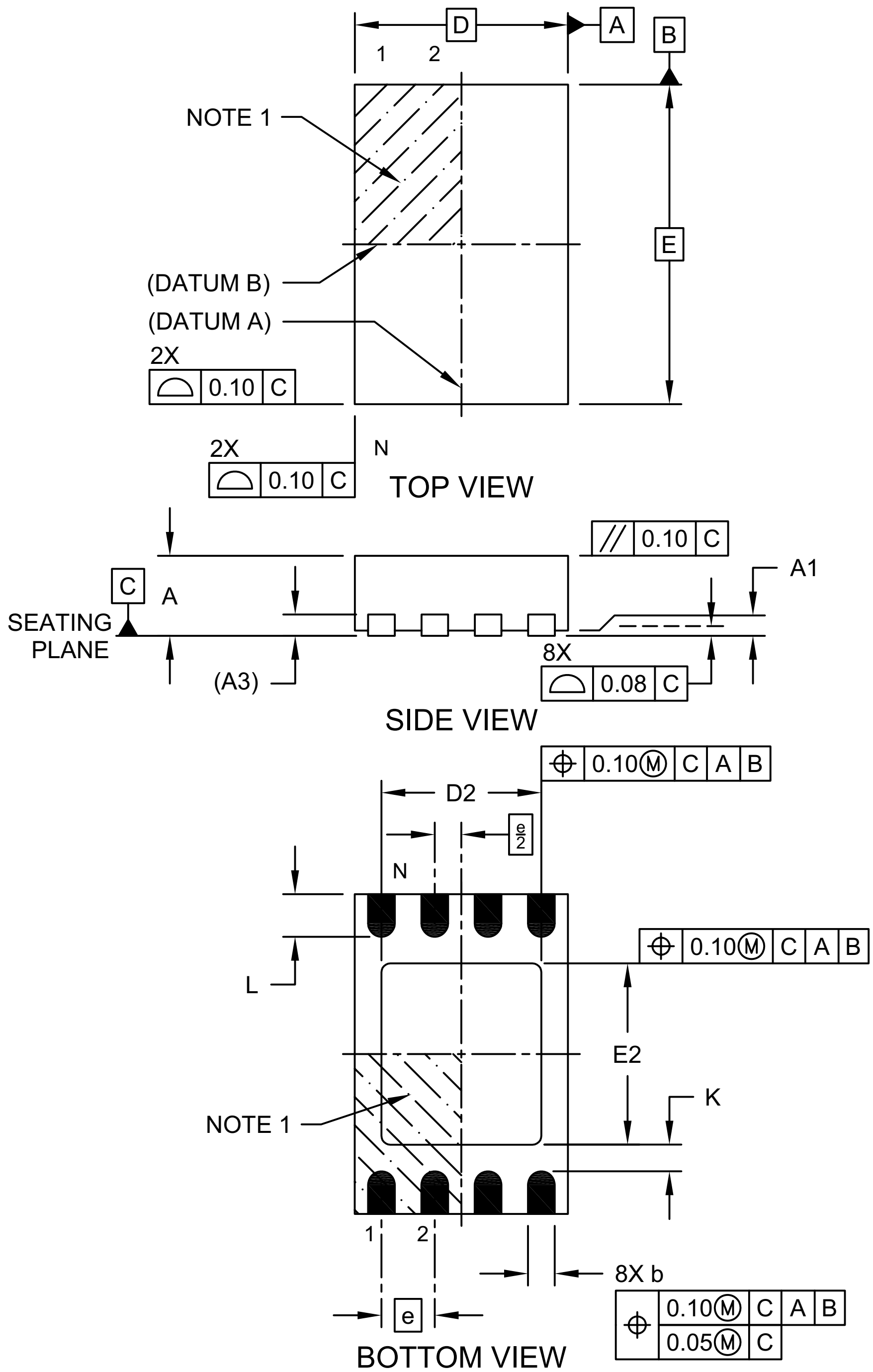
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev F

8-Lead Very Thin Plastic Dual Flat, No Lead Package (8Q) - 2x3 mm Body [VDFN]

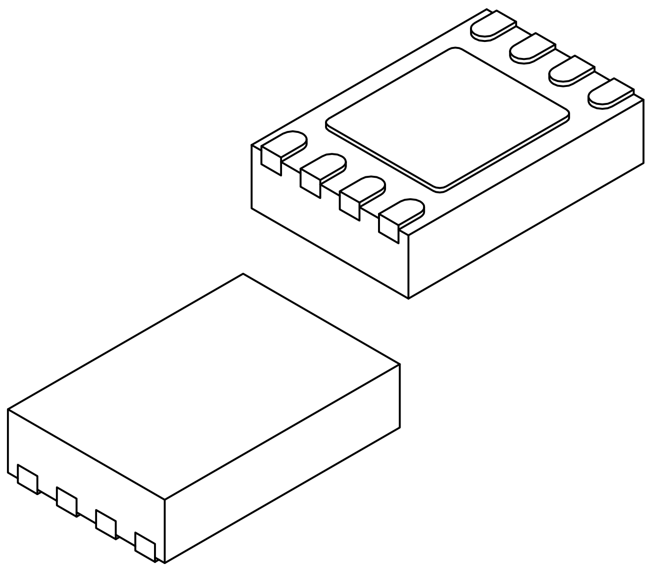
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-382A Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (8Q) - 2x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.60	1.70	1.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

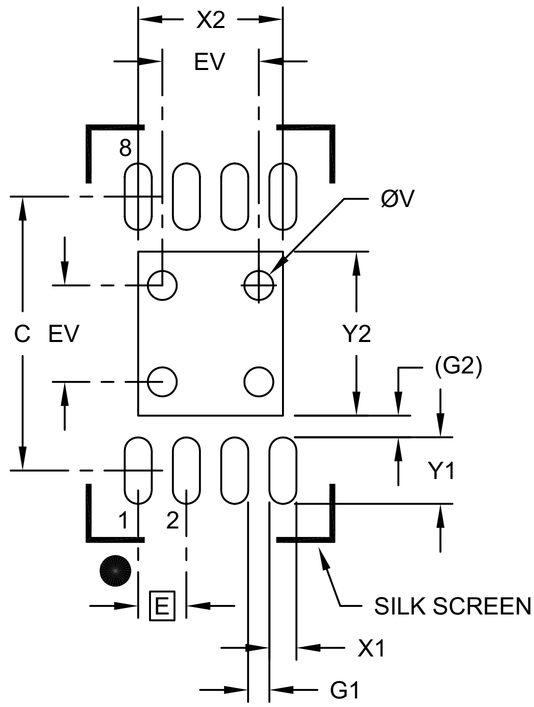
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-382A Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (8Q) - 2x3 mm Body [VDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.50
Optional Center Pad Length	Y2			1.70
Contact Pad Spacing	C		2.84	
Contact Pad Width (X8)	X1			0.28
Contact Pad Length (X8)	Y1			0.69
Space Between Pads	G1	0.20		
Contact Pad to Center Pad (X8)	(G2)	0.225 REF		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2382A

APPENDIX A: REVISION HISTORY

Revision B (November 2022)

- Document converted to Microchip format
- Updated Package Drawings in **Section 7.1 "Package Marking Information"**

Revision A (February 2015)

- Original release of this document

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	-XXXX	-XX(1)
Device	SMBus Address	Package	Tape and Reel Option

Device: EMC1412: Multiple Channel, 1°C Accuracy Temperature Sensors with Beta Compensation

SMBus Address:
- 1 = Fixed Address: 1001_100(r/w)
- A = Programmable Address
- 2 = Fixed Address: 1001_101(r/w)

Package:
- ACZL = 8-Lead Plastic Micro Small Outline (MSOP), RoHS Compliant
- AC3 = 8-Lead Very Thin Plastic Dual Flat, No Lead (TDFN), RoHS Compliant

Tape and Reel: TR = Tape and Reel

Examples:

a) EMC1412-1-ACZL-TR: 8-pin MSOP package, fixed SMBus Address 1001_100(r/w)

b) EMC1412-2-ACZL-TR 8-pin MSOP package, fixed SMBus Address 1001_101(r/w)

c) EMC1412-A-AC3-TR: 8-pin TDFN package, programmable SMBus address selectable via THERM pull-up

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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