

# EMC2DXV5T1, EMC5DXV5T1

Preferred Devices

## Dual Common Base-Collector Bias Resistor Transistors

### NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the EMC5DXV5T1 series, two complementary BRT devices are housed in the SOT-553 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- Lead Free

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted, common for  $Q_1$  and  $Q_2$ , - minus sign for  $Q_1$  (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CB0}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mAdc

#### THERMAL CHARACTERISTICS

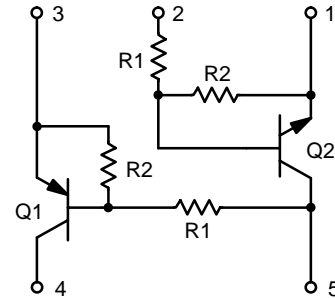
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	357 (Note 1) 2.9 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	500 (Note 1) 4.0 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad



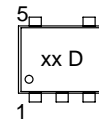
ON Semiconductor®

<http://onsemi.com>



SOT-553  
CASE 463B

#### MARKING DIAGRAM



xx = Specific Device Code  
D = Date Code

#### ORDERING INFORMATION

Device	Package	Shipping†
EMC2DXV5T1	SOT-553	4 mm pitch 4000/Tape & Reel
EMC2DXV5T5	SOT-553	2 mm pitch 8000/Tape & Reel
EMC5DXV5T1	SOT-553	4 mm pitch 4000/Tape & Reel
EMC5DXV5T5	SOT-553	2 mm pitch 8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

# EMC2DXV5T1, EMC5DXV5T1

## DEVICE MARKING AND RESISTOR VALUES

Device	Marking	Transistor 1 – PNP		Transistor 2 – NPN	
		R1 (K)	R2 (K)	R1 (K)	R2 (K)
EMC2DXV5T1	UC	22	22	22	22
EMC5DXV5T1	U5	4.7	10	47	47

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### Q1 TRANSISTOR: PNP

#### OFF CHARACTERISTICS

Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	100	nAdc
Collector-Emitter Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	500	nAdc
Emitter-Base Cutoff Current (V <sub>EB</sub> = 6.0, I <sub>C</sub> = 5.0 mA)	EMC2DXV5T1 EMC5DXV5T1 I <sub>EBO</sub>	– –	– –	0.2 1.0	mAdc

#### ON CHARACTERISTICS

Collector-Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	–	–	Vdc
DC Current Gain (V <sub>CE</sub> = 10 V, I <sub>C</sub> = 5.0 mA)	EMC2DXV5T1 EMC5DXV5T1 h <sub>FE</sub>	60 20	100 35	– –	
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0.3 mA)	V <sub>CE(SAT)</sub>	–	–	0.25	Vdc
Output Voltage (on) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 2.5 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OL</sub>	–	–	0.2	Vdc
Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.5 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OH</sub>	4.9	–	–	Vdc
Input Resistor	EMC2DXV5T1 EMC5DXV5T1 R1	15.4 3.3	22 4.7	28.6 6.1	kΩ
Resistor Ratio	EMC2DXV5T1 EMC5DXV5T1 R1/R2	0.8 0.38	1.0 0.47	1.2 0.56	

### Q2 TRANSISTOR: NPN

#### OFF CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	100	nAdc
Collector-Emitter Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	500	nAdc
Emitter-Base Cutoff Current (V <sub>EB</sub> = 6.0, I <sub>C</sub> = 5.0 mA)	EMC2DXV5T1 EMC5DXV5T1 I <sub>EBO</sub>	– –	– –	0.2 0.1	mAdc

#### ON CHARACTERISTICS

Collector-Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	–	–	Vdc
DC Current Gain (V <sub>CE</sub> = 10 V, I <sub>C</sub> = 5.0 mA)	EMC2DXV5T1 EMC5DXV5T1 h <sub>FE</sub>	60 80	100 140	– –	
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0.3 mA)	V <sub>CE(SAT)</sub>	–	–	0.25	Vdc
Output Voltage (on) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 2.5 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OL</sub>	–	–	0.2	Vdc
Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.5 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OH</sub>	4.9	–	–	Vdc
Input Resistor	EMC2DXV5T1 EMC5DXV5T1 R1	15.4 33	22 47	28.6 61	kΩ
Resistor Ratio	EMC2DXV5T1 EMC5DXV5T1 R1/R2	0.8 0.8	1.0 1.0	1.2 1.2	

# EMC2DXV5T1, EMC5DXV5T1

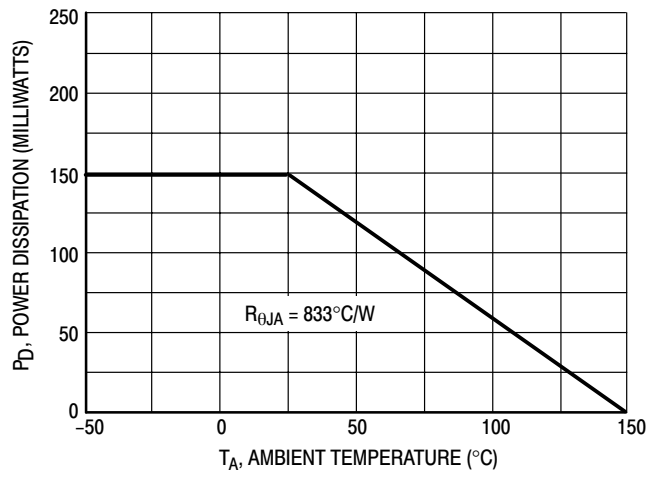


Figure 1. Derating Curve

# EMC2DXV5T1, EMC5DXV5T1

## TYPICAL ELECTRICAL CHARACTERISTICS — EMC2DXV5T1 PNP TRANSISTOR

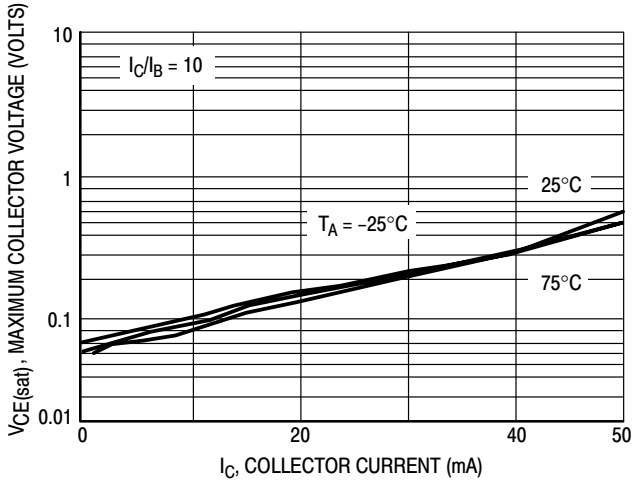


Figure 2.  $V_{CE(sat)}$  versus  $I_C$

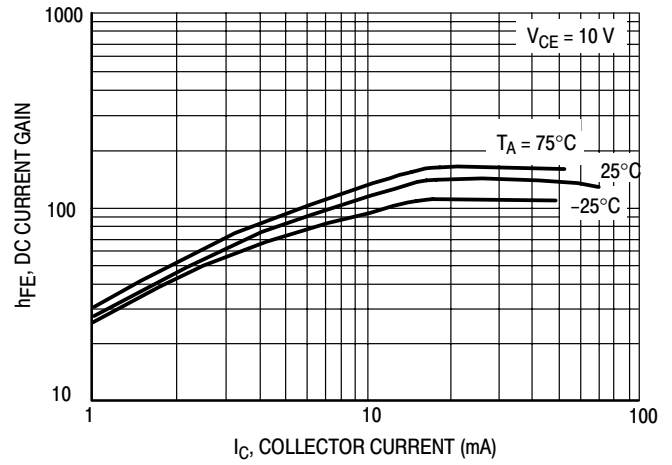


Figure 3. DC Current Gain

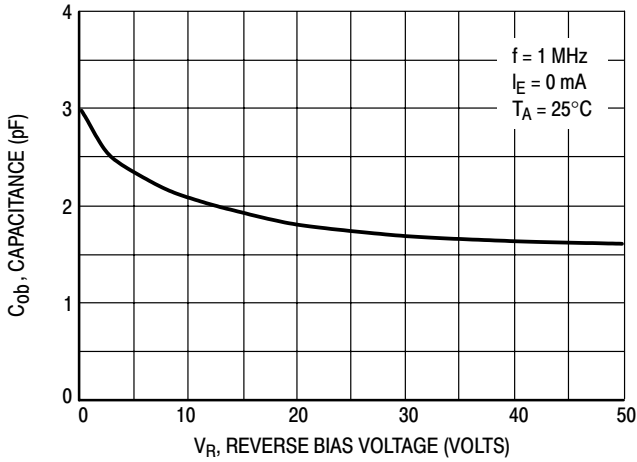


Figure 4. Output Capacitance

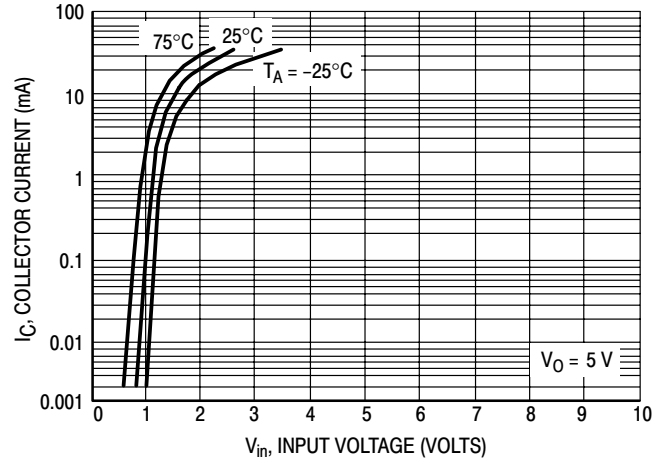


Figure 5. Output Current versus Input Voltage

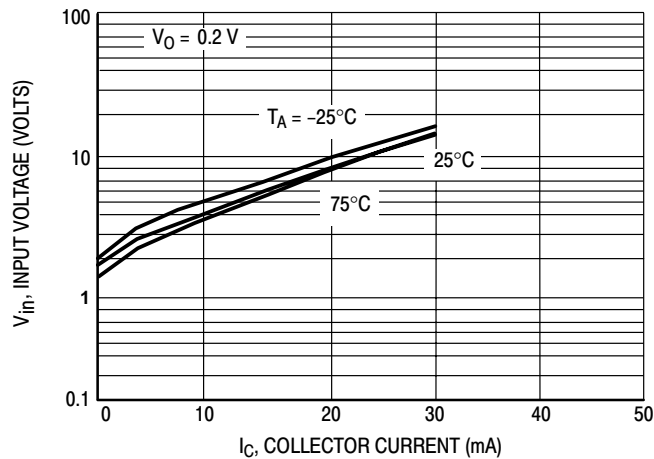


Figure 6. Input Voltage versus Output Current

# EMC2DXV5T1, EMC5DXV5T1

## TYPICAL ELECTRICAL CHARACTERISTICS — EMC2DXV5T1 NPN TRANSISTOR

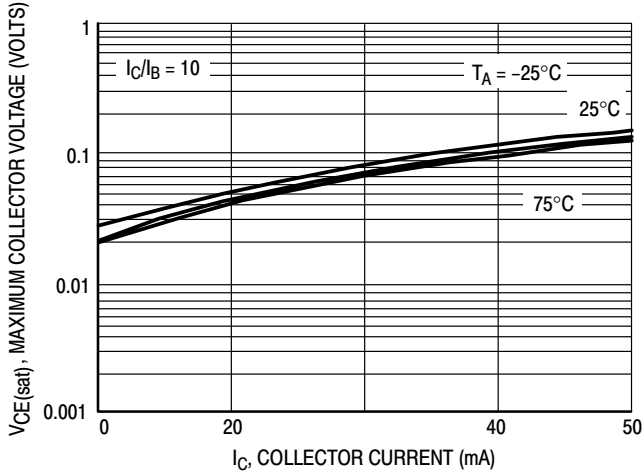


Figure 7.  $V_{CE(sat)}$  versus  $I_C$

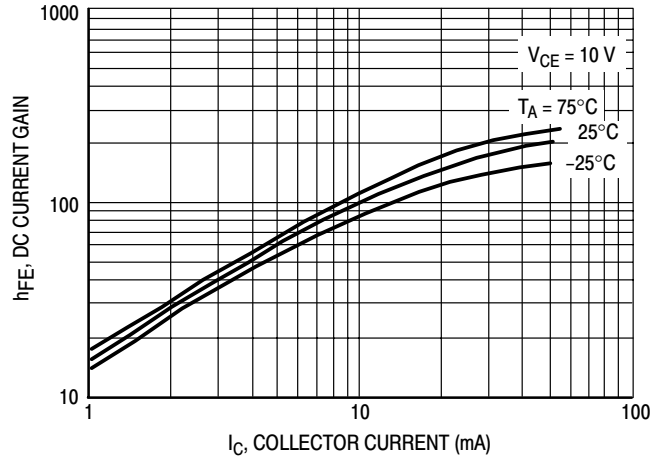


Figure 8. DC Current Gain

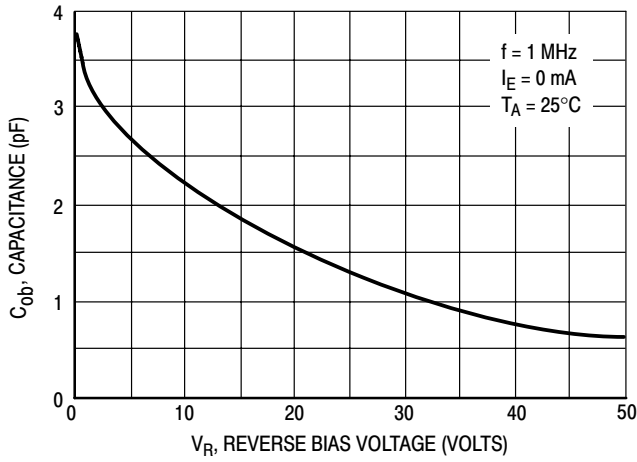


Figure 9. Output Capacitance

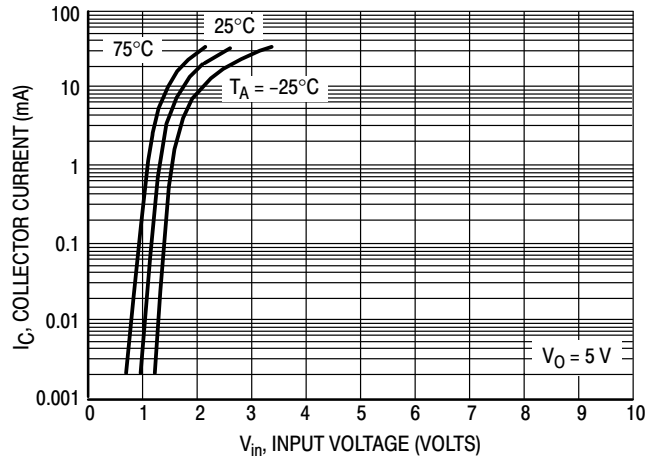


Figure 10. Output Current versus Input Voltage

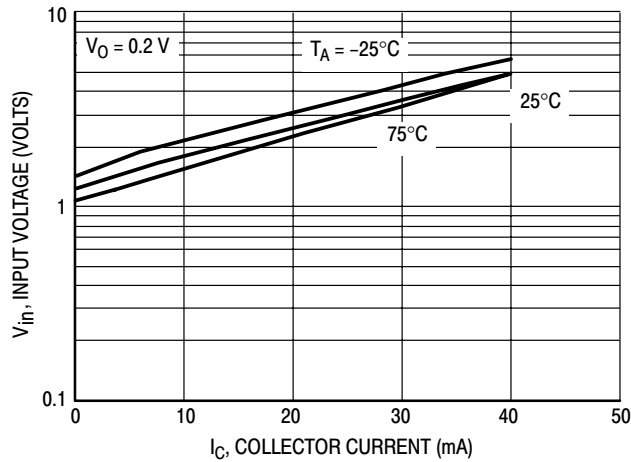


Figure 11. Input Voltage versus Output Current

# EMC2DXV5T1, EMC5DXV5T1

## TYPICAL ELECTRICAL CHARACTERISTICS — EMC5DXV5T1 PNP TRANSISTOR

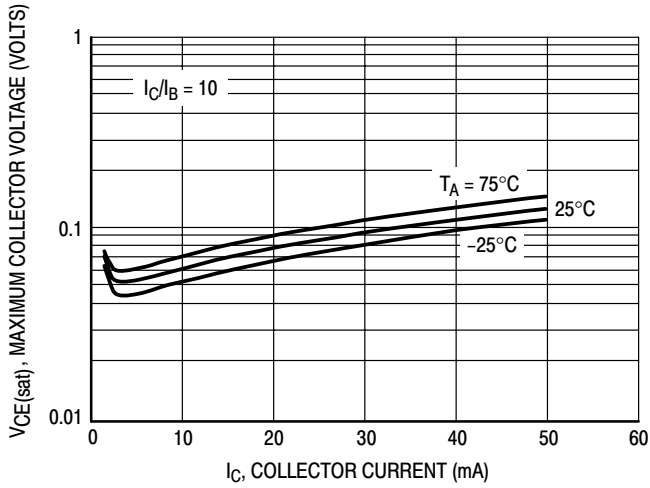


Figure 12.  $V_{CE(sat)}$  versus  $I_C$

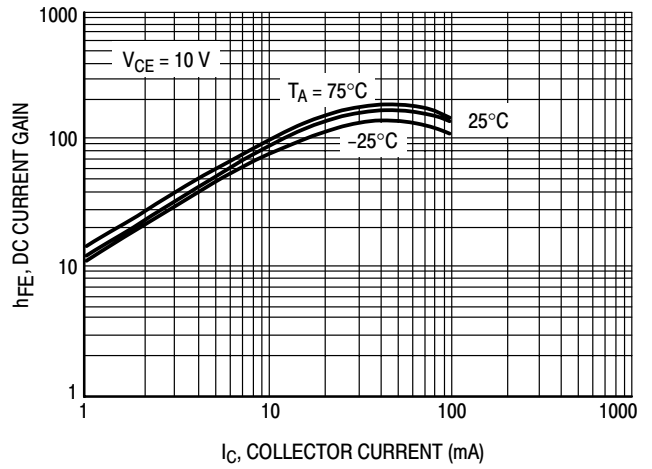


Figure 13. DC Current Gain

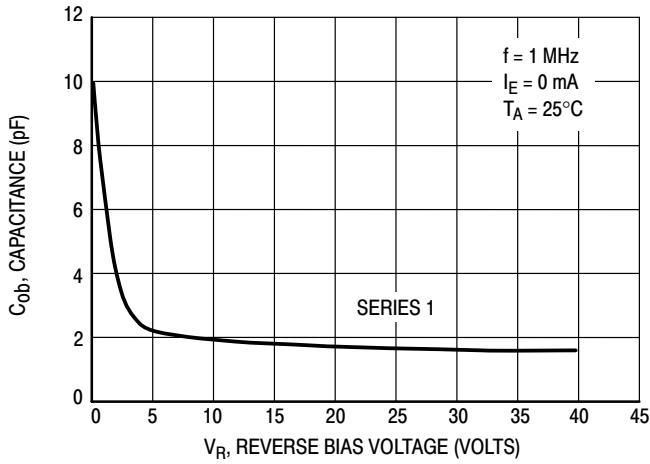


Figure 14. Output Capacitance

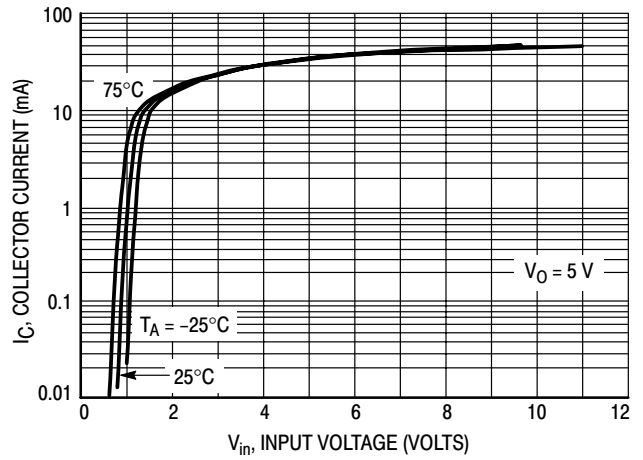


Figure 15. Output Current versus Input Voltage

# EMC2DXV5T1, EMC5DXV5T1

## TYPICAL ELECTRICAL CHARACTERISTICS — EMC5DXV5T1 NPN TRANSISTOR

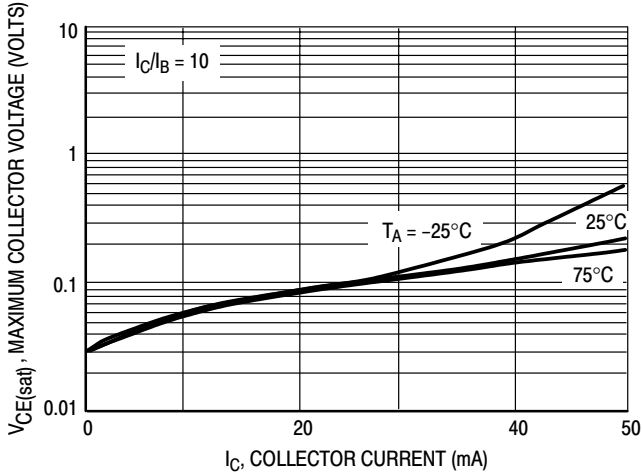


Figure 16.  $V_{CE(sat)}$  versus  $I_C$

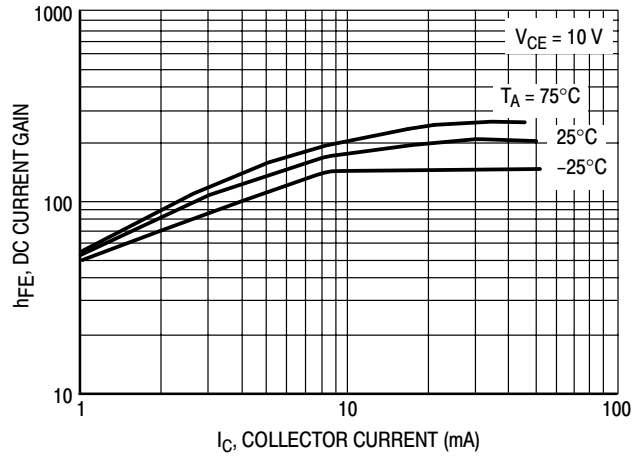


Figure 17. DC Current Gain

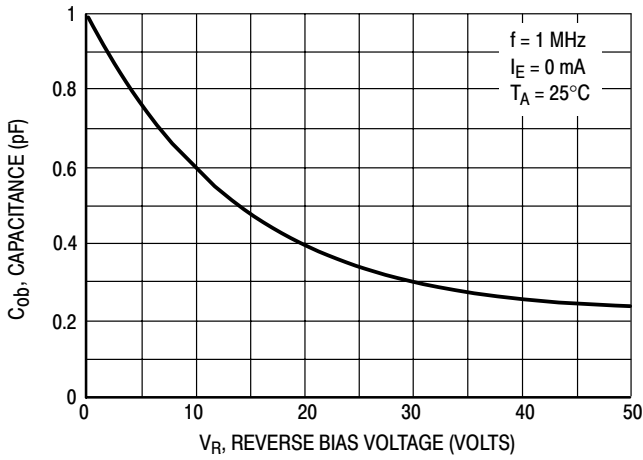


Figure 18. Output Capacitance

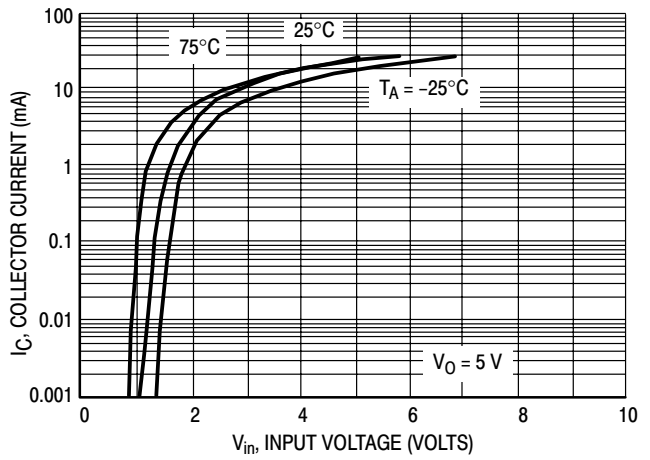


Figure 19. Output Current versus Input Voltage

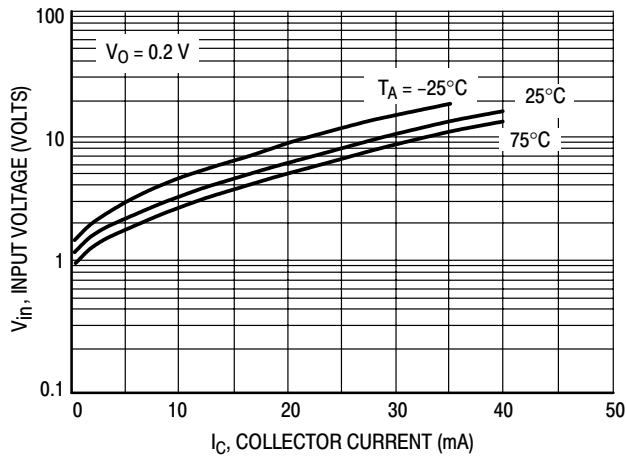


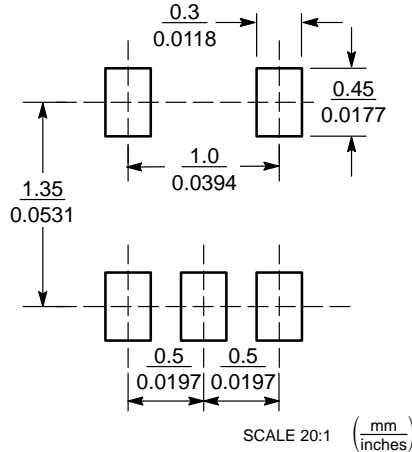
Figure 20. Input Voltage versus Output Current

**INFORMATION FOR USING THE SOT-553 SURFACE MOUNT PACKAGE**

**MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS**

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



**SOT-553**

**SOT-553 POWER DISSIPATION**

The power dissipation of the SOT-553 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet for the SOT-553 package,  $P_D$  can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{833^\circ\text{C/W}} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT-553 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-553 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

**SOLDERING PRECAUTIONS**

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

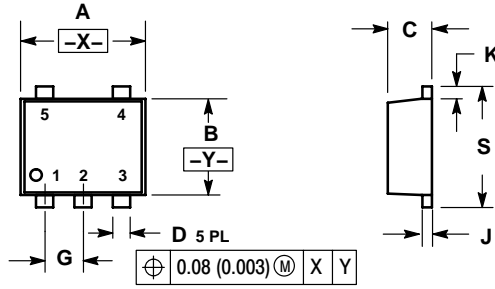
\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.



# EMC2DXV5T1, EMC5DXV5T1

## PACKAGE DIMENSIONS

SOT-553  
 XV5 SUFFIX  
 5-LEAD PACKAGE  
 CASE 463B-01  
 ISSUE O




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

# EMC2DXV5T1, EMC5DXV5T1

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