EMC4002

SMBus Fan Driver with Temperature Monitoring

PRODUCT FEATURES

Data Sheet

Description

The EMC4002 is a combination fan controller device, temperature sensor, and thermal monitor. It contains two RPM based Fan Control Algorithms that monitor the fan's speed and automatically adjust the drive to maintain the desired fan speed. These RPM based Fan Control Algorithms act independently and can be coupled to either a Dual Voltage High Side Fan driver or a PWM output. The Dual Voltage High Side fan drivers offer power savings by only drawing current from the necessary supply line based on the output voltage settings.

In addition, the EMC4002 monitors up to nine (9) external diode or thermistor channels and up to seven (7) voltage channels.

The EMC4002 also acts as an always on thermal monitor to signal a system wide interrupt should the CPU well temperature exceed a hardware set limit that cannot be altered via software. This ThermTrip logic uses signals from other external devices to determine overall system operation.

Finally, the EMC4002 contains a programmable Low Dropout Voltage Regulator to supply 3.3V, 2.5V, or a user selected voltage. This LDO is muxed with one of the two Dual Voltage High Side Fan Drivers for flexibility. Each can source up to 600mA of current from the VDD_5V supply.

Features

- RPM Closed-loop Control
  - "Set and Forget control"
  - 1% control accuracy with external clock
  - Two 10 Bit PWMs
  - Two 10 bit TACHs
- BC-Link™ Communications Interface
  - Up to 24Mbps data rate
  - Multiplexed with SMBus
- Flexible Thermal Monitors
  - Anti-Parallel Diodes allow 2 thermal diodes on one DP/DN pair
  - Two DP and DN pins may also be used as voltage inputs to monitor thermistors or voltages
- Voltage Regulator Multiplexed with Dual Voltage Fan Driver
  - LDO: 3.3V in, 600mA @ 2.5V out, or 5V in, 400mA @ 3.3V out
  - Dual Voltage Fan Driver rated 600mA @ 5V
- Vset uses a single 1% resistor
- Voltage Programmable Fail-Safe Monitor
  - External voltage programmed thermal sensor
  - Can use either a remote diode or thermistor
- ThermTrip Logic Integration
- Dual Voltage Fan Driver
  - Uses 5V or 3.3V supply for power efficiency
  - 600mA maximum output current drive
  - 10 bit resolution
- Up to Nine External Temperature Monitors
  - ±1°C Accuracy 60°C to 100°C
  - Resistance Error Correction
  - Automatically detects and supports CPU diodes requiring the BJT or Transistor models
- Up to Seven Voltage Monitors
  - Monitors VDD
  - Programming Voltage (VSET)
  - Vcp1, Vcp2, and a low (0.8V max) voltage input
  - Two voltage inputs mux'd on diode lines
- 5 (mux'd) General Purpose Digital I/O's
- SMBus 2.0 Compliant interface
  - Two selectable addresses
  - SMBus Alert
- 48 pin QFN, RoHS Compliant package, 7x7mm with exposed pad

Order Number:

EMC4002-HZH for 48-pin, RoHS Compliant package

This product meets the halogen maximum concentration values per IEC61249-2-21

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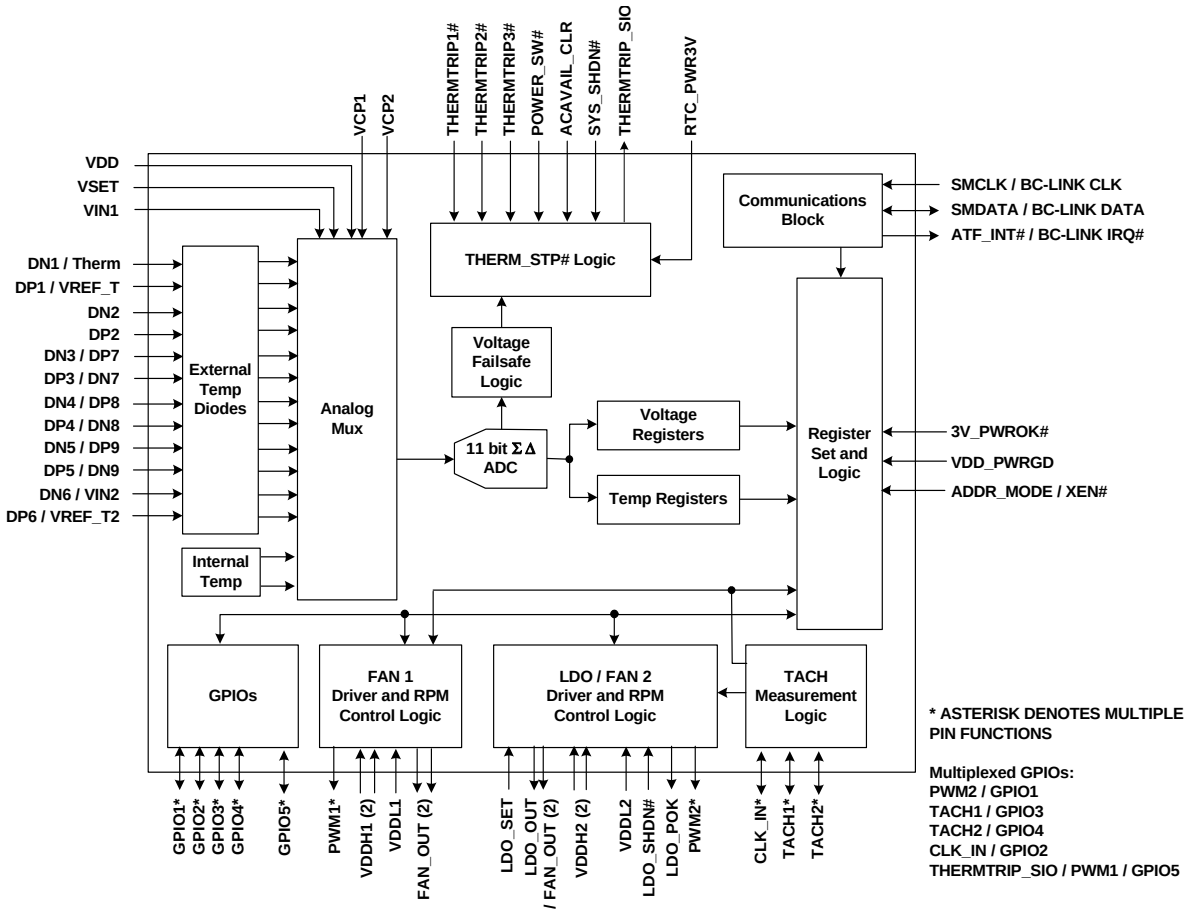

Figure 1.1 EMC4002 Functional Block Diagram

Chapter 2 Pin Configuration

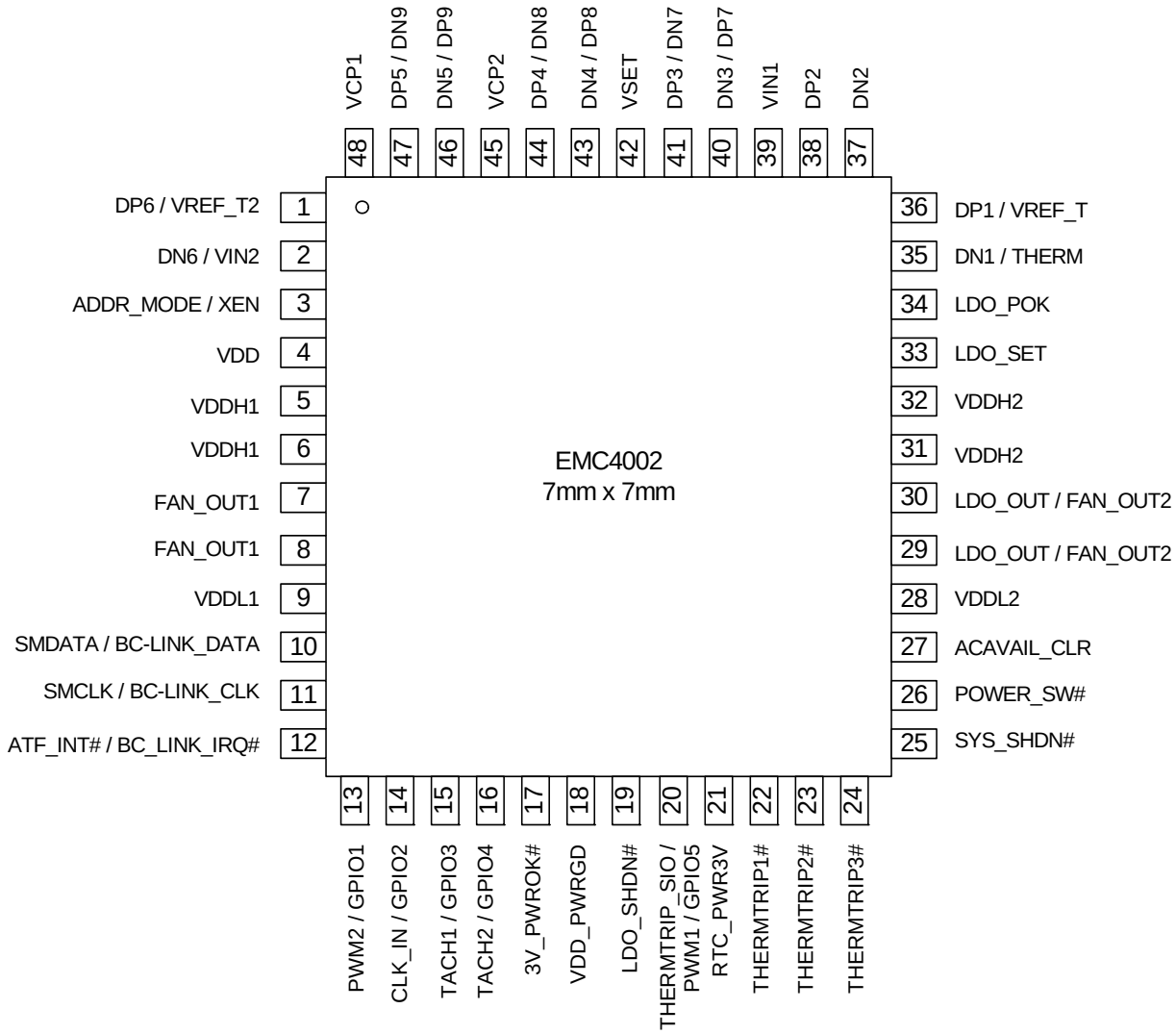

Figure 2.1 Pin Diagram for EMC4002

Table 2.1 Pin Functions for EMC4002

PIN NUMBER	NAME	FUNCTION	PIN TYPE	POWER PLANE
1	DP6 / VREF_T2	DP6 - External Diode 6 positive (anode) connection	AIO (2V)	VDD
		VREF_T2 - Switched reference output	AIO (2V)	VDD
2	DN6 / VIN2	DN6 - External Diode 6 negative (cathode) connection	AIO (2V)	VDD
		VIN2 - General ADC input 2	AIO (2V)	VDD
3	ADDR_MODE / XEN	ADDR_MODE - Address mode selection	DI (5V)	VDD
		XEN - XOR Mode enable	DI (5V)	VDD
4	VDD	Positive Supply Voltage for general operation	Power	VDD
5	VDDH1	5V supply for Dual Voltage Fan Driver	Power (5V)	VDDH1
6	VDDH1	5V supply for Dual Voltage Fan Driver	Power (5V)	VDDH1
7	FAN_OUT1	Fan output for Dual Voltage Fan Driver 1	AO (5V)	VDDH1 and VDDL1
8	FAN_OUT1	Fan output for Dual Voltage Fan Driver 1	AO (5V)	VDDH1 and VDDL1
9	VDDL1	3.3V supply for Dual Voltage Fan Driver	Power	VDDL1
10	SMDATA / BC-LINK_DATA	SMDATA - Bi-directional SMBus data line. Requires a pull up resistor	DIOD (5V)	VDD
		BC-LINK_DATA - Bi-directional BC-Link Data line. Requires a pull-up resistor	DIOD (5V)	VDD
11	SMCLK / BC-LINK_CLK	SMCLK - SMBus Clock line.	DI (5V)	VDD
		BC-LINK_CLK - BC-LINK Clock line.	DI (5V)	VDD
12	ATF_INT# / BC-LINK_IRQ#	ATF_INT# - Active low interrupt output for SMBus	OD (5V)	VDD
		BC-LINK_IRQ# - Active low interrupt output for BC-LINK	OD (5V)	VDD
13	PWM2 / GPIO1	PWM2 - Open Drain PWM Output (software programmed)	OD (5V)	VDD
		PWM2 - Push - Pull PWM Output (software programmed)	DO	VDD
		GPI1 - General purpose input (default)	DI (5V)	VDD
		GPO1 - General purpose push-pull output (software programmed)	DO	VDD
		GPO1 - General purpose open drain output (software programmed)	OD (5V)	VDD

Table 2.1 Pin Functions for EMC4002 (continued)

PIN NUMBER	NAME	FUNCTION	PIN TYPE	POWER PLANE
14	CLK_IN / GPIO2	CLK_IN - 32.768kHz clock input for TACH measurement (default)	DI (5V)	VDD
		GPI2 - General purpose input (software programmed)	DI (5V)	VDD
		GPO2 - General purpose push-pull output (software programmed)	DO	VDD
		GPO2 - General purpose open drain output (software programmed)	OD (5V)	VDD
15	TACH1 / GPIO3	TACH1 - TACH input for fan controller 1 (default)	DI (5V)	VDD
		GPI3 - General purpose input (software programmed)	DI (5V)	VDD
		GPO3 - General purpose push-pull output (software programmed)	DO	VDD
		GPO3 - General purpose open drain output (software programmed)	OD (5V)	VDD
16	TACH 2 / GPIO4	TACH2 - TACH input for fan controller 2 (software programmed)	DI (5V)	VDD
		GPI4 - General purpose input (default)	DI (5V)	VDD
		GPO4 - General purpose push-pull output (software programmed)	DO	VDD
		GPO4 - General purpose open drain output (software programmed)	OD (5V)	VDD
17	3V_PWROK#	Active low power okay input	DI (5V)	VDD
18	VDD_PWRGD	Active high power okay input	DI (5V)	VDD
19	LDO_SHDN#	Active low shutdown for LDO	DI (5V)	VDD

Table 2.1 Pin Functions for EMC4002 (continued)

PIN NUMBER	NAME	FUNCTION	PIN TYPE	POWER PLANE
20	THERMTRIP_SIO / PWM1 / GPIO5	THERMTRIP_SIO - Open Drain, active high output from ThermTrip Logic (default)	OD (5V)	RTC_PWR3V
		PWM1 - Open Drain PWM driver output	OD (5V)	RTC_PWR3V
		PWM1 - Push-Pull PWM driver output	DO	RTC_PWR3V
		GPI5 - General purpose input (software programmed)	DI (5V)	RTC_PWR3V
		GPO5 - General purpose push-pull output (software programmed)	DO	RTC_PWR3V
		GPO5 - General purpose open drain output (software programmed)	OD (5V)	RTC_PWR3V
21	RTC_PWR3V	RTC power input	Power	RTC_PWR3V
22	THERMTRIP1#	Active low thermtrip input	DI (5V)	RTC_PWR3V
23	THERMTRIP2#	Active low thermtrip input	DI (5V)	RTC_PWR3V
24	THERMTRIP3#	Active low thermtrip input	DI (5V)	RTC_PWR3V
25	SYS_SHDN#	Active low output from ThermTrip Logic	OD (5V)	RTC_PWR3V
26	POWER_SW#	Active low reset for ThermTrip logic output	DI (5V)	RTC_PWR3V
27	ACAVAIL_CLR	Active high reset for Thermtrip logic output	DI (5V)	RTC_PWR3V
28	VDDL2	VDDL2 - LDO supply	Power	VDDL2
		VDDL2 - Dual Voltage Fan Driver 2 3.3V supply	Power	VDDL2
29	LDO_OUT / FAN_OUT2	LDO_OUT - LDO regulated output	AO (5V)	VDDL2 and VDDH2
		FAN_OUT2 - Dual Voltage Fan Driver 2 Output	AO (5V)	VDDL2 and VDDH2
30	LDO_OUT / FAN_OUT2	LDO_OUT - LDO regulated output	AO (5V)	VDDL2 and VDDH2
		FAN_OUT2 - Dual Voltage Fan Driver 2 Output	AO (5V)	VDDL2 and VDDH2
31	VDDH2	VDDH2- LDO supply	Power	VDDH2
		VDDH2 - Dual Voltage Fan Driver 5V supply	Power	VDDH2
32	VDDH2	VDDH2 - LDO supply	Power	VDDH2
		VDDH2 - Dual Voltage Fan Driver 2 5V supply	Power	VDDH2
33	LDO_SET	LDO output set input	AIO	VDDH2

Table 2.1 Pin Functions for EMC4002 (continued)

PIN NUMBER	NAME	FUNCTION	PIN TYPE	POWER PLANE
34	LDO_POK	Power Ok output signal for LDO	OD (5V)	VDD
35	DN1 / THERM	DN1 - External Diode 1 negative (cathode) connection	AIO (2V)	VDD
		THERM - Thermistor measurement input	AIO (2V)	VDD
36	DP1 / VREF_T	DP1 - External Diode 1 positive (anode) connection	AIO (2V)	VDD
		VREF_T - Thermistor measurement reference voltage	AIO (2V)	VDD
37	DN2	External Diode 2 negative (cathode) connection	AIO (2V)	VDD
38	DP2	External Diode 2 positive (anode) connection	AIO (2V)	VDD
39	VIN1	General Voltage Input	AIO (2V)	VDD
40	DN3 / DP7	External Diode 3 negative (cathode) connection and External Diode 7 positive (anode) connection when APD enabled	AIO (2V)	VDD
41	DP3 / DN7	External Diode 3 positive (anode) connection and External Diode 7 negative (cathode) connection when APD enabled	AIO (2V)	VDD
42	VSET	Voltage input to set hardware failsafe temperature threshold	AIO (2V)	VDD
43	DN4 / DP8	External Diode 4 negative (cathode) connection and External Diode 8 positive (anode) connection when APD enabled	AIO (2V)	VDD
44	DP4 / DN8	External Diode 4 positive (anode) connection and External Diode 8 negative (cathode) connection when APD enabled	AIO (2V)	VDD
45	VCP2	Voltage Input for VCP2 channel	AIO	VDD
46	DN5 / DP9	External Diode 5 negative (cathode) connection and External Diode 9 positive (anode) connection when APD enabled	AIO (2V)	VDD
47	DP5 / DN9	External Diode 5 positive (anode) connection and External Diode 9 negative (cathode) connection when APD enabled	AIO (2V)	VDD
48	VCP1	Voltage Input for VCP1 channel	AIO	VDD
Exposed Bottom Pad	VSS	Ground Connection	Power	

The EMC4002 is available in a 48 pin 7mm x 7mm QFN package with exposed pad. The Exposed bottom pad must be electrically connected to ground for proper operation and thermal protection.

All pins labelled (5V) are 5V tolerant. All pins labelled (2V) are 2V tolerant.

The pin type is shown in Table 2.2.

Table 2.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
DI	Digital Input - this pin is used as a digital input. This pin is 5V tolerant.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
AO	Analog Output - this pin is used for outputting analog signals and amy have large current sourcing capabilities
DO	Push / Pull Digital Output - this pin is used as a digital output. It can both source and sink current.
DIOD	Digital Input / Open Drain Output this pin is used as an digital I/O. When it is used as an output, It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION Note 3.1	RATING	UNIT
Voltage on VDD pin	4V	V
Voltage on RTC_PWR3V pin	4V	V
Voltage on 5V tolerant pins	-0.3 to 6.5	V
Voltage on LDO_OUT pin	-0.3 to VDDH2 or VDDL2+ 0.3	V
Voltage on FAN_OUT pin	-0.3 to VDDH1 + 0.3 or VDDH2 + 0.3	V
Voltage on SYS_SHDN# and THERMTRIP_SIO pins	-0.3 to RTC_PWR3V + 0.3	V
Voltage on 2V tolerant pins	-0.3 to 2.6	V
Voltage on any other pin to GND	-0.3 to VDD + 0.3	V
Operating Ambient Temperature Range	0 to 85	°C
Operating Die Temperature Range	0 to 125	°C
Storage Temperature Range	-55 to 150	°C
Package Power Dissipation Note 3.2	1.2W up to T_A = 85°C	W
Power Derating	44, T_A > 85°C	mW /°C
Junction to Ambient (θ_{JA}) Note 3.3	20-52	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 3.1 All voltages are relative to ground.

Note 3.2 The Package Power Dissipation specification assumes a thermal via design consisting of nine 20mil vias connected to the ground plane with a 4x4mm thermal landing.

Note 3.3 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 52°C/W including localized PCB temperature increase. Refer to Application Note “Power and Layout Considerations for EMC4002” for design guidance to implement the thermal via and landing solution.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

VDD = 3V to 3.6V, RTC_PWR3V = 2V to 3.6V, VDDL2 = VDDH2 = 3V to 5.5V, VDDL1 = 3.3V to 3.6V, VDDH1 = 4.5V to 5.5V, T_A = 0°C to 85°C All Typical values at VDD = 3.3V, RTC_PWR3V = 3.3V, VDDH2 = VDDL2 = 3.3V, VDDH1 = 5V, VDDL1 = 3.3V, T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC Power						
Supply Voltage (VDD)	VDD	3	3.3	3.6	V	
RTC Supply Voltage	RTC_PWR 3V	2	3.3	3.6	V	
RTC Data Retention		2			V	
Supply Current from VDD pin	I_{SUS}		1.5	2	mA	Continuous Conversions, Fan Drivers enabled at max frequency (PWM)
Supply current from RTC_PWR3V pin	I_{RTC}			5	uA	Monitoring Disabled, Fan Drivers Disabled, LDO disabled, VDD disabled.
Sleep Current from VDD	I_{SLEEP}		700		uA	Fan drivers disabled, Monitoring disabled (3V_PWROK# or VSUS_PWRGD unasserted)
Low Power Current from VDD	I_{LPM}		900		uA	Fan drivers disabled. 3V_PWROK# or VSUS_PWRGD unasserted. LPM bit set. Continuous Conversions
POR Threshold	V_{PORR}		2.2		V	Rising edge of VDD or RTC_PWR3V
	V_{PORF}		2		V	Falling edge of VDD
External Temperature Monitors						
Temperature Accuracy			±0.5	±1	°C	60°C < T_{DIODE} < 100°C, 30°C < T_{die} < 85°C Note 3.4
			±1	±2	°C	0°C < T_{DIODE} < 125°C, 0°C < T_{die} < 115°C Note 3.4
Temperature Resolution			0.125		°C	
Conversion Time per Channel	t_{CONV}		43		ms	External Diodes 1 - 3
	t_{CONV}		22		ms	External Diodes 4 - 9
Diode decoupling capacitor	C_{FILTER}		2200	2700	pF	Connected across external diode
Resistance Error Corrected	R_{SERIES}			100	Ohm	Total series resistance in DP and DN lines
Thermistor Monitors						
Voltage Measurement Accuracy	V_{THERM}		0.5	1	%	20°C < T_{THERM} < 80°C 1%, 10k Thermistor connected to ground

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, RTC_PWR3V = 2V to 3.6V, VDDL2 = VDDH2 = 3V to 5.5V, VDDL1 = 3.3V to 3.6V, VDDH1 = 4.5V to 5.5V, T_A = 0°C to 85°C All Typical values at VDD = 3.3V, RTC_PWR3V = 3.3V, VDDH2 = VDDL2 = 3.3V, VDDH1 = 5V, VDDL1 = 3.3V, T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Temperature Accuracy	T_{THERM}		1	2	°C	20°C < T_{THERM} < 80°C 1%, 10k Thermistor connected to ground (Note 3.5), 1% resistor from VREF to VIN
Voltage Monitors						
Total Unadjusted Error	TUE			1	%	Measured at 3/4 full scale
Differential Non-Linearity	DNL		±0.5		LSB	
Input Impedance	RIN	232	300		kOhm	Impedance for those inputs with input attenuators (VCP1, VCP2, VDD)
Conversion Time Per Channel	t_{CONV}		12.25		ms	
PWM Driver						
PWM Resolution	PWM		1024		Steps	
PWM Duty Cycle	DUTY	0		100	%	
RPM Based Fan Controller						
Tachometer Range	TACH	480		16000	RPM	
Tachometer Setting Accuracy	Δ_{TACH}		±1	±2	%	External oscillator 32.768kHz
	Δ_{TACH}		±2.5	±5	%	Internal Oscillator 40°C < T_{DIE} < 100°C
Dual Voltage Fan Driver						
Supply current from VDDH pin	I_{DD5}		35		uA	Fan not being driven
Supply current from VDDL pin	I_{DD3}		140		uA	Fan not being driven
Output High Voltage from 5V supply	V_{OH_5V}		VDDH - 0.3	VDDH - 0.4	V	I_{SOURCE} = 600mA, VDDH = 5V
Sourcing Current	I_{SOURCE}			600	mA	
DC Short Circuit Current Limit	I_{SHORT}		700		mA	Sourcing current, Thermal shutdown not triggered, FAN_OUT = 0V
Short circuit delay	t_{DFS}		2		s	See Section 5.7.1
Output Capacitive Load	C_{LOAD}	10		100	uF	100mΩ < ESR < 1Ω

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, RTC_PWR3V = 2V to 3.6V, VDDL2 = VDDH2 = 3V to 5.5V, VDDL1 = 3.3V to 3.6V, VDDH1 = 4.5V to 5.5V, T_A = 0°C to 85°C All Typical values at VDD = 3.3V, RTC_PWR3V = 3.3V, VDDH2 = VDDL2 = 3.3V, VDDH1 = 5V, VDDL1 = 3.3V, T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Low Dropout Regulator						
LDO Input Voltage	V_{LDO_IN}	3.0	3.3	3.6	V	LDO_SET = Ground
		4.5	5	5.5	V	LDO_SET = 3.3V
LDO Output Voltage	V_{LDO_OUT}		2.5		V	LDO_SET = Ground
			3.3		V	LDO_SET = VDD
		1.12		2.5	V	LDO_SET = resistor divider
LDO Quiescent Current	I_{LDO}		140		uA	I_{LOAD} =0A, VDDH2 = VDDL2
LDO Output Current	I_{LOAD}	0		600	mA	LDO_OUT = 2.5V
	I_{LOAD}	0		400	mA	LDO_OUT = 3.3V
Regulated Output Voltage Accuracy	ΔV_{LDO_OUT}		1	2	%	I_{LOAD} = 600mA
Line Regulation	ΔV_{LNR}		0.5		%	I_{LOAD} = 600mA, V_{LDO_IN} = 3.0V to 3.6V
Load Regulation	ΔV_{LDR}		0.5		%	I_{LOAD} = 0A to 600mA
Short Circuit Current	I_{SHORT}		700	1000	mA	V_{LDO_OUT} = 0V
Output Capacitive Load requirement	C_{LOAD}	10		100	uF	100mΩ < ESR < 1Ω
POK Range relative to nominal LDO output Voltage	V_{OK}	80	82.5	85	%	LDO_SET = ground or +3.3V Compared to V_{LDO_OUT}
		75	82.5	90	%	LDO_SET = resistor divider Compared to V_{LDO_OUT}
POK Delay	t_{DPOK}	42	55	77	us	Delay after LDO output drops below the trip level.
Thermal Shutdown						
Thermal Shutdown Threshold	TSD_{TH}		150		°C	
Thermal Shutdown Hysteresis	TSD_{HYST}		50		°C	
Digital I/O, ALERT#, and LDO_POK pins						
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage	V_{OH}	VDD - 0.4			V	4mA current drive

Table 3.2 Electrical Specifications (continued)

VDD = 3V to 3.6V, RTC_PWR3V = 2V to 3.6V, VDDL2 = VDDH2 = 3V to 5.5V, VDDL1 = 3.3V to 3.6V, VDDH1 = 4.5V to 5.5V, T_A = 0°C to 85°C All Typical values at VDD = 3.3V, RTC_PWR3V = 3.3V, VDDH2 = VDDL2 = 3.3V, VDDH1 = 5V, VDDL1 = 3.3V, T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Output Low Voltage	V_{OL}			0.4	V	4mA current sink
Leakage Current	ILEAK			±5	uA	ALERT#, SYS_SHDN#, THERMTRIP_SIO pins Device powered or unpowered

Note 3.4 T_{DIE} refers to the internal die temperature and may not match T_A due to self heating of the device. The internal temperature sensor will return T_{DIE}.

Note 3.5 The EMC4002 performs no calculations to determine the thermistor temperature. These specifications are based on the thermistor data shown in Table A.1, ""Low Side" Thermistor Look Up Table" and are not guaranteed.

3.3 SMBus Electrical Characteristics

VDD = 3V to 3.6V, T_A = 0°C to 85°C, Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0			V	SMCLK
Input Low Voltage	V_{IL}			0.8	V	SMCLK
Output High Voltage	V_{OH}	VDD - 0.4			V	24mA current drive - SMDATA
Output Low Voltage	V_{OL}			0.4	V	24mA current sink - SMDATA
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Device Powered or Unpowered
Hysteresis			420		mV	
SMBus Timing						
Input Capacitance	C_{IN}		5		pF	
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.6		6	us	
Data Setup Time	$t_{SU:DAT}$	0.6		72	us	
Clock Low Period	t_{LOW}	1.3			us	

VDD = 3V to 3.6V, T_A = 0°C to 85°C, Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

3.4 BC-Link Electrical Characteristics

VDD = 3V to 3.6V, T_A = 0°C to 85°C, Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Electrical Interface						
Input High Voltage	V_{IH}	2.0			V	BC-LINK_CLK and BC-LINK_DAT
Input Low Voltage	V_{IL}			0.8	V	BC-LINK_CLK and BC-LINK_DAT
Output High Voltage	V_{OH}	VDD - 0.4			V	24mA current drive - BC-LINK_DAT
Output Low Voltage	V_{OL}			0.4	V	24mA current sink - BC-LINK_DAT
Input High/Low Current	I_{IH} / I_{IL}	-1		1	uA	
Hysteresis			420		mV	
Input Capacitance	C_{IN}		5		pF	
Timing						
Clock Period	t_{CLK}	34.7	41.67	52.1	ns	
Data Hold Time	$t_{HD:DAT}$	0			us	
Data Setup Time	$t_{SU:DAT}$	30			us	Data must be valid before clock
Clock Duty Cycle	Duty	40	50	60	%	

Chapter 4 Communications Protocols

The EMC4002 communicates with a host controller, such as a Microchip KBC using one of two communications protocols that are automatically detected upon every communication. The two protocols supported are the System Management Bus (SMBus) and the proprietary communications protocol called BC-Link.

APPLICATION NOTE: No communications should be sent during the first 15ms after power up.

4.1 Selecting Communications Bus

The selection of the communications bus is performed automatically for each transaction. Once a communication begins, the communication type is fixed until the communication ends.

After the communication ends, the device will wait 50ms before it resets the automatic detection circuitry. Therefore, any communications received during this window will be assumed to be using the protocol that was previously detected.

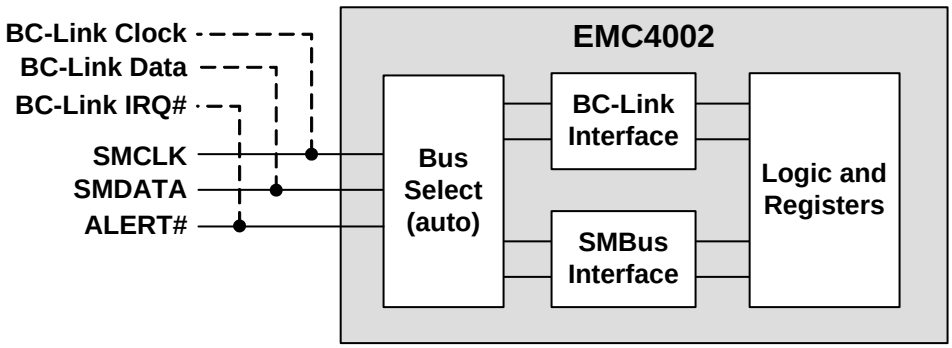

Figure 4.1 BC-Link Multiplexed with SMBus

4.2 SMBus Communications

The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.2, "SMBus Timing Diagram". Stretching of the SMCLK signal is supported, however the EMC4002 will not stretch the clock signal.

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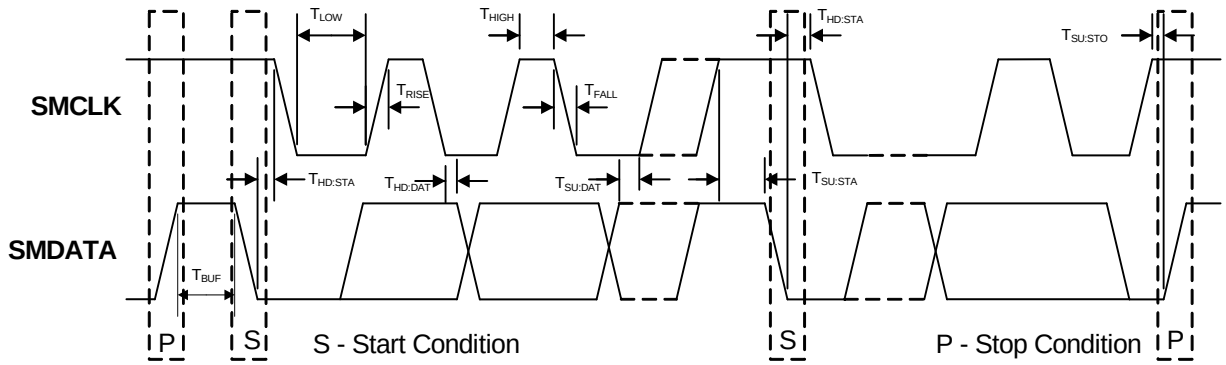

Figure 4.2 SMBus Timing Diagram

4.2.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state. When the EMC4002 detects an SMBus Start bit, it will disable the BC-Link protocol circuitry and communicate using the SMBus Protocol

4.2.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by a -bit RD / $\overline{WR}$ indicator. If this RD / WR bit is a logic ‘0’, then the SMBus Host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, then the SMBus Host is reading data from the client device.

The EMC4002 can be used with two 7 bit client addresses. These addresses are chosen by the value of the pull-up resistor on the ADDR_MODE/XEN pin upon power up. This pin also selects the mode for Remote Diode #1, which can be either a diode or a thermistor. Table 4.1, "SMBus Address and Mode Selection" summarizes the mode and address selections.

Table 4.1 SMBus Address and Mode Selection

R_{PULLUP} ON ADDR_MODE/XEN PIN	REMOTE1 MODE	SMBUS ADDRESS
<= 4.7k Ohm ±5%	2N3904	0101 111(r/w)b
10K Ohm ±5%	2N3904	0101 110(r/w)b
18K Ohm ±5%	Thermistor	0101 111(r/w)b
>= 33k Ohm ±5%	Thermistor	0101 110(r/w)b

Attempting to communicate with the EMC4002 SMBus interface with an invalid client address or invalid protocol will result in no response from the device and will not affect its register contents.

4.2.3 SMBus Data Bytes

All SMBus Data bytes are sent MSBit first and composed of 8-bits of information.

4.2.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the ATF_INT# pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The Host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the 8th data bit has been sent.

4.2.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the EMC4002 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

4.2.6 SMBus Time-out

The EMC4002 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

4.2.7 SMBus and I^2C Compliance

The major difference between SMBus and I^2C devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz.
2. The client protocol will reset if the clock is held for longer than 30ms.
3. I2C devices do not support the Alert Response Address functionality (which is optional for SMBus).

4.3 SMBus Protocols

The EMC4002 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte and Write Byte as valid protocols as shown below. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in Table 4.2.

Table 4.2 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
Data sent	Data sent

4.3.1 SMBus Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.3:

Table 4.3 Write Byte Protocol

START	CLIENT ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
0 ->1	0101_110	0	0	XXh	0	XXh	0	1 -> 0

4.3.2 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.4.

Table 4.4 Read Byte Protocol

START	Client ADDRESS	WR	ACK	Register Address	ACK	START	Client Address	RD	ACK	Register Data	NACK	STOP
0->1	0101_110	0	0	XXh	0	0 ->1	0101_110	1	0	XXh	1	1 -> 0

4.3.3 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.5.

Table 4.5 Send Byte Protocol

START	CLIENT ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
0 -> 1	0101_110	0	0	XXh	0	1 -> 0

4.3.4 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.6.

Table 4.6 Receive Byte Protocol

START	CLIENT ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
0 -> 1	0101_110	0b	0b	XXh	1	1 -> 0

4.3.5 SMBus Alert Response Address

The ATF_INT# output can be used as a processor interrupt or as an $\overline{\text{SMBALERT}}$.

When it detects that the $\overline{\text{SMBALERT}}$ pin is asserted, the host will send the Alert Response Address (general address of 000_1100b) on the bus. All devices with active interrupts will respond with their client address as shown in Table 4.7.

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Table 4.7 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
0 -> 1	000_1100	1b	0b	0101_110x	1	1 -> 0

The EMC4002 will respond to the ARA command and will immediately de-assert the ATF_INT# pin by clearing the INTEN bit (see Section 6.30).

4.4 BC-Link Interface

The BC-Link is a proprietary bus developed to allow communication between a host controller based device to a companion device. This device uses this serial bus to read and write registers and for interrupt processing. The interface uses a data port concept, where the base interface has an address register, data register and a control register, defined in the Microchip's 8051's SFR space.

Refer to documentation for the 8051 based host controller for details on how to access the EMC4002 via the BC-Link Interface.

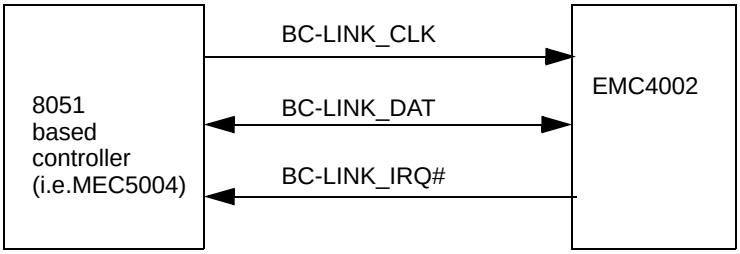

Figure 4.3 LSBC Bus Interface Signal Connections

Chapter 5 Functional Description

5.1 General Operation

The EMC4002 is a combination fan controller device, temperature sensor, and thermal monitor. It contains two RPM based Fan Control Algorithms that monitor the fan's speed and automatically adjust the drive to maintain the desired fan speed. These RPM based Fan Control Algorithms act independently and can be coupled to either a Dual Voltage High Side Fan driver or a PWM output. The Dual Voltage High Side fan drivers offer power savings by only drawing current from the necessary supply line based on the output voltage settings.

In addition, the EMC4002 monitors up to nine (9) external diode or thermistor channels and up to seven (7) voltage channels.

The EMC4002 also acts as an always on thermal monitor to signal a system wide interrupt should the CPU temperature exceed a hardware set limit that cannot be altered via software. This ThermTrip logic uses signals from other external devices to determine overall system operation.

Finally, the EMC4002 contains a programmable Low Dropout Voltage Regulator to supply 3.3V, 2.5V, or a user selected voltage. This LDO is muxed with one of the two Dual Voltage High Side Fan Drivers for flexibility. Each can source up to 600mA of current from the 5V supply or 300mA from the 3.3V supply.

A system level diagram is shown in Figure 5.1.

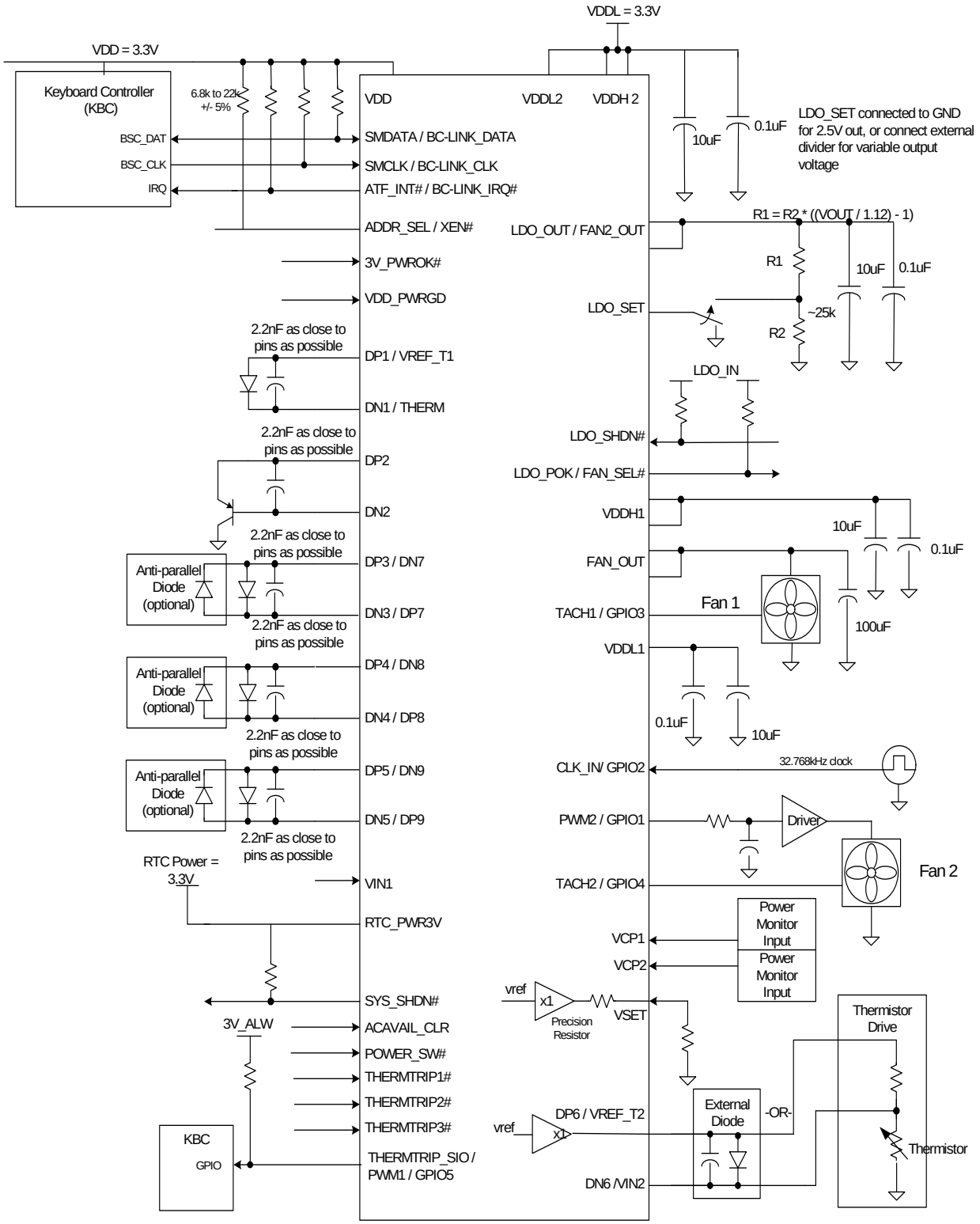

Figure 5.1 System Diagram for EMC4002

5.2 Conversion Cycle

The EMC4002 monitors at least six (6) temperature channels (not including internal diode) and as many as nine (9) in addition to at least five (5) voltage channels and as many as seven (7). All of these measurements are performed in a round-robin loop. Whenever the EMC4002 monitoring is disabled (by de-asserting either the 3V_PWROK# or the VDD_PWRGD signals) and restarted, the cycle starts from the beginning.

Table 5.1 Conversion Channel Order

ORDER	CHANNEL	RESOLUTION
1	External Diode 1	12-bit
	Thermistor 1 (if enabled)	10-bit
2	VSET Voltage	10-bit
3	VDD Voltage	10-bit
4	VCP1 Voltage	10-bit
5	VCP2 Voltage	10-bit
6	External Diode 2	12-bit
7	External Diode 3	12-bit
8	External Diode 7 (if enabled)	11-bit
9	External Diode 4	11-bit
10	External Diode 8 (if enabled)	11-bit
11	External Diode 5	11-bit
12	External Diode 9 (if enabled)	11-bit
13	External Diode 6 (if enabled)	11-bit
	VIN2 (if enabled)	10-bit
14	VIN1	10-bit
15	Internal Diode	9-bit

5.3 Power Modes

The EMC4002 has several power modes depending on which functions are enabled. The Temperature monitoring and Fan Drivers are each independently controlled. Typically, the device will only operate in the Run Mode. However, if either the 3V_PWROK# or VDD_PWRGD signals become released (either high or low respectively), then the other power modes are available.

- Run Mode - in this mode, the EMC4002 continuously samples and updates all of its temperature channels. The fan drivers are active and the RPM based Fan Control Algorithms are operating (if enabled).
- Low Power - In this mode, the EMC4002 is placed into a lower power mode. This mode is enabled by setting the LPM bit and de-asserting either the VDD_PWRGD or the 3V_PWROK# signals. In this mode the monitoring circuitry is still active and will sample and update all of its channels. The SYS_SHDN# pin will be not be asserted for any reason. The Fan Drivers will be disabled but the LDO will still be active unless disabled.

- Sleep - in this mode, the EMC4002 is placed into the lowest power mode available. This mode is enabled by clearing the LPM bit (if set) and de-asserting either the VDD_PWRGD or the 3V_PWROK# signals to disable monitoring. The Fan Drivers will be disabled and the LDO will still be active unless disabled. If disabled, then the device will be at its lowest power setting.
- RTC Power Mode - this mode is reached by removing the VDD power supply. The device will not function and cannot be communicated with in any way. The ThermTrip Logic will still be powered though it cannot be updated.

APPLICATION NOTE: When in the RTC Power Mode, the THERMTRIP_SIO pin will be set to the default setting of THERMTRIP_SIO.

Table 5.2 Power States

POWER STATE	TEMP AND LIMITS	FAN DRIVER	LDO	SMBUS AND GPIOS	SYS_SHDN	NOTES	ACTIVATION	SUPPLIES USED
Run Mode	Active	Active	User Defined	Active	Active	All active as programmed	VDD present, 3V_PWROK# and VSUS_PWRG asserted, VDDH and VDDL present	VDD VDDH and VDDL RTC
Low Power	Active	Not Active	User Defined	Active	Not Active	Monitoring active as programmed. Fan Drivers disabled.	VDD present, 3V_PWROK# or VSUS_PWRGD unasserted, LPM bit set	VDD VDDH and VDDL (if LDO Active) RTC
Sleep	Not Active	Not Active	User Defined	Active	Not Active	ADC, temp monitor, fan drivers disabled	VDD present 3V_PWROK# or VSUS_PWRGD unasserted, LPM bit not set	VDD (if LDO Active) VDDH and VDDL (if LDO Active) RTC
RTC Power	Not Active	Not Active	Not Active	Not Active	Not Active	All blocks powered down. Data retention on ThermTrip Status register only	VDD not present	RTC

5.4 Fan Control Modes of Operation

The EMC4002 has two modes of operation for the High Side Fan Driver. They are:

1. Manual Mode - in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Section 6.32, "Fan Driver Setting Registers") will update the fan drive based on the programmed ramp rate (default disabled).
   - The Manual Mode is enabled by clearing the EN_ALGO bit in the Fan Configuration Register (see Section 6.33, "Fan Configuration 1 Registers").
   - Whenever the Manual Mode is enabled the current drive settings will be changed to what was last used by the RPM control algorithm.
   - Setting the drive value to 00h will disable the High Side Fan Driver for lower power operation.
   - Changing the drive value from 00h will invoke the Spin Up Routine.
2. Using RPM based Fan Control Algorithm - in this mode of operation, the user determines a target tachometer reading and the drive setting is automatically updated to achieve this target speed.

Table 5.3 Fan Controls Active for Operating Mode

MANUAL MODE	ALGORITHM
Fan Driver Setting (read / write)	Fan Driver Setting (read only)
EDGES[1:0] (Fan Configuration)	EDGES[1:0] (Fan Configuration)
UPDATE[2:0] (Fan configuration)	UPDATE[2:0] (Fan Configuration)
LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)
SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)
Fan Step	Fan Step
-	Fan Minimum Drive
Valid TACH Count	Valid TACH Count
-	TACH Target
TACH Reading	TACH Reading
RANGE[2:0] (Fan Configuration 2)	RANGE[2:0] (Fan Configuration 2)
-	DRIVE_FAIL_CNT[2:0] (Spin Up Config) and Drive Fail Band

5.5 RPM Based Fan Control Algorithms

The EMC4002 includes two RPM based Fan Control Algorithms. Each algorithm operates independently and controls a separate fan driver.

This fan control algorithm uses Proportional, Integral, and Derivative terms to automatically approach and maintain the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source. Figure 5.2, "RPM based Fan Control Algorithm" shows a simple flow diagram of the RPM based Fan Control Algorithm operation.

The desired tachometer count is set by the user inputting the desired number of 32.768KHz cycles that occur per fan revolution. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000 RPMs then the user would input the hexadecimal equivalent of 1312d (52_00h in the TACH Target Registers). This number represents the number of 32.768KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000RPMs (see Section 6.41, "TACH Target Registers" and Section 6.42, "TACH Reading Registers")

The EMC4002's RPM based Fan Control Algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a stalled/stuck fan condition while also asserting the ATF_INT# pin. The EMC4002 works with fans that operate up to 16,000 RPMs and provide a valid tachometer signal. The fan controller will function either with an externally supplied 32.768KHz clock source or with it's own internal 32KHz oscillator depending on the required accuracy.

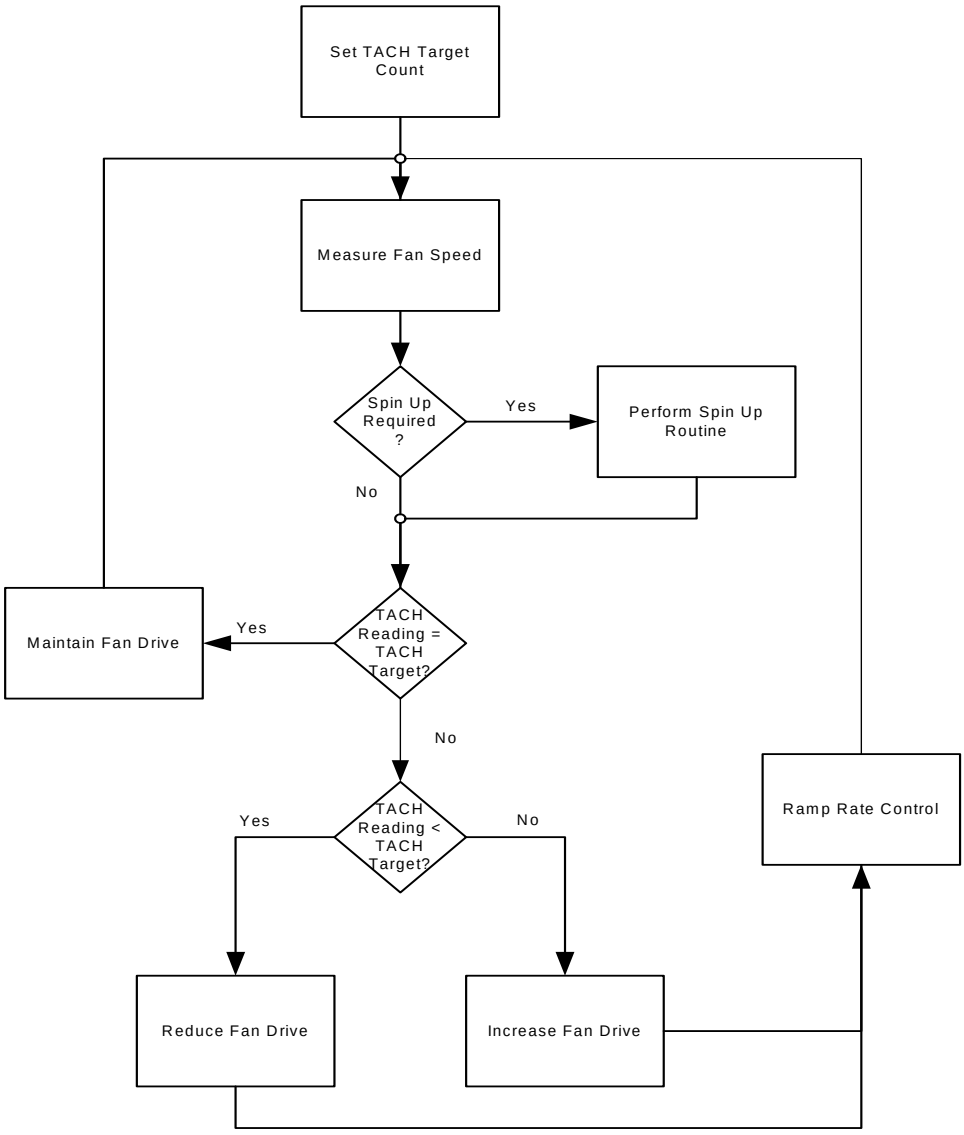

Figure 5.2 RPM based Fan Control Algorithm

5.5.1 Programming the RPM based Fan Control Algorithm

The RPM based Fan Control Algorithm powers-up disabled. The following registers control the algorithm. The EMC4002 fan control registers are pre-loaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

1. Program the GPIO Configuration Register for the desired operation on each pin. Disabling either TACH input will cause the RPM based Fan Control Algorithm to be disabled.
2. Set the Valid TACH Count Register to the minimum tachometer count that indicates the fan is spinning.
3. Set the Spin Up Configuration Register to the spin up level and Spin Time desired.
4. Set the Fan Step Register to the desired step size.

5. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
6. Set the Update Time, and Edges options in the Fan Configuration Register.
7. Set the TACH Target Register to the desired tachometer count.
8. Enable the RPM based Fan Control Algorithm by setting the EN_RPM bit.

5.5.2 Tachometer Measurement

In both modes of operation, the tachometer measurement operates independently of the mode of operation of the fan driver and RPM based Fan Speed Control algorithm. Any tachometer reading that is higher than the Valid TACH Count (see Section 6.39, "Valid TACH Count Registers") will flag a stalled fan and trigger an interrupt.

When measuring the tachometer, the fan must provide a valid tachometer signal at all times to ensure proper operation. The tachometer measurement circuitry is programmable to detect the fan speed of a variety of fan configurations and architectures including 1-pole, 2-pole (default), 3-pole, and 4-pole fans.

APPLICATION NOTE: The tachometer measurement works independently of the drive settings. If the device is put into manual mode and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the tachometer measurement may signal a Stalled Fan condition and assert an interrupt.

5.5.2.1 Stalled Fan

If the TACH Reading Register exceeds the user-programmable Valid TACH Count setting then it will flag the fan as stalled and trigger an interrupt. If the RPM based Fan Control Algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid tachometer level or is disabled.

The FAN_STALL Status bit indicates that a stalled fan was detected. This bit is checked conditionally depending on the mode of operation.

- Whenever the Manual Mode is enabled or whenever the drive value is changed from 00h, the FAN_STALL interrupt will be masked for the duration of the programmed Spin Up Time (see Table 6.51, "Spin Time") to allow the fan an opportunity to reach a valid speed without generating unnecessary interrupts.
- In Manual Mode, whenever the TACH Reading Register exceeds the Valid TACH Count Register setting, the FAN_STALL status bit will be set.
- When the RPM based Fan Control Algorithm, the stalled fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

5.5.3 Spin Up Routine

The EMC4002 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation. The Spin Up Routine is initiated under the following conditions:

1. The TACH Target High Byte Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Section 6.39).
2. The RPM based Fan Control Algorithm's measured tachometer reading is greater than the Valid TACH Count.
3. When in Manual Mode, the Drive Setting changes from a value of 00h.

When the Spin Up Routine is operating, the fan driver is set to full scale for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set a a user defined level (30% to 65% drive).

After the Spin Up Routine has finished, the EMC4002 measures the tachometer. If the measured tachometer reading is higher than the Valid TACH Count Register setting, the FAN_SPIN status bit is set and the Spin Up Routine will automatically attempt to restart the fan.

APPLICATION NOTE: When the device is operating in manual mode, the FAN_SPIN status bit may be set if the fan drive is set at a level that is lower than the fan can operate (excluding zero drive which disables the fan driver(s)). If the FAN_SPIN interrupt is unmasked, then this condition will trigger an errant interrupt.

Figure 5.3, "Spin Up Routine" shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

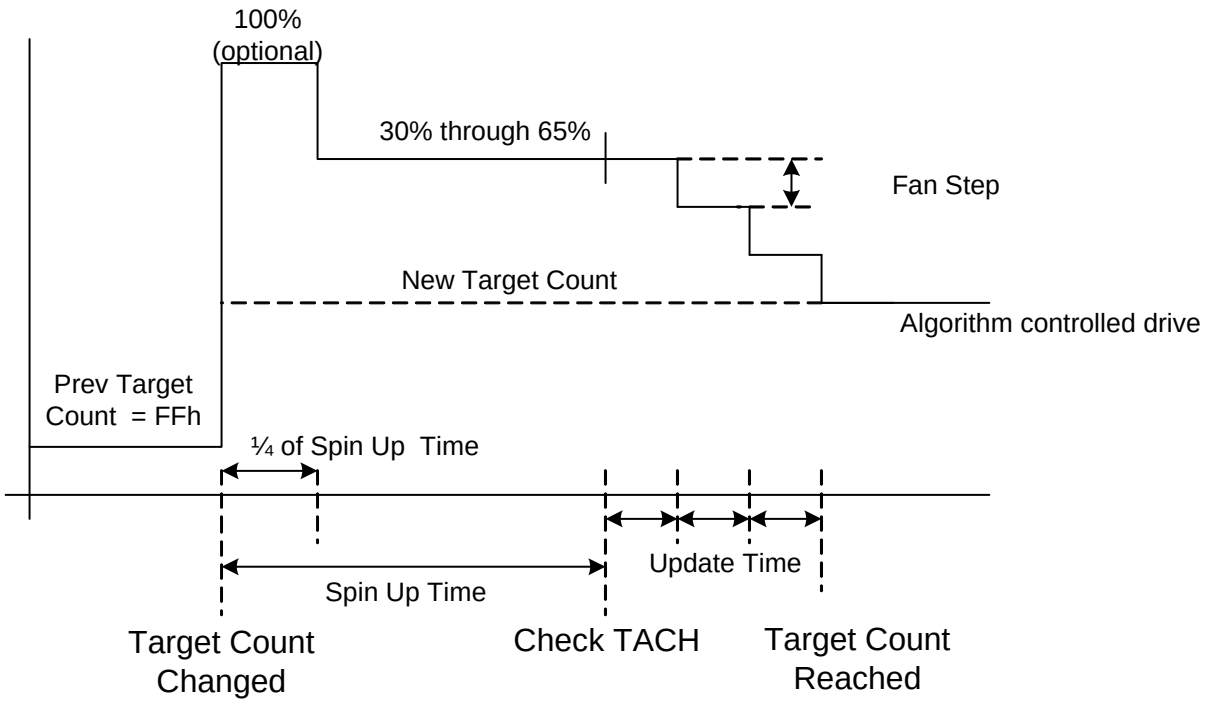

Figure 5.3 Spin Up Routine

5.5.4 32KHz Clock Source

The EMC4002 allows the user to choose between supplying an external 32.768KHz clock or use of the internal 32KHz oscillator to measure the tachometer signal. This clock source is used by the RPM based Fan Control Algorithm to calculate the current fan speed. This fan controller accuracy is directly proportional to the accuracy of the clock source.

5.6 Watchdog Timer

The EMC4002 contains an internal Watchdog Timer. Once the device has powered up the watchdog timer monitors the bus traffic for signs of activity. The Watchdog Timer starts whenever both the VDD_PWRGD and 3V_PWROK# signals are asserted.

If six (6) seconds elapse without the system host programming the device, then the following will occur:

1. The WATCH status bit will be set.
2. The High Side Fan Driver for Fan #1 will be set to full scale. If enabled, the High Side Fan Driver #2 will likewise be set to full scale.

APPLICATION NOTE: The PWM channels are not affected by the Watchdog (as the default operation for both PWM outputs is a GPIO).

The Watchdog Timer is disabled when the host device successfully uses the Write Data Byte protocol (for either SMBus or BC-Link) to write any data byte in the EMC4002. The target register does not need to be a defined register and no data needs to be changed. Simply receiving a write command will disable the Watchdog Timer. When it is disabled, the Fan Drivers return to their normal, default, operation.

If the Watchdog timer has been activated and either the VDD_PWRGD or 3V_PWROK# pins are deasserted then the Watchdog Timer will be stopped and reset. It will restart once the pins are properly asserted.

5.7 Dual Voltage Fan Drivers

The EMC4002 contains two Dual Voltage Fan Drivers with integrated pass devices. One is a dedicated fan driver and the other serves either as a secondary high side fan driver or as an LDO. This new feature biases the pass device from either a 3.3V supply (VDDL) or a 5V supply (VDDH) depending on the output voltage requirements. As the voltage level increases from 0V, the drive current is sourced from the 3.3V supply. This produces immediate power-saving benefits due to the lower voltage dropped across the pass device. When the output voltage reaches a threshold level of approximately 3V, the Dual Voltage Fan Driver seamlessly switches its sourcing supply to the 5V supply for increased drive up to 5V.

The Dual Voltage Fan Driver can source up to 600mA and is controlled by an internal 10 bit DAC that can be programmed to drive virtually any voltage from 0V to 5V.

5.7.1 Short Circuit Current Limit

The High Side Fan Driver contains circuitry to allow for significant overcurrent levels to accommodate transient conditions on the FAN pins. The overcurrent limit is dependent upon the output voltage with the limit dropping as the voltage nears 0V.

If the fan driver current detects a short-circuit condition for longer than 2 seconds, then the FANx_SHORT status bit is set and an interrupt generated. The TACH Target will be set to FF_F8h (which will disable the Fan Driver)

5.8 PWM Drivers

The EMC4002 contains two programmable 10-bit PWM drivers which can serve as part of the RPM based Fan Speed Control Algorithm or in Manual Mode. PWM drivers that are not used by the RPM based Fan Control Algorithm are configured as GPIO's.

When enabled, the PWM drivers can operate in four programmable frequency bands. The lower frequency bands offer frequencies in the range of 9Hz to 4.8kHz while the higher frequency options offer frequencies of 19.5kHz or 26kHz.

APPLICATION NOTE: The highest frequency available, 26kHz, operates in 8-bit resolution. All other PWM frequencies operate in 10-bit resolution.

5.9 Low Dropout Voltage Regulator

The EMC4002 contains a low dropout voltage regulator that is multiplexed with one of the two Dual Voltage Fan Drivers. The LDO can be configured to regulate a +3.3V output from a +5V source in addition to regulating a 2.5V output from a 3.3V source.

This voltage remains stable over current load up to 600mA and operates independently of the rest of the EMC4002 device. Figure 5.4 shows a general block diagram of the Low Dropout Voltage Regulator.

APPLICATION NOTE: The operation of the LDO is not controlled by registers within the EMC4002 device, however it still requires that VDD be present. If the VDD is removed, then the LDO output voltage will drop to 0V.

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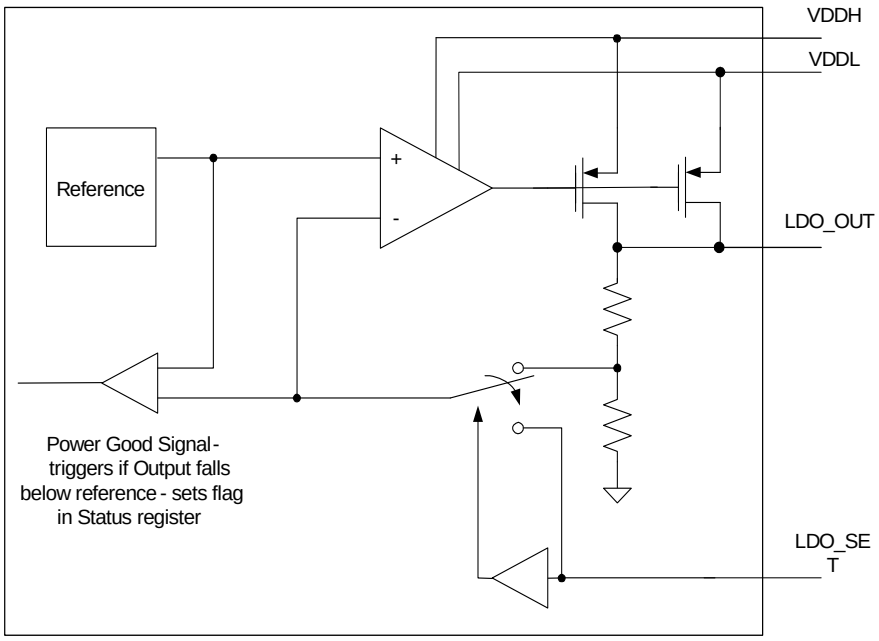

Figure 5.4 Block Diagram of Low Dropout Voltage Regulator

5.9.1 Power Control

The LDO, when configured as an LDO is enabled or disabled by the LDO_SHDN# pin. This pin is active low and when pulled to ground will cause the LDO to be disabled and the output voltage to be 0V.

5.9.2 Output Selection

The LDO output is selected at power up by the status of the LDO_SET pin as shown in Table 5.4, "LDO / Fan Driver Configuration Options".

At initial power up, the LDO / Dual Voltage Fan Driver is held off for 10ms after power up. After this time, the state of the LDO_SET pin is monitored and will determine the device operation.

Table 5.4 LDO / Fan Driver Configuration Options

VDDH	VDDL	LDO_SET	MODE / RATINGS
3.3V	3.3V	Ground	LDO, 2.5V fixed @600mA
3.3V	3.3V	Resistor Divider	LDO, 1.2-2.5V adjustable, @ 600mA (see Figure 5.5)
5V	5V	Pull-up to VDD	LDO, 3.3V fixed @ 400mA
5V	3.3V	Pull-up to VDDH2	Fan Driver enabled - 5V @ 600mA

When the LDO is configured to drive an output voltage other than 3.3V or 2.5V, then care must be taken that the power dissipation of the LDO is taken into account for the selected voltage levels. The maximum power dissipation for the LDO should be limited to 0.88W dropped internally. Refer to Application Note “Power and Layout Considerations for EMC4002”.

When the LDO is configured to operate as a 2nd Dual Voltage Fan Driver, it will be controlled as described in Section 5.7, "Dual Voltage Fan Drivers". In this configuration, the LDO_POK pin will be driven to a logic ‘0’ state. Any pull-up placed on this pin will cause current flow from VDDH.

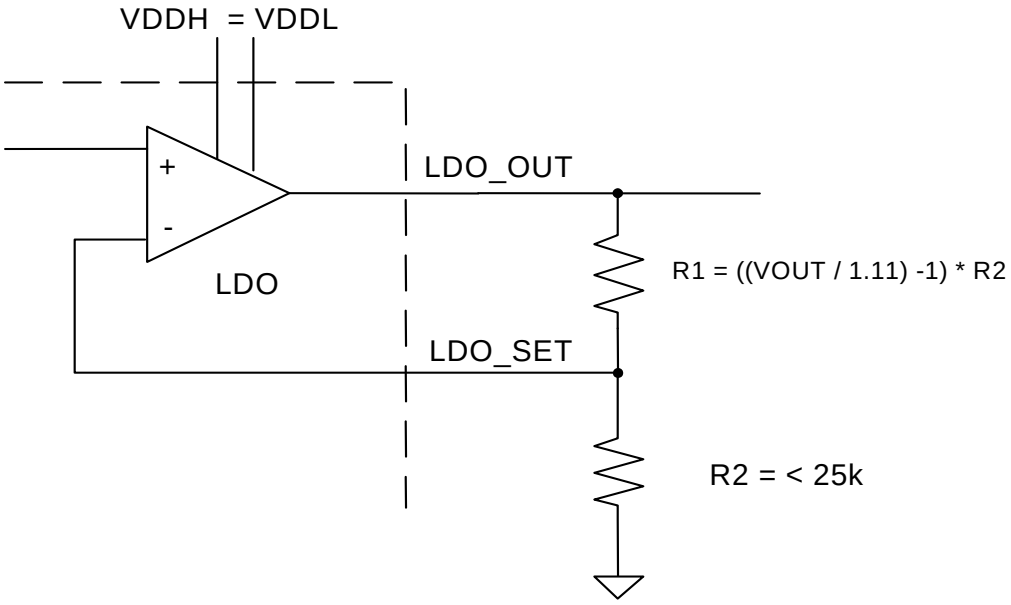

Figure 5.5 Adjustable LDO Output Configuration

5.9.3 Power OK

The LDO has an external signal called LDO_POK that is used by the LDO to indicate that the regulated voltage is within specified limits. The output voltage is constantly measured and compared against the internal reference. If the regulated voltage drops below 15%-20% of its nominal value, the LDO_POK pin will be driven low after a delay of approximately 50us and the status register will be updated.

In the event of a short circuit condition, or in the event of a Thermal Shutdown condition, this signal will be asserted low after a delay of approximately 50us and remain low while the condition remains in effect.

5.9.4 Short Circuit Condition

The LDO has internal circuitry that detects a short circuit condition. When a short circuit condition is detected (and the LDO is enabled), the LDO_POK will be asserted low and the LDO_SHORT bit will be set in the Status registers. If the interrupts are enabled for the LDO, this will cause the ATF_INT# pin to be asserted low. The LDO will be held off until the short circuit condition is removed and then returned to its normal operating condition.

5.10 Thermal Shutdown

The EMC4002 contains an internal Thermal Shutdown circuit. If the die temperature exceeds the shutdown threshold which is set at approximately 150°C then a Thermal Shutdown event has occurred. In the case of a Thermal Shutdown event, the TSD bit in both the Status register and the ThermTrip

status register will be set. If the Thermal Shutdown interrupt is not masked, then the ATF_INT# pin will be asserted low. In the case of a Thermal Shutdown, the LDO_POK signal will also be set low and the LDO will be disabled (if enabled).

The Thermal Shutdown will remain asserted until the die temperature drops below the threshold level minus the hysteresis (typical 50°C) at which point it will automatically be released.

APPLICATION NOTE: The Thermal Shutdown will NOT affect the fan driver. Therefore, if the Fan Driver is operating at a maximum power dissipation condition (2.5V out with high current drive), it is possible that it may cause the device to exceed the Thermal Shutdown limit. Because the Thermal Shutdown device does not control the fan driver, the user is responsible to ensure that the Fan Driver circuitry is disabled as necessary to prevent permanent damage to the device.

5.11 Voltage Monitors

The EMC4002 contains inputs for measuring the VDD voltage as well as voltages at VSET, VCP1 and VCP2. Additionally, the EMC4002 can be configured to measure inputs VIN1, and VIN2. The nominal value, range, and resolution of the input voltage channels is shown in Table 5.5, "Voltage Input Characteristics".

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Table 5.5 Voltage Input Characteristics

VOLTAGE INPUT	NOMINAL INPUT VOLTAGE	MAXIMUM INPUT VOLTAGE	RESOLUTION
VSET	600mV	800mV	3.125mV
VCP1	5V	6.66V	26.04mV
VCP2	5V	6.66V	26.04mV
VDD	3.3V	4.4V	17.18mV
VIN1	600mV	800mV	3.125mV
VIN2	600mV	800mV	3.125mV
THERM1	600mV	800mV	3.125mV

5.11.1 Input Attenuators

The VCP1, VCP2, and VDD voltage inputs contain attenuators that are used to bias the nominal voltage to 3/4 of full scale on the ADC. The total impedance on these attenuators is typically 300k Ohm and each contains a low pass filter with a cutoff frequency of approximately 140kHz.

The VSET, VIN1, and VIN2 inputs do not have attenuator inputs. Any voltage above the Maximum voltage will result in a full scale reading. The VIN1 pin has an input filter with a cutoff frequency of approximately 140kHz.

5.11.2 VCPx as Thermistor Input

As shown in Figure 5.1, "System Diagram for EMC4002", both VCPx input channels can be configured with an external thermistor to provide an inexpensive temperature monitor. A thermistor is a two-terminal resistor-style element that has a roughly linear relationship between its impedance and its temperature over a limited temperature range. Care should be taken such that the impedance of the external resistor divider is not influenced by the input resistance of the voltage attenuator on this input pin.

There is no special configuration required to read the thermistor. The EMC4002 converts the thermistor voltage to a digital voltage measurement but not to a temperature.

5.12 Temperature Monitors

The EMC4002 can monitor the temperature of up to nine (9) externally connected diodes as well as the internal or ambient temperature. Each channel is configured with the following features enabled or disabled based on user settings and system requirements.

5.12.1 Resistance Error Correction

The EMC4002 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of parasitic resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC4002 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

5.12.2 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. This correction is done my implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC4002 corrects for this beta variation to eliminate any error which would normally be induced. It automatically detects the appropriate beta setting to use.

5.13 Anti-Parallel Diode Support

Five of the external diode channels have alternate functions. External Diodes 3, 4 and 5 can be configured as Anti-Parallel Diodes, where the temperature of 2 diode-connected transistors can be read on a single DP/DN pair.

When enabled, the anti-parallel diode channels do not support CPU or GPU diodes that require the BJT or transistor models.

5.14 ADC/Thermistor Support on External Diode Lines

The External Diode 1 channel normally monitors a 2N3904 diode in the CPU well. The measured temperature is compared against the ThermTrip Temperature threshold determined by the V_{SET} voltage and SYS_SHDN# is asserted if it exceeds the set point.

To allow a longer trace run to the CPU well, the EMC4002 can also use a thermistor as the critical shutdown thermal sensor. This mode is selected by populating the correct pull-up resistor on the ADDR_MODE/XEN pin (see Table 4.1, "SMBus Address and Mode Selection"). The thermal sensor circuit options are illustrated in Figure 5.6, "Configurable Thermal Diode Channels". The resistor/thermistor divider voltage is driven out on DP1 when a measurement is made, and the voltage measurement is made on DN1. This reading can be capacitively filtered with a 0.1uF cap and is inherently averaged by the delta-sigma ADC so the results are very noise immune.

Additionally, the data measured on the DN1 / THERM pin will be automatically inverted (subtracted from FFh) prior to being loaded into the data registers.

The External Diode 6 channel can also be configured to measure a thermistor or generic voltage input. When the External Diode 1 and 6 channels are configured to measure a Thermistor voltage, the data can be inverted (subtracted from FFh) or not inverted based on user settings.

APPLICATION NOTE: When changing between measuring a diode and a thermistor the limit settings may cause invalid interrupts. It is recommended that the channels be disabled until the limits are properly configured.

APPLICATION NOTE: When configured to measure a thermistor on the External Diode 1 channel (see Appendix A), it is the users responsibility to set the VSET voltage to an appropriate level to emulate the desired threshold temperature. The EMC4002 will perform no calculations to translate the VSET voltage to an equivalent thermistor voltage. Additionally, high and low limits comparisons are not changed so the user should set the limits to appropriate values.

Thermistor and voltage monitoring configurations are illustrated in Figure 5.6, "Configurable Thermal Diode Channels"

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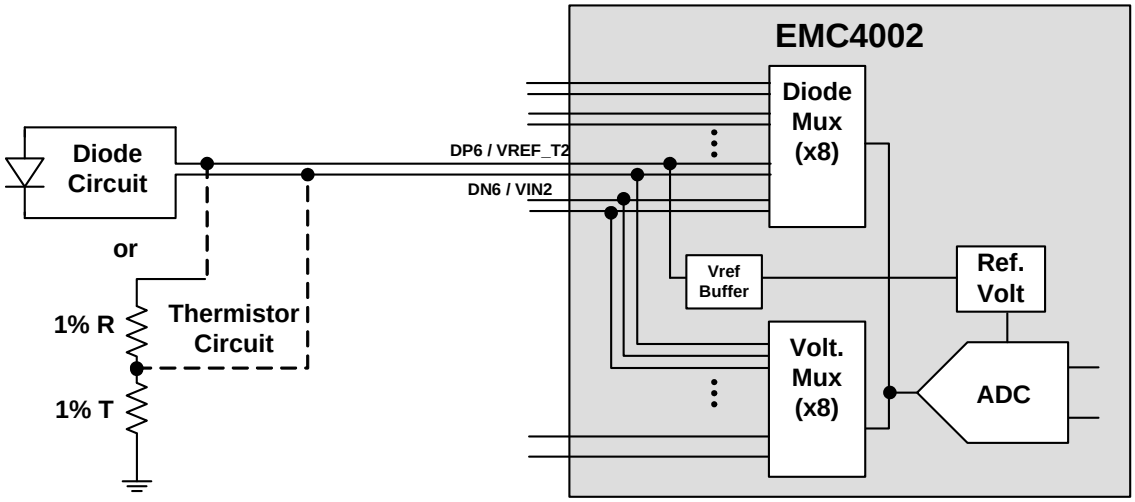

Figure 5.6 Configurable Thermal Diode Channels

This thermistor implementation eliminates three components used for calibration (N-FET, Resistor, GPIO) as well as software calibration overhead. The thermistor interface can be used for long trace runs in noisy environments. Accuracy of 2°C max. can be obtained using the components indicated in Figure 5.6.

Note: The Thermistor mode does not convert the ADC codes to temperature readings. Thermistor linearization, or a look up table, needs to be done in the EC if actual temperature values are required. See Appendix A "Thermistors".

5.15 Diode Connections

The external diode channels supports any diode connection shown below. The External Diode 2 - 6 channel settings can be modified at any time, however the External Diode 1 settings are fixed at power up based on the pull-up resistor setting of the ADDR_MODE / XEN pin as shown in Table 4.1, "SMBus Address and Mode Selection".

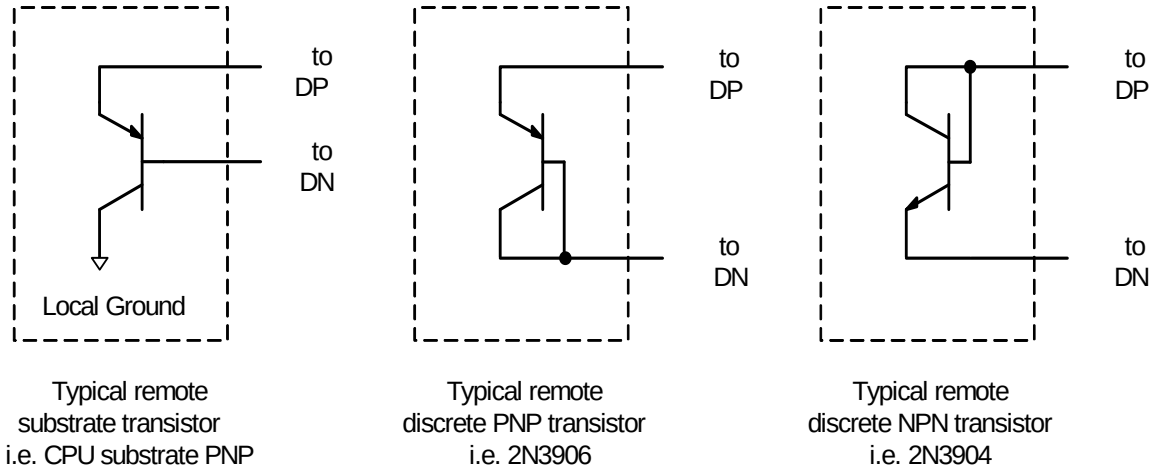

Figure 5.7 Diode Connections

5.15.1 Anti-Parallel Diode Capability

The EMC4002 has another unique technology available to allow 2 thermal diodes to share a single DP/DN temperature sensing pair. The “Anti-Parallel” circuit drives measurement currents alternately in opposite directions to measure first one, then the other diode. Because the diodes are reverse biased relative to each other, their temperatures can be measured independently. This arrangement can provide a very efficient pin usage. Figure 5.8, "Anti-Parallel Diode Configuration" illustrates the Anti-Parallel diode configuration.

See Application Note 16.4 “Using Anti-Parallel Diode (APD) with SMSC Temperature Sensors” for more information on using the Anti-Parallel Diode technology.

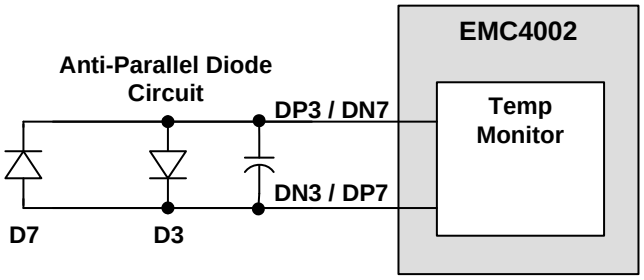

Figure 5.8 Anti-Parallel Diode Configuration

Note 5.1 This technique must not be used for CPU and GPU thermal diodes that require the BJT or transistor models

Note 5.2 It is recommended that the PCB layout includes capacitor footprints near the EMC4002 and near each thermal diode. The capacitors near the thermal diodes are normally not placed.

5.15.2 Diode Faults

The EMC4002 actively detects an open and short condition on each measurement channel. When a diode fault is detected, the temperature data MSByte is forced to a value of 80h and the FAULT bit is set in the Status Register. When the External Diode 3 channel is configured to operate in APD mode, the circuitry will detect independent open fault conditions, however a short condition will be shared between the External Diode 3 and External Diode 7 channels.

5.16 Voltage Programmable Fail-Safe Temperature Monitor

The Voltage Programmable Fail-Safe Temperature monitor provides thermal fail-safe detection without software intervention or programming. The voltage determined on the VSET input determines the logic threshold for the temperature measured by External Diode 1. Additionally, the output of the Voltage Programmable Fail-Safe Temperature Monitor provides a software independent interrupt and can be optionally configured to provide an SMBus Alert.

The Voltage Programmable Fail-Safe Temperature Monitor operates off of the VDD power supply.

5.16.1 VSET Pin

The EMC4002's VSET pin is an input to the ThermTrip block which sets the ThermTrip shutdown temperature. The system designer creates a voltage level at these input through a simple resistor connected to GND as shown in Figure 5.9, "Vset Circuit". The value of this resistor is used to create an input voltage on the TRIP_SET pin which is translated into a temperature ranging from 60°C to 123°C as enumerated in Table 5.6, "VSET Resistor Setting".

APPLICATION NOTE: VSET is designed to operate using a 1% resistor. If a 5% resistor is used, then the decoded temperature may have as much as 1C error.

APPLICATION NOTE: Note that an open condition on the VSET pin will be decoded as a minimum temperature threshold level.

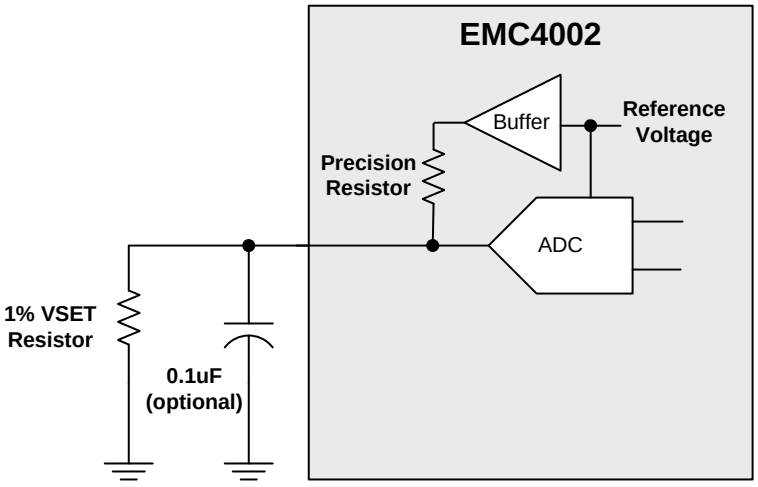

Figure 5.9 Vset Circuit

Table 5.6 VSET Resistor Setting

T_{TRIP} (°C)	RSET	T_{TRIP} (°C)	RSET
60	0.0	92	1240.0
61	28.7	93	1330.0
62	48.7	94	1400.0
63	69.8	95	1500.0
64	90.9	96	1580.0
65	113.0	97	1690.0
66	137.0	98	1820.0
67	158.0	99	1960.0
68	182.0	100	2050.0
69	210.0	101	2210.0
70	237.0	102	2370.0
71	261.0	103	2550.0
72	294.0	104	2740.0
73	324.0	105	2940.0
74	348.0	106	3160.0
75	383.0	107	3480.0
76	412.0	108	3740.0
77	453.0	109	4120.0
78	487.0	110	4530.0
79	523.0	111	4990.0
80	562.0	112	5490.0
81	604.0	113	6040.0
82	649.0	114	6810.0
83	698.0	115	7870.0
84	750.0	116	9090.0
85	787.0	117	10700.0
86	845.0	118	12700.0
87	909.0	119	15800.0
88	953.0	120	20500.0
89	1020.0	121	29400.0
90	1100.0	122	49900.0
91	1150.0	60	Open

5.16.2 Internal POWER_OK Signal

The internal POWER_OK signal is set to a logic ‘1’ when the 3V_PWROK# signal is asserted low (external pin) and the VDD_PWRGD signal is asserted high (external pin). If either pin changes state, the POWER_OK signal will be set to a logic ‘0’.

When the POWER_OK signal is set to a logical ‘0’, the ADC conversions will stop and the conversion cycle logic will reset. If the LPM bit is set, then the ADC conversions will continue to function normally. The inverted POWER_OK signal, INV_POWER_OK, is used to enable the ThermTrip logic block (see Section 5.17, "ThermTrip Logic Integration").

5.16.3 Internal HW_FAILSAFE# Signal

The HW_FAILSAFE# output from the Voltage Programmable Fail-Safe Temperature Monitor is a logical indicator of the temperature state of External Diode 1. HW_FAILSAFE# is an internal signal routed as an input to the ThermTrip logic.

Note that HW_FAILSAFE# is not available as an external pin, but when HW_FAILSAFE# is asserted, the HWFS bit in the FailSafe Status register is asserted.

The HW_FAILSAFE# output is set to logic ‘0’ when the External Diode 1 temperature exceeds the temperature threshold (T_P) established by the VSET input pin (as shown in Figure 5.10, "Example #1 of HW_FAILSAFE# Operation"). The HW_FAILSAFE# output is also asserted when the External Diode 1 temperature exceeds T_P minus 10°C during the first valid conversion cycle after POWER_OK is asserted (as shown in Figure 5.11, "Example #2 of HW_FAILSAFE# Operation").

Under normal operating conditions when the EMC4002 HW_FAILSAFE# output is asserted, the power supplies that affect POWER_OK are de-asserted, however the POWER_OK signal is not directly related to the status of the HW_FAILSAFE# signal.

The HW_FAILSAFE# output remains at a logic ‘1 level when the External Diode 1 temperature is less than T_P minus 10°C during the first valid conversion cycle after POWER_OK is asserted. Likewise, if the HW_FAILSAFE# output is asserted and the temperature drops below T_P, then it will be set to a logic ‘1’ state.

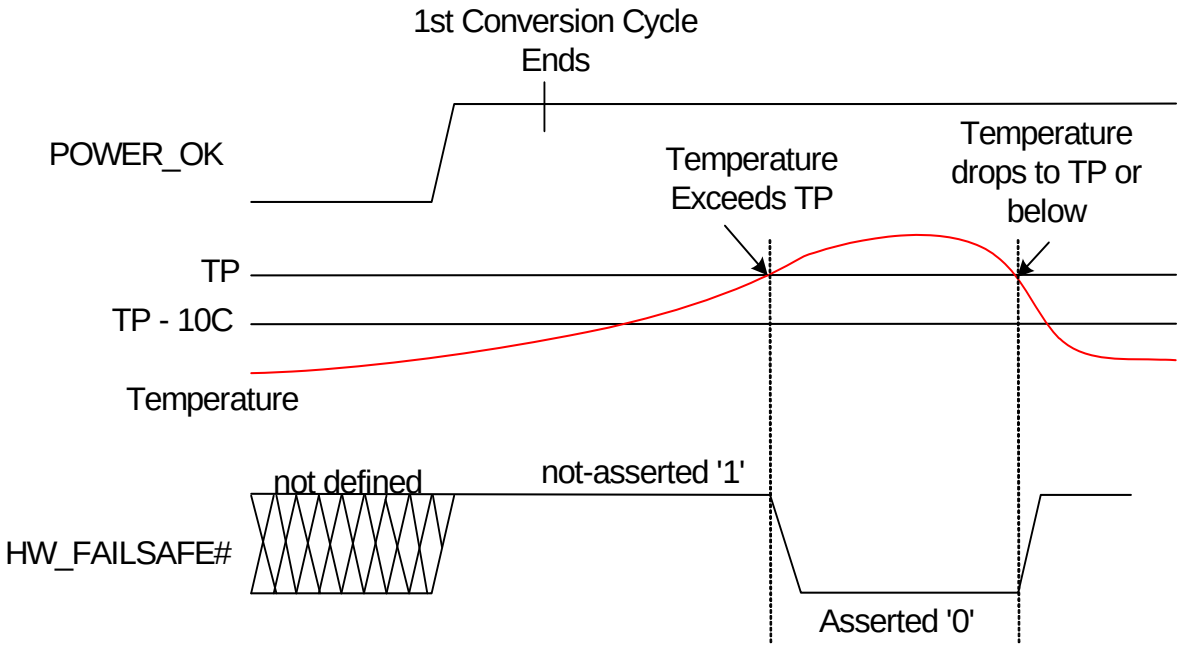

Figure 5.10 Example #1 of HW_FAILSAFE# Operation

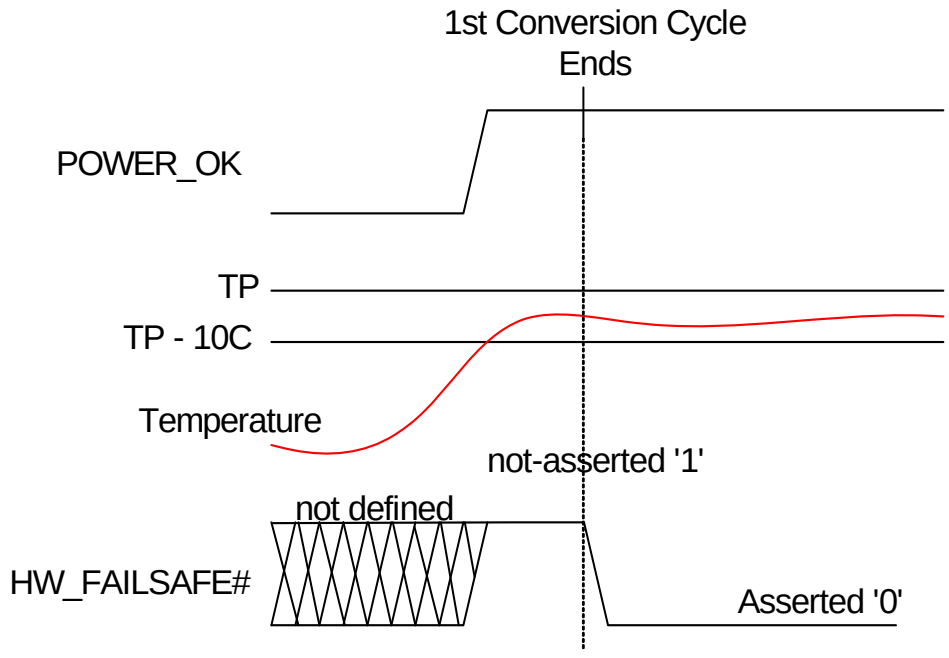

Figure 5.11 Example #2 of HW_FAILSAFE# Operation

5.17 ThermTrip Logic Integration

The EMC4002 includes the same ThermTrip logic integration that was used in the EMC4001 and EMC4000 devices. This logical integration uses the HW_FAILSAFE# and INV_POWER_OK signals (both internal signals based on the status of additional pins) in addition to the THERMTRIP1#, THERMTRIP2#, THERMTRIP3#, POWER_SW#, SYS_SHDN#, THERMTRIP_SIO, and ACAVAIL_CLR pins.

The THERMTRIP_SIO, SYS_SHDN#, and POWER_SW# signals are powered by the RTC_PWR3V supply. In addition, this supply signal powers all of the ThermTrip Logic integration as well an internal status register that indicates which of the inputs caused the outputs to be asserted.

The signal interaction is shown in Table 5.7, "ThermTrip Logic Functionality".

Table 5.7 ThermTrip Logic Functionality

INPUTS				CONTROL SIGNALS			OUTPUTS		
THERMTRIP1#	THERMTRIP2#	THERMTRIP3#	HW_FAILSAFE# (INT)	INV_POWER_OK (INT)	POWER_SW#	ACAVAIL_CLR	THERMTRIP _SIO	SYS_SHDN#	DESCRIPTION
X	X	X	X	1	1	0	no change	no change	Power is not supplied. ThermTrip Inputs and HW_FAILSAFE# are ignored and outputs remain unchanged
1	1	1	1	0	1	0	no change	no change	Power is supplied, but the Inputs are de-asserted. The outputs latch so that they do not change state.
0	X	X	X	0	1	0	1	0	Power is supplied. Any of the inputs asserting to ‘0’ causes the outputs to be asserted.
X	0	X	X						
X	X	0	X						
X	X	X	0						
X	X	X	X	X	1 -> 0	X	0	1	The POWER_SW# and ACAVAIL_CLR pins acts as a reset for the logic block - both pins generate a short duration pulse when asserted so that holding either pin in the asserted state (‘0’ for POWER_SW# or ‘1’ for ACAVAIL_CLR) will not permanently disable the ThermTrip logic block.
X	X	X	X	X	X	0 -> 1			

5.17.1 POWER_SW# Pin

The POWER_SW# pin is used in the ThermTrip logic integration as a reset input for the circuitry. In order to prevent a device from holding the POWER_SW# low and effectively holding the ThermTrip logic inactive, the POWER_SW# pin has some special logic added to it that generates a short duration (~1 clock pulse) reset pulse that is triggered on the falling edge of the POWER_SW# pin.

5.17.2 ACAVAIL_CLR Pin

The ACAVAIL_CLR pin, like the POWER_SW# pin, is used by the ThermTrip logic integration as a reset input for the circuitry. In order to prevent a device from holding the ACAVAIL_CLR pin high and effectively holding the ThermTrip logic inactive, the ACAVAIL_CLR pin has some special logic added to it that generates a short duration (~1 clock pulse) reset pulse that is triggered on the rising edge of the ACAVAIL_CLR pin.

5.18 General Purpose I/Os

The EMC4002 contains five (5) shared general purpose I/O pins. They can be configured as either input pins or output pins. When they are configured as inputs, each GPIO can be configured to assert the ATF_INT# pin if its input is changed.

When they are configured as outputs, each GPIO can be configured as an open drain or push-pull style.

All of the GPIO pins are multiplexed with other functions and may not be available depending on the system configuration.

5.19 Alerts and Limits

Figure 5.12, "Temperature Channel Interrupt Flow" and Figure 5.13, "Other Channel Interrupt Flow" show the interactions of the interrupts for temperature channels, voltage channels, LDO, Fan driver, and GPIO's.

The EMC4002 contains both high and low limits for all temperature channels and both high and low limits for VIN1, VCP1, VCP2, VDD, and VIN2 (muxed with DN6). If the corresponding channel exceeds these limits (by either being too high or too low), then the ATF_INT# pin will be asserted low (if enabled). If an external diode detects a diode fault then the ATF_INT# pin will be asserted low (if enabled).

Likewise, if either Dual Voltage Fan Driver detects a short circuit condition, the LDO detects a short circuit condition or de-asserts the LDO_POK, or a thermal shutdown event occurs, then the ATF_INT# pin will be asserted low (if enabled).

All of these interrupts can be masked from updating the Status Registers individually or globally. If any bit of either Status register are set, then the ATF_INT# pin will be asserted low provided that the TEMP (or VOLT) bits and INTEN bit are set accordingly.

The Status register will be updated only if the individual status enable bits are set. Once a status bit has been set, it will remain set until the Status register is read (and the error condition has been removed).

The ATF_INT# pin will be set if the individual status enable bits are set, the 'group' enable bit is set (TEMP, VOLT, or GPIO) and the INTEN bit is set. If the interrupt pin be asserted, it will be cleared immediately if any of these bits are cleared.

The Voltage Programmable Fail-Safe Temperature Monitor can be masked from asserting the ATF_INT# pin low, however it will always affect the ThermTrip logic block normally.

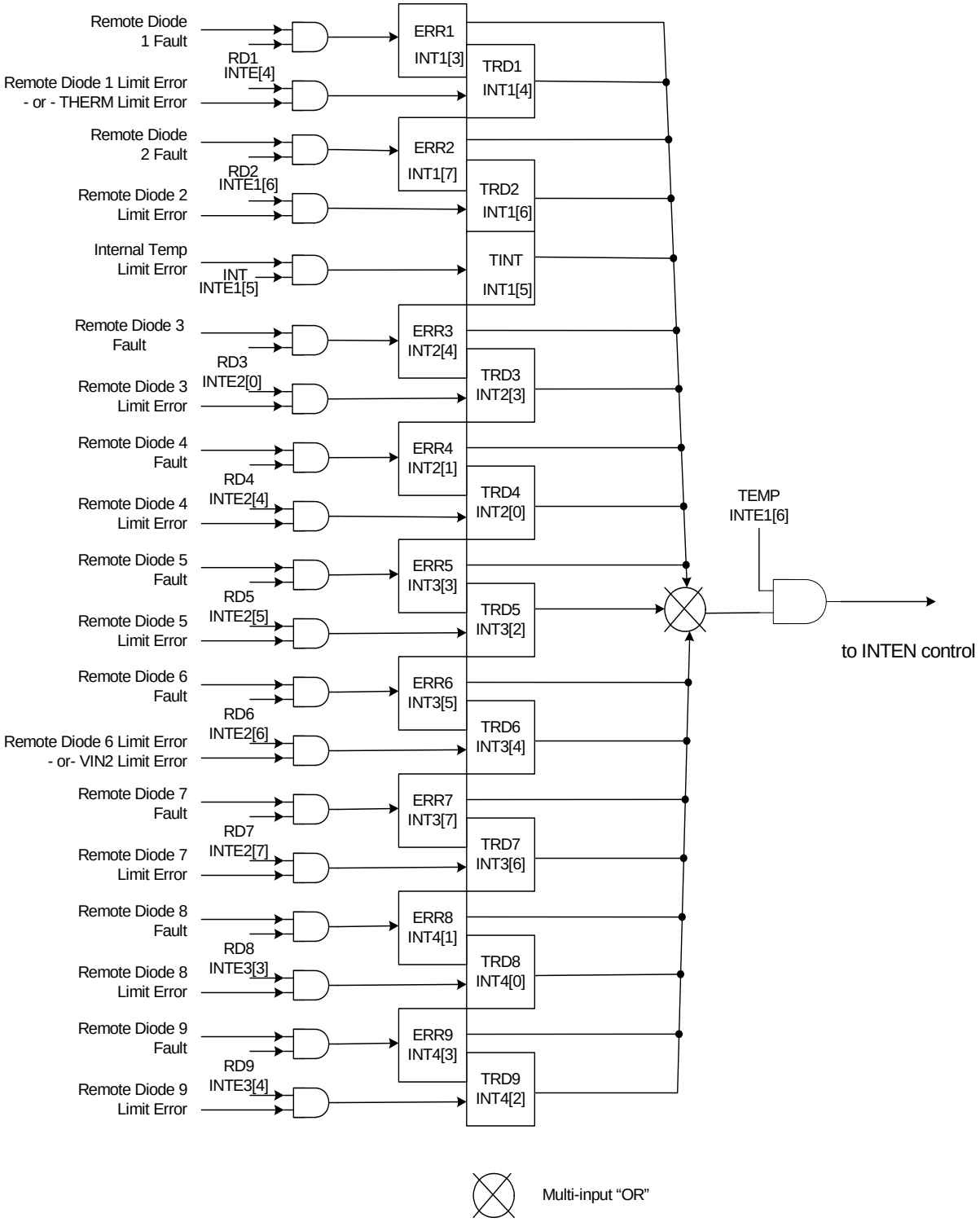

Figure 5.12 Temperature Channel Interrupt Flow

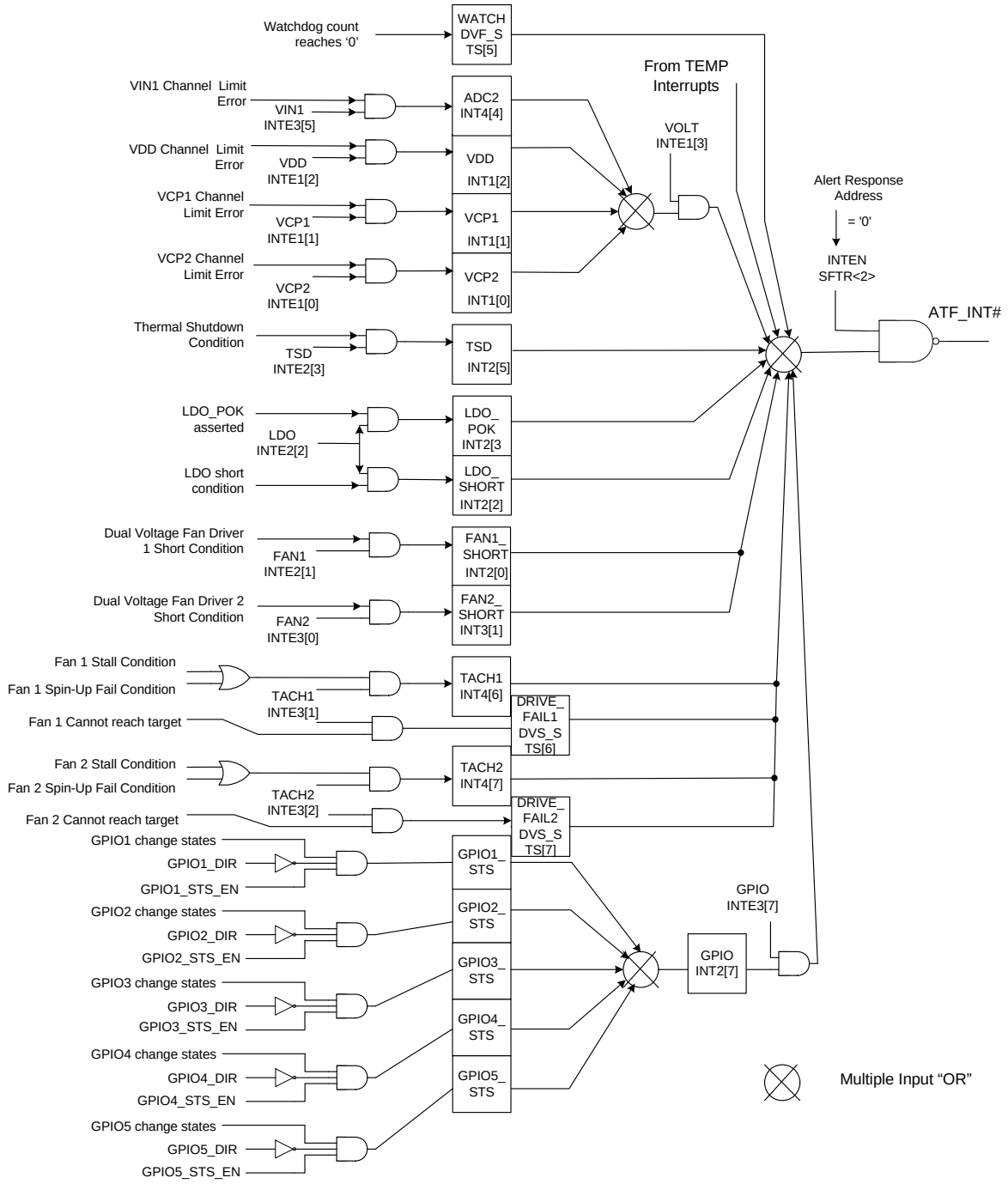

Figure 5.13 Other Channel Interrupt Flow

5.20 Multiple Supply Considerations

Because the EMC4002 contains multiple power domains and power supply inputs, there is the potential for power-coupling between them. The device operates off of five power domains: VDD, RTC_PWR3V, VDDL2 / VDDH2 (LDO), VDDL / VDDH. These power domains interact as shown in Figure 5.14, "Power Supply Domains for EMC4002".

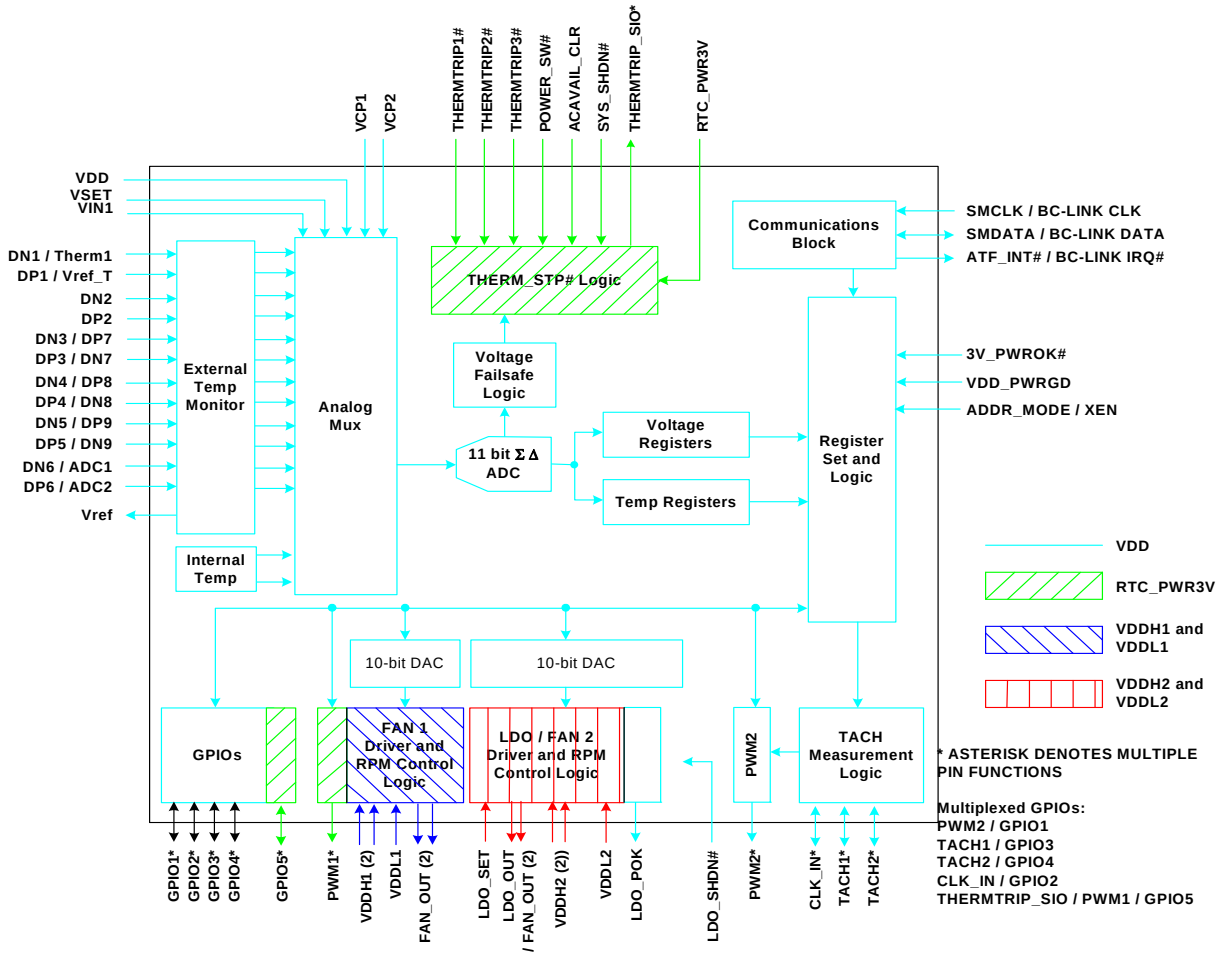

Figure 5.14 Power Supply Domains for EMC4002

The majority of the circuitry functions from the VDD power supply input. It is important to note that the LDO requires the Reference to be operational to function properly. Similarly, the Dual Voltage Fan Driver requires both the Reference and 10-bit DAC to be operational to function properly (both of which are powered from VDD). Therefore, if the VDD power supply is removed from the chip, these features will not operate.

Ideally, all the power supplies will be powered simultaneously. If this is not the case, then the power supply inputs should be powered up in the following order:

1. RTC_PWR3V
2. VDD
3. VDDH
4. VDDL

The Power-On-Reset (POR) circuitry operates off of the VDD power supply so that, in the event that this supply fails, all digital registers will be reset. The exception to this is the ThermTrip Status register and which is reset only when the CFS in the Special Function Registers is asserted to ‘1’. The other exception is the ThermTrip Config Register which is reset on the RTC_PWR3V Power on Reset.

Chapter 6 Register Set

6.1 Register Map

The following registers are accessible through the SMBus Interface.

Table 6.1 EMC4002 Register Set

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
00h	R	External Diode 1 Temperature Low Byte	Stores fractional data for External Diode 1	00h	No	page 59
01h	R	Internal Temperature Low Byte	Stores fractional data for the Internal Diode (used to measure T_{DIE})	00h	No	page 59
02h	R	External Diode 2 Temperature Low Byte	Stores the Fractional data for External Diode 2	00h	No	page 59
03h	R	External Diode 3 Temperature Low Byte	Stores the Fractional data for External Diode 3	00h	No	page 59
04h	R	External Diode 4 Temperature Low Byte	Stores the fractional data for External Diode 4	00h	No	page 59
05h	R	External Diode 5 Temperature Low Byte	Stores the fractional data for External Diode 5	00h	No	page 59
06h	R	External Diode 6 Temperature Low Byte	Stores the fractional data for External Diode 6	00h	No	page 59
07h	R	External Diode 7 Temperature Low Byte	Stores the fractional data for External Diode 7	00h	No	page 59
08h	R	External Diode 8 Temperature Low Byte	Stores the fractional data for External Diode 8	00h	No	page 59
09h	R	External Diode 9 Temperature Low Byte	Stores the fractional data for External Diode 9	00h	No	page 59
0Eh	R	VIN 1 Voltage	Stores the voltage Measured on VIN1 channel	FFh	No	page 61
20h	R	GPIO Status	Stores the Status bits of which GPIO changed states	00h	No	page 62
21h	R	VCP1 Voltage Reading	Stores the VCP1 Voltage Monitor data	FFh	No	page 61
22h	R	VDD Voltage Reading	Stores the VDD Voltage Monitor data	FFh	No	page 61
23h	R	VCP2 Voltage Reading	Stores the VCP2 Voltage Monitor data	FFh	No	page 61

Table 6.1 EMC4002 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
25h	R	External Diode 1 Temp Reading High Byte	Stores the integer data of External Diode 1 or the Thermistor Input if enabled (THERM)	00h	No	page 59
26h	R	Internal Diode Temp Reading High Byte	Stores the integer data of the Internal Diode (used to measure T_{DIE}.)	00h	No	page 59
27h	R	External Diode 2 Temp Reading High Byte	Stores the integer data of External Diode 2	00h	No	page 59
28h	R	External Diode 3 Temp Reading High Byte	Stores the Integer data of External Diode 3	00h	No	page 59
29h	R	External Diode 4 Temp Reading High Byte	Stores the Integer data of External Diode 4	00h	No	page 59
2Ah	R	External Diode 5 Temp Reading High Byte	Stores the Integer data of External Diode 5	00h	No	page 59
2Bh	R	External Diode 6 Temp Reading High Byte	Stores the Integer data of External Diode 6 or the VIN2 data if enabled.	00h	No	page 59
2Ch	R	External Diode 7 Temp Reading High Byte	Stores the Integer data of External Diode 7	00h	No	page 59
2Dh	R	External Diode 8 Temp Reading High Byte	Stores the Integer data of External Diode 8	00h	No	page 59
2Eh	R	External Diode 9 Temp Reading High Byte	Stores the Integer data of External Diode 9	00h	No	page 59
Configuration and Control						
2Fh	R/W	Configuration	Controls the temperature channels and power modes	00h	SWL	page 63
30h	R/W	GPIO Config	Configures whether GPIO1 - 5 are enabled	05h	SWL	page 64
31h	R/W	GPIO Direction	Configures the direction of GPIOs 1-5	00h	SWL	page 65
32h	R/W	GPIO Output Config	Configures the output type of GPIOs 1-5	00h	SWL	page 65
33h	R	GPIO Input	Stores the input state of each GPIO	00h	No	page 66
34h	R/W	GPIO Output	Sets the output state of each GPIO output	00h	No	page 66
35h	R/W	GPIO Interrupt Enable	Configures whether each GPIO input flags an interrupt if it changes states	00h	SWL	page 66
36h	R/W	Dual Voltage Fan Config	Configures advanced features of both Dual Voltage Fan Drivers	00h	SWL	page 67
37h	R	Dual Voltage Status	Indicates status of Dual Voltage Fan Driver 1 and 2	00h	No	page 68

Table 6.1 EMC4002 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
Ideality and Beta Configuration						
38h	R/W	External Diode 2 Beta Configuration	Configures the beta compensation settings for External Diode 2	10h	SWL	page 69
39h	R/W	External Diode 3 Beta Configuration	Configures the beta compensation settings for External Diode 3	10h	SWL	page 69
3Bh	R/W	External Diode 2 Ideality Configuration	Sets the Ideality Factor that applies to External Diode 2	12h	SWL	page 70
3Ch	R/W	External Diode 3 Ideality Configuration	Sets the Ideality Factor that applies to External Diode 3	12h	SWL	page 70
3Dh	R/W	PWM Configuration	Controls the base PWM frequencies	0Fh	SWL	page 71
Revision Control						
3Eh	R	Company ID	Stores the company ID	5Dh	No	page 72
3Fh	R	Version/Stepping	Stores the revision information	00h	No	page 72
40h	R/W	Lock Start	Enables the software lock functionality and give status of the monitoring functionality.	01h	SWL	page 73
Interrupt Status						
41h	R-C	Interrupt Status Register 1	Stores the status bits for the Internal Diode, External Diode 1, External Diode 2, and Voltage channels	00h	No	page 73
42h	R-C	Interrupt Status Register 2	Stores the status bits for the External Diode 3 channel as well as the LDO, Dual Voltage Fan Driver, Thermal Shutdown, and GPIO inputs	00h	No	page 73
43h	R	ThermTrip Pin State	Stores the pin state of the THERTRIPx# pins, the POWER_SW#, and ACAVAIL_CLR pins	00h	No	page 75
44h	R-C	Interrupt Status Register 3	Stores the status bits for the External Diode 4, through External Diode 7	00h	No	page 73
45h	R-C	Interrupt Status Register 4	Stores the status bits for External Diode 8 and 9, the VIN1 and 2 inputs, and the TACH inputs	00h	No	page 73
Limit Registers						
46h	R/W	VCP1 Low Limit	Low limit for VCP1 Voltage Monitor	00h (0V)	SWL	page 76
47h	R/W	VCP1 High Limit	High limit for VCP1 Voltage Monitor	FFh (6.5V)	SWL	page 76
48h	R/W	VDD Low Limit	Low Limit for VDD Voltage Monitor	00h (0V	SWL	page 76
49h	R/W	VDD High Limit	High Limit for VDD Voltage Monitor	FFh (4.44V)	SWL	page 76
4Ah	R/W	VCP2 Low Limit	Low limit for VCP2 Voltage Monitor	00h (0V)	SWL	page 76
4Bh	R/W	VCP2 High Limit	High limit for VCP2 Voltage Monitor	FFh (6.5V)	SWL	page 76

Table 6.1 EMC4002 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
4Ch	R/W	VIN 1 Low Limit	Low Limit for VIN 1 Input Channel	00h (0V)	SWL	page 76
4Dh	R/W	VIN 1 High Limit	High Limit for VIN 1 Input Channel	FFh (800mV)	SWL	page 76
4Eh	R/W	External Diode 1 Temp Low Limit	Low limit for External Diode 1	81h (-127°C)	SWL	page 76
4Fh	R/W	External Diode 1 Temp High Limit	High limit for External Diode 1	7Fh (+127°C)	SWL	page 76
50h	R/W	Internal Temp Low Limit	Low limit for the Internal Diode	81h (-127°C)	SWL	page 76
51h	R/W	Internal Temp High Limit	High limit for the Internal Diode	7Fh (127°C)	SWL	page 76
52h	R/W	External Diode 2 Temp Low Limit	Low limit for External Diode 2	81h (-127°C)	SWL	page 76
53h	R/W	External Diode 2 Temp High Limit	High limit for External Diode 2	46h (+70°C)	SWL	page 76
54h	R/W	External Diode 3 Temp Low Limit	Low limit for External Diode 3	81h (-127°C)	SWL	page 76
55h	R/W	External Diode 3 Temp High Limit	High limit for External Diode3	7Fh (127°C)	SWL	page 76
56h	R/W	External Diode 4 Temp Low Limit	Low limit for External Diode 4	81h (-127°C)	SWL	page 76
57h	R/W	External Diode 4 Temp High Limit	High limit for External Diode 4	7Fh (127°C)	SWL	page 76
58h	R/W	External Diode 5 Temp Low Limit	Low limit for External Diode 5	81h (-127°C)	SWL	page 76
59h	R/W	External Diode 5 Temp High Limit	High limit for External Diode 5	7Fh (127°C)	SWL	page 76
5Ah	R/W	External Diode 6 Temp Low Limit	Low limit for External Diode 6	81h (-127°C)	SWL	page 76
5Bh	R/W	External Diode 6 Temp High Limit	High limit for External Diode 6	7Fh (127°C	SWL	page 76
5Ch	R/W	External Diode 7 Temp Low Limit	Low limit for External Diode 7	81h (-127°C)	SWL	page 76
5Dh	R/W	External Diode 7 Temp High Limit	High limit for External Diode 7	7Fh (127°C	SWL	page 76
5Eh	R/W	External Diode 8 Temp Low Limit	Low limit for External Diode 8	81h (-127°C)	SWL	page 76
5Fh	R/W	External Diode 8 Temp High Limit	High limit for External Diode 8	7Fh (127°C	SWL	page 76
60h	R/W	External Diode 9 Temp Low Limit	Low limit for External Diode 9	81h (-127°C)	SWL	page 76

Table 6.1 EMC4002 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
61h	R/W	External Diode 9 Temp High Limit	High limit for External Diode 9	7Fh (127°C)	SWL	page 76
External Diode 4 - 9 Beta Configuration						
64h	R/W	External Diode 4 Beta Configuration	Configures the beta compensation settings for External Diode 4	10h	SWL	page 69
65h	R/W	External Diode 5 Beta Configuration	Configures the beta compensation settings for External Diode 5	10h	SWL	page 69
66h	R/W	External Diode 6 Beta Configuration	Configures the beta compensation settings for External Diode 6	10h	SWL	page 69
70h	R/W	REC Enable Register	Enables REC for all external diode channels	FFh	SWL	page 78
Misc. Registers						
71h	R	VSET Voltage Reading	Stores the VSET Voltage Monitor reading	FFh	No	page 61
72h	R/W	PWM 1 Divide	Sets the final divide ratio for the PWM 1 output (when enabled)	28h (40d)	SWL	page 78
73h	R/W	PWM 2 Divide	Sets the final divide ratio for the PWM 2 output (when enabled)	28h (40d)	SWL	page 78
75h	R	Thermal Trip Temperature	Stores the calculated ThermTrip temperature high limit derived from the voltage on VSET and compared against External Diode 1.	7Fh	No	page 79
76h	R	FailSafe Status	Stores the status bits that indicate which ThermTrip input condition caused the outputs (SYS_SHDN# and THERMTRIP_SIO) to be asserted.	00h	No	page 79
77h	R/W	FailSafe Config	Stores configuration bits that are retained over all power modes	00h	SWL	page 80
7Ah	R	Error Debug Register	Stores the status bits that indicate the type of SMBus Errors	00h	No	page 80
7Ch	R/W	Special Function Register	Controls the global interrupt enable bit and the bit that resets the FailSafe Status register	04h	No	page 81
7Dh	R/W	Interrupt Status Enable 2	Controls whether the LDO, Dual Voltage Fan Driver, Thermal Shutdown, External Diode 3, External Diode 4 - 7 may update the corresponding status registers	00h	SWL	page 81
7Eh	R/W	Interrupt Status Enable 1	Controls whether any voltage channel and any temperature channel may assert an interrupt if set. Also enables whether the Internal Diode, External Diode 1, External Diode 2, or voltage channels may update the corresponding status registers.	C0h	SWL	page 81

Table 6.1 EMC4002 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
7Fh	R/W	Interrupt Status Enable 3	Controls whether External Diode channels 8 - 9, tachometer measurement circuitry, Fan 2, GPIO, or VIN 1 and 2 channels may update the corresponding status registers (or ATF_INT# pin)	00h	SWL	page 81
Fan 1 Control						
80h	R/W	Fan 1 Setting Low Byte	Always displays the most recent fan driver input setting for Fan 1. If the RPM based Fan Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	page 83
81h	R/W	Fan 1 Setting High Byte		00h	No	
82h	R/W	Fan 1 Configuration 1	Sets configuration values for the RPM based Fan Control Algorithm for Fan 1	2Bh	No	page 84
83h	R/W	Fan 1 Configuration 2	Sets additional configuration values for the Fan 1 driver	34h	SWL	page 85
84h	R/W	Gain 1	Holds the gain terms used by the RPM based Fan Control Algorithm for Fan 1	2Ah	SWL	page 88
85h	R/W	Fan 1 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 1 driver	19h	SWL	page 88
86h	R/W	Fan 1 Step	Sets the maximum change per update for Fan 1	10h	SWL	page 90
87h	R/W	Fan 1 Minimum Drive	Sets the minimum drive value for the Fan 1 driver	66h	SWL	page 91
88h	R/W	Fan 1 Valid TACH Count	Holds the minimum tachometer value that indicates the fan is spinning properly	F5h	SWL	page 91
89h	R/W	Fan 1 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	page 92
8Ah	R/W	Fan 1 Drive Fail Band High Byte		00h	SWL	
8Bh	R/W	TACH 1 Target Low Byte	Holds the target tachometer count for Fan 1	F8h	No	page 92
8Ch	R/W	TACH 1 Target High Byte		FFh	No	
8Dh	R	TACH 1 Reading High Byte	Holds the tachometer count for Fan 1	FFh	No	page 93
8Eh	R	TACH 1 Reading Low Byte		F8h	No	
Fan 2 Control						
90h	R/W	Fan 2 Setting Low Byte	Always displays the most recent fan driver input setting for Fan 2. If the RPM based Fan Control Algorithm is disabled, allows direct user control of the fan driver.	00h	No	page 83
91h	R/W	Fan 2 Setting High Byte		00h	No	
92h	R/W	Fan 2 Configuration 1	Sets configuration values for the RPM based Fan Control Algorithm for Fan 2	2Bh	No	page 84

Table 6.1 EMC4002 Register Set (continued)

ADDR	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	LOCK	PAGE
93h	R/W	Fan 2 Configuration 2	Sets additional configuration values for the Fan 2 driver	34h	SWL	page 85
94h	R/W	Gain 2	Holds the gain terms used by the RPM based Fan Control Algorithm for Fan 2	2Ah	SWL	page 88
95h	R/W	Fan 2 Spin Up Configuration	Sets the configuration values for Spin Up Routine of the Fan 2 driver	19h	SWL	page 88
96h	R/W	Fan 2 Step	Sets the maximum change per update for Fan 2	10h	SWL	page 90
97h	R/W	Fan 2 Minimum Drive	Sets the minimum drive value for the Fan 2 driver	66h	SWL	page 91
98h	R/W	Fan 2 Valid TACH Count	Holds the minimum tachometer value that indicates the fan is spinning properly	F5h	SWL	page 91
99h	R/W	Fan 1 Drive Fail Band Low Byte	Stores the number of Tach counts used to determine how the actual fan speed must match the target fan speed at full scale drive	00h	SWL	page 92
9Ah	R/W	Fan 1 Drive Fail Band High Byte		00h	SWL	
9Bh	R/W	TACH 2 Target Low Byte	Holds the target tachometer count for Fan 2	F8h	No	page 92
9Ch	R/W	TACH 2 Target High Byte		FFh	No	
9Dh	R	TACH 2 Reading High Byte	Holds the tachometer count for Fan 2	FFh	No	page 93
9Eh	R	TACH 2 Reading Low Byte		F8h	No	
FDh	R	Product ID	Stores the unique Product ID	13h	No	page 94

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

6.1.1 Lock Entries

The Lock Column describes the locking mechanism, if any, used for individual registers. All SWL registers are Software Locked and therefore made read-only when the LOCK bit is set in the RLS Register (40h).

6.2 Data Read Interlock

The data read interlock mechanism used on all temperature data, voltage data, tach reading, and PWM setting registers works as follows. When the High byte is read, the corresponding low byte is copied into internal ‘shadow’ registers. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from a specific channel high byte will automatically refresh this stored low byte data.

When writing to the tach and PWM setting registers (such as PWM setting, Min PWM Setting, Valid TACH Count, TACH Target), writing to the high byte register will cause the data to be accepted. For

these registers, if the full resolution is to be used, the low byte should be loaded prior to the high byte being written.

6.2.1 Programming the Limit Registers

The Limit and configuration registers can be updated at any time before the SWL bit is asserted (LOCK bit in RLS register 40h). To avoid erroneous alerts during this process, the following steps are recommended.

1. Disable interrupts - write a '0' to the INTEN bit in the Special Function Register (INTEN bit, register 7Ch).
2. Clear Status bits - read all Status registers to clear any errant bits.
3. Clear all Status Interrupt Enable bits.
4. Load Limit and/or configuration values into appropriate registers.
5. Enable interrupts - write a '1' to the INTEN bit and enable all desired interrupt channels in the Interrupt Enable registers (7Dh, 7Eh, 7Fh).

6.3 Temperature Data Registers

Table 6.2 Temperature Data Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
25h	External Diode 1 High Byte	Sign	64	32	16	8	4	2	1	No	00h
	Thermistor Data (when enabled)	128	64	32	16	8	4	2	1	No	00h
00h	External Diode 1 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h
26h	Internal Temp High Byte	Sign	64	32	16	8	4	2	1	No	00h
01h	Internal Temp Low Byte	0.5	-	-	-	-	-	-	-	No	00h
27h	External Diode 2 High Byte	Sign	64	32	16	8	4	2	1	No	00h
02h	External Diode 2 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h
28h	External Diode 3 High Byte	Sign	64	32	16	8	4	2	1	No	00h
03h	External Diode 3 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h

Table 6.2 Temperature Data Registers (continued)

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
29h	External Diode 4 High Byte	Sign	64	32	16	8	4	2	1	No	00h
04h	External Diode 4 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h
2Ah	External Diode 5 High Byte	Sign	64	32	16	8	4	2	1	No	00h
05h	External Diode 5 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h
2Bh	External Diode 6 High Byte	Sign	64	32	16	8	4	2	1	No	00h
	VIN2 (if enabled)	128	64	32	16	8	4	2	1	No	00h
06h	External Diode 6 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h
2Ch	External Diode 7 High Byte	Sign	64	32	16	8	4	2	1	No	00h
07h	External Diode 7 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h
2Dh	External Diode 8 High Byte	Sign	64	32	16	8	4	2	1	No	00h
08h	External Diode 8 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h
2Eh	External Diode 9 High Byte	Sign	64	32	16	8	4	2	1	No	00h
09h	External Diode 9 Low Byte	0.5	0.25	0.125	-	-	-	-	-	No	00h

As shown in Table 6.2, "Temperature Data Registers", each temperature monitor has two byte wide data registers. The 11 bit data temperature is stored aligned to the left resulting in the High Byte to contain temperature in 1°C steps and the Low Byte to contain fractions of a degree. The temperature format is shown below. The '-' entries represent bits are not part of the measured data and will be read as a logic '0'.

Table 6.3 Temperature Data Format

TEMPERATURE (°C)	2'S COMPLEMENT FORMAT		2'S COMPLEMENT FORMAT	
	BINARY (11-BIT)	HEX (11-BIT)	BINARY (9-BIT)	HEX (9-BIT)
Diode Fault	1000 0000 000- ----b	80 00h	1000 0000 0--- ----b	80 00h
<= -63.875	1100 0000 001- ----b	C0 20h	1100 0000 0--- ----b	C0 00h
-63	1100 0001 000- ----b	C1 00h	1100 0001 0--- ----b	C1 00h
-1	1111 1111 000- ----b	FF 00h	1111 1111 0--- ----b	FF 00h
0	0000 0000 000- ----b	00 00h	0000 0000 0--- ----b	00 00h
0.125	0000 0000 001- ----b	00 20h	0000 0000 0--- ----b	00 00h
1	0000 0001 000- ----b	01 00h	0000 0001 0--- ----b	01 00h
63	0011 1111 000- ----b	3F 00h	0011 1111 0-- ----b	3F 00h
64	0100 0000 000- ----b	40 00h	0100 0000 0--- ----b	40 00h
65	0100 0001 000- ----b	41 00h	0100 0001 0--- ----b	41 00h
126	0111 1110 000- ----b	7E 00h	0111 1110 0--- ----b	7E 00h
127	0111 1111 000- ----b	7F 00h	0111 1111 0--- ----b	7F 00h
>=127.875	0111 1111 111- ----b (Note 6.1)	7F E0h	0111 1111 1--- ----b (Note 6.1)	7F 80h

Note 6.1 All temperatures above 127.875°C will be reported as 127.875°C.

If the LDO and/or high side fan drivers are active, then self-heating of the large current drive devices will affect the internal temperature reading. Therefore, it is not recommended that the Internal temperature channel be used to monitor the ambient air temperature.

When the External Diode 1 channel is configured to operate in Thermistor mode, the External Diode 1 High Byte is loaded with the measured voltage of the thermistor circuit instead of temperature data.

When the External Diode 6 channel is configured to operate in voltage mode (i.e. the VIN2 channel is enabled), the External Diode 6 High Byte is loaded with the measured voltage of the DN6 / VIN2 pin instead of temperature data.

6.4 Voltage Data Registers

Table 6.4 Voltage Data Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
0Eh	VIN1	7	6	5	4	3	2	1	0	No	FFh
21h	VCP1	7	6	5	4	3	2	1	0	No	FFh
22h	VDD	7	6	5	4	3	2	1	0	No	FFh
23h	VCP2	7	6	5	4	3	2	1	0	No	FFh
71h	VSET	7	6	5	4	3	2	1	0	No	FFh

The voltage data registers hold measured values of the voltage input channels. The resolution of the data is dependent upon which channel is being measured as shown in Section 5.11, "Voltage Monitors". The data is displayed in a binary form with 00h corresponding to 0V in and FFh corresponding to the an input that is equal to or greater than the maximum voltage.

The channels are configured so that the nominal voltage will equal 3/4 of full scale (high byte = C0h output). See Table 6.5, "Voltage Data Format Example".

Table 6.5 Voltage Data Format Example

INPUT CHANNEL	INPUT VOLTAGE	DATA READING	
		BINARY	HEX
VSET / VIN 1 / VIN 2 / THERM (600mv nominal)	0V	0000 0000b	00h
	600mV	1100 0000b	C0h
	800mV	1111 1111b	FFh
VCP1 / VCP2 (5V nominal)	0V	0000 0000b	00h
	3.3V	0111 1101b	7Dh
	5.0V	1100 0000b	C0h (3/4 full scale)
	6.66V	1111 1111	FFh
VDD (3.3V nominal)	0V	0000 0000b	00h
	2.5V	1010 0010b	A2h
	3.3V	1100 0000b	C0h (3/4 full scale)
	4.4V	1111 1111b	FFh

6.5 GPIO Status Register

Table 6.6 GPIO Status Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
20h	GPIO Status	-	-	-	GPIO5_STS	GPIO4_STS	GPIO3_STS	GPIO2_STS	GPIO1_STS	No	00h

The GPIO Status Register reports which GPIO changed states. Each bit is set when the corresponding GPIO input changes states (and is enabled). If the corresponding GPIO is not configured as an input or if the corresponding GPIO interrupt is disabled, then the bit will not change states. Whenever a bit is set in this register, the GPIO status bit (Bit 7 - Interrupt Status 2 Register).

All bits are cleared when the register is read.

6.6 Configuration Register

Table 6.7 Configuration Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
2Fh	Config	VIN2_ INV	VIN2EN	APD5	APD4	APD3	AVG_ EN	CONV[1:0]		SWL	00h

The Configuration Register controls the basic functionality of the EMC4002. The bits are described below.

Bit 7 - VIN2_INV - Determines whether the VIN2 channel data is inverted.

- '0' (default) - The VIN2 channel data is not inverted.
- '1' - The VIN2 channel data is inverted. The data presented to the reading registers and compared against the limits is determined as FFh - the measured input voltage.

Bit 6 - VIN2_EN - Enables the VIN2 channel and the VREF_T2 reference output.

- '0' (default) - The DN6 / VIN2 and DP6 / VREF_T2 pins are used for the External Diode 6 channel.
- '1' - The DN6 / VIN2 pin is used as a voltage input (VIN2). The DP6 / VREF_T2 pin is used as a reference voltage. When enabled, the current flow from the reference voltage is available only when the VIN1 and VIN2 are being actively measured. At all other times, the current will be disabled.

Bit 5 - APD5 - Enables anti-parallel diode technology on the DP5 / DN9 and DN5 / DP9 pins.

- '0' (default) - The anti-parallel diode technology is disabled. The DP5 / DN9 and DN5 / DP9 pins will be used only for the External Diode 5 channel. Any diode type (CPU, GPU, or diode connected transistor) can be connected to these pins.
- '1' -The anti-parallel diode technology is enabled. The DP5 / DN9 and DN5 / DP9 pins will be used for both the External Diode 5 and the External Diode 9 channels. The two diodes are connected in an ant-parallel fashion and only diode-connected transistors are supported for each diode.

Bit 4 - APD4 - Enables anti-parallel diode technology on the DP4 / DN8 and DN4 / DP8 pins.

- '0' (default) - The anti-parallel diode technology is disabled. The DP4 / DN8 and DN4 / DP8 pins will be used only for the External Diode 4 channel. Any diode type (CPU, GPU, or diode connected transistor) can be connected to these pins.
- '1' -The anti-parallel diode technology is enabled. The DP4 / DN8 and DN4 / DP8 pins will be used for both the External Diode 4 and the External Diode 8 channels. The two diodes are connected in an ant-parallel fashion and only diode-connected transistors are supported for each diode.

Bit 3 - APD3 - Enables anti-parallel diode technology on the DP3 / DN7 and DN3 / DP7 pins.

- '0' (default) - The anti-parallel diode technology is disabled. The DP3 / DN7 and DN3 / DP7 pins will be used only for the External Diode 3 channel. Any diode type (CPU, GPU, or diode connected transistor) can be connected to these pins.
- '1' -The anti-parallel diode technology is enabled. The DP3 / DN7 and DN3 / DP7 pins will be used for both the External Diode 3 and the External Diode 7 channels. The two diodes are connected in an ant-parallel fashion and only diode-connected transistors are supported for each diode.

Bit 2 - AVG_EN - enables software averaging.

- '0' (default) - digital averaging is not enabled
- '1' - digital averaging is enabled and both the External Diode 1 and External Diode 2 temperature channels will be put into four stage running average. The temperature will continue to be updated after every conversion based on the average of the previous four measurement values

Bit 1-0 - CONV<1:0> - determine the temperature conversion rate that is used. The following table shows the temperature conversion rates available.

Table 6.8 Temp Conversion Rate

CONV<1:0>		CONVERSION RATE
0	0	Continuous (approximately 4 Conversions / sec). (default)
0	1	1 conversion / sec
1	0	2 conversions / sec.
1	1	Reserved

6.7 GPIO Configuration Register

Table 6.9 GPIO Config Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
30h	GPIO Config	-	-	-	-	GPIO5_ CFG	GPIO4_ CFG	GPIO3_ CFG	GPIO2_ CFG	SWL	05h

The GPIO Configuration Register controls the pin function of the multi-function GPIO pins.

Bits 3 - GPIO5_CFG- Determines the pin function of the THERMTRIP_SIO / PWM1 / GPIO5 pin.

- '0' (default) - The THERMTRIP_SIO / PWM1 / GPIO5 pin is configured to operate as a THERMTRIP_SIO output.
- '1' - The THERMTRIP_SIO / PWM1 / GPIO5 pin is configured to operate as either a PWM or a GPIO as determined by the FAN1 / PWM1 bit in the Fan 1 Configuration 2 register.

Bit 2 - GPIO4_CFG - Determines the pin function of the TACH2 / GPIO4 pin.

- '0' - The TACH2 / GPIO4 pin is configured to act as a tachometer input for Fan 2.
- '1' (default) - The TACH2 / GPIO4 pin is configured to act as a GPIO. Setting this bit will force the RPM based Fan Control Algorithm for Fan 2 to be disabled (the circuitry requires a tachometer input to function properly).

Bit 1 - GPIO3_CFG - Determines the pin function of the TACH1 / GPIO3 pin.

- '0' (default) - The TACH1 / GPIO3 pin is configured to act as the tachometer input for Fan 1.
- '1' - the TACH1 / GPIO3 pin is configured to act as a GPIO. Setting this bit will force the RPM based Fan Control Algorithm for Fan 1 to be disabled (the circuitry requires a tachometer input to function properly).

Bit 0 - GPIO2_CFG - Determines the pin function of the CLK_IN / GPIO2 pin.

- '0' - The CLK_IN / GPIO2 pin is configured to act as the external clock input for the tachometer measurement circuitry.
- '1' (default) - The CLK_IN / GPIO2 pin is configured to act as a GPIO. The tachometer measurement circuitry will use the internal clock at a reduced accuracy.

6.8 GPIO Direction Register

Table 6.10 GPIO Config Register 2

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
31h	GPIO Direction	-	-	-	GPIO5_ DIR	GPIO4_ DIR	GPIO3_ DIR	GPIO2_ DIR	GPIO1_ DIR	SWL	00h

The GPIO Direction Register controls the direction of all GPIOs that are enabled as GPIOs. If a pin is not configured as a GPIO, then the corresponding bit is ignored.

Bit 4 - GPIO5_DIR - Determines the direction of GPIO5.

- '0' (default) - GPIO5 is configured as an input.
- '1' - GPIO5 is configured as an output.

Bit 3 - GPIO4_DIR - Determines the direction of GPIO4.

Bit 2 - GPIO3_DIR - Determines the direction of GPIO3.

Bit 1 - GPIO2_DIR - Determines the direction of GPIO2.

Bit 0 - GPIO1_DIR - Determines the direction of GPIO1.

6.9 GPIO Output Config Register

Table 6.11 GPIO Config Register 2

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
32h	GPIO Output Config	-	-	-	GPIO5_ OT	GPIO4_ OT	GPIO3_ OT	GPIO2_ OT	GPIO1_ OT	SWL	00h

The GPIO Direction Register controls the output type of all GPIOs configured as outputs. If a pin is not configured as a GPIO or as an output, then the corresponding bit is ignored.

Bit 4 - GPIO5_OT - Determines the output type of GPIO5 when configured as an output.

- '0' (default) - GPIO5 is configured as an open-drain output.
- '1' - GPIO5 is configured as a push-pull output.

Bit 3 - GPIO4_OT - Determines the output type of GPIO4 when configured as an output.

Bit 2 - GPIO3_OT - Determines the output type of GPIO3 when configured as an output.

Bit 1 - GPIO2_OT - Determines the output type of GPIO2 when configured as an output.

Bit 0 - GPIO1_OT - Determines the output type of GPIO1 when configured as an output.

6.10 GPIO Data Registers

Table 6.12 GPIO Data Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
33h	GPIO Input Register	-	-	-	GPIO5_ IN	GPIO4_ IN	GPIO3_ IN	GPIO2_ IN	GPIO1_ IN	No	00h
34h	GPIO Output Register	-	-	-	GPIO5_ OUT	GPIO4_ OUT	GPIO3_ OUT	GPIO2_ OUT	GPIO1_ OUT	No	00h

The GPIO Data Register holds the input and output data of the GPIO pins. The GPIOx_IN bits will always reflect what is on the GPIO pin. The GPIOx_OUT bits are used to program the output level of the pins. GPIO's that are configured as inputs will ignore the value in the GPIOx_OUT bits. Those that are configured as outputs will reflect the value of the GPIOx_OUT bits on the next digital clock cycle.

6.11 GPIO Interrupt Enable Register

Table 6.13 GPIO Mask Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
35h	GPIO Interrupt Enable Register	-	-	-	GPIO5_ INT_ EN	GPIO4_ INT_ EN	GPIO3_ INT_ EN	GPIO2_ INT_ EN	GPIO1_ INT_ EN	SWL	00h

The GPIO Interrupt Enable Register determines whether a GPIO channel configured as an input asserts the GPIO_STS bit when its value changes states. If the GPIO Interrupt is enabled, whenever the GPIO input changes states (from '0' to '1' or from '1' to '0'), it will cause the corresponding GPIO_STS bit to be set. If the GPIO channels are configured as outputs, the corresponding bits are ignored.

Bit 4 - GPIO5_INT_EN - determines whether GPIO 5 will assert the status bit when it changes state.

- '0' (default) - GPI0 5 will not cause an interrupt.
- '1' - whenever GPI0 5 is configured as an input and changes states, it will set the GPIO bit in the status register and trigger an interrupt (assuming that the INTEN bit is set).

Bit 3 - GPIO4_INT_EN - determines whether GPIO 4 will assert the status bit when it changes state.

Bit 2 - GPIO3_INT_EN - determines whether GPIO 3 will assert the status bit when it changes state.

Bit 1 - GPIO2_INT_EN - determines whether GPIO 2 will assert the status bit when it changes state.

Bit 0 - GPIO1_INT_EN - determines whether GPIO 1 will assert the status bit when it changes state.

6.12 Dual Voltage Fan Configuration Register

Table 6.14 Dual Voltage Fan Configuration Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
36h	DVF Config	-	-	FAN_ RATING2	5V_ EN2	3V_ EN2	FAN_ RATING1	5V_ EN1	3V_ EN1	SWL	00h

The Dual Voltage Fan Configuration Register controls advanced functionality of the Dual Voltage Fan Driver. These bits are ignored if the Fan Driver is configured as a PWM. Likewise, the FAN_RATING2, 5V_EN2, and 3V_EN2 bits are ignored if the Dual Voltage Fan Driver 2 circuitry is configured to operate as an LDO.

Bit 5 - FAN_RATING2 - sets the expected maximum current to be delivered to the FAN 2.

- '0' (default) - the maximum current expected for Fan 2 is less than 300mA.
- '1' - the maximum current expected for Fan 2 is greater than 300mA.

APPLICATION NOTE: The FAN_RATING bits adjust the trip point on the FAN_OUT pins only when in normal operation mode (as shown in Table 6.15). If using a high current fan (300-600mA) then set this bit to '1'.

Bit 4 - 5V_EN2 - along with 3V_EN configures which of the Dual Voltage pass devices are active as shown in Table 6.15.

Bit 3 - 3V_EN2 - along with 5V_EN configures which of the Dual Voltage pass devices are active as shown in Table 6.15.

Bit 2 - FAN_RATING1 - sets the expected maximum current to be delivered to the FAN 1.

- '0' (default) - the maximum current expected for Fan 1 is less than 300mA.
- '1' - the maximum current expected for Fan1 is greater than 300mA.

Bit 1 - 5V_EN1 - along with 3V_EN configures which of the Dual Voltage pass devices are active as shown in Table 6.15.

Bit 0 - 3V_EN1 - along with 5V_EN configures which of the Dual Voltage pass devices are active as shown in Table 6.15.

Table 6.15 5V_EN and 3V_EN Decode

5V_EN	3V_EN	DUAL VOLTAGE FAN DRIVER FUNCTION
0	0	Normal operation - supply current will be drawn from most efficient supply based on programmed output voltage (default)
1	0	The 5V Pass device will supply all supply current from the VDDH supply
0	1	The 3.3V Pass will supply all supply current from the VDDL supply.
1	1	Normal operation - supply current will be drawn from most efficient supply based on programmed output voltage

APPLICATION NOTE: The 3.3V Pass device should only be enabled using the 3V_EN bit if the fan voltage will never exceed 3.3V and the Fan current will never exceed 300mA.

APPLICATION NOTE: If the EMC4002 is configured with the 3.3V Pass device enabled, then the FAN_RATING bit should be set to maximize power efficiency. Additionally, the Fan Setting Registers will be capped at a value of 3Fh (3/4 full scale).

6.13 Dual Voltage Fan Status Register

Table 6.16 Dual Voltage Fan Status Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
37h	DVF Status	DRIVE_ FAIL2	DRIVE_ FAIL1	WATCH	-	POK2	3V_ DRIVE2	POK1	3V_ DRIVE1	No	00h

The Dual Voltage Fan Status Register indicates the current operating condition of the Dual Voltage Fan Drivers. These status bits are set to ‘0’ if the corresponding Dual Voltage Fan Driver is disabled.

Bit 7 - DRIVE_FAIL2 - Indicates that the RPM based Fan Speed Control Algorithm cannot drive Fan 2 to the desired target setting at maximum drive. If this bit is set and enabled, then it will cause the ATF_INT# pin to be asserted. This bit is sticky and will be cleared when read if the error condition has been removed.

- ‘0’ - The RPM based Fan Speed Control Algorithm can drive Fan 2 to the desired target setting.
- ‘1’ - The RPM based Fan Speed Control Algorithm cannot drive Fan 2 to the desired target setting at maximum drive.

Bit 6 - DRIVE_FAIL1 - Indicates that the RPM based Fan Speed Control Algorithm cannot drive Fan 1 to the desired target setting at maximum drive. If this bit is set and enabled, then it will cause the ATF_INT# pin to be asserted. This bit is sticky and will be cleared when read if the error condition has been removed.

- ‘0’ - The RPM based Fan Speed Control Algorithm can drive Fan 1 to the desired target setting.
- ‘1’ - The RPM based Fan Speed Control Algorithm cannot drive Fan 1 to the desired target setting at maximum drive.

Bit 5 - WATCH - Indicates that the Watchdog Timer has timed out and set the fans on full. If this bit is set, then it will cause the ATF_INT# pin to be asserted. This bit cannot be masked (though the ATF_INT# pin can be masked using the INTEN bit). This bit will be cleared when read.

- ‘0’ - The Watchdog Timer has not reached its full count of 6 seconds or has been disabled by writing to any data byte.
- ‘1’ - The Watchdog Timer has reached its full count of 6 seconds and turned both fan drivers on full.

Bit 3 - POK2 - Indicates that the Dual Voltage Fan Driver 2 output voltage matches the programmed output voltage.

- ‘0’ - the Dual Voltage Fan Driver output voltage does not match the programmed output voltage. This bit may be set to ‘0’ because the Fan voltage is ramping to the desired voltage based on a programmed change. Alternately, this bit may be set by a short-circuit condition (which will assert the FAN_SHORT bit in Interrupt Status Register 2).
- ‘1’ - the Dual Voltage Fan Driver 2 output voltage matches the programmed output voltage.

Bit 2 - 3V_DRIVE2 - Indicates which of the pass devices in the Dual Voltage Fan Driver 2 is currently active and providing current to the Fan. This bit will be set to ‘0’ if the Dual Voltage Fan Driver 2 is configured as an LDO.

- ‘0’ - the 5V pass device is active and providing current to Fan 2.
- ‘1’ - the 3.3V pass device is active and providing current to Fan 2.

Bit 1 - POK1 - Indicates that the Dual Voltage Fan Driver 1 output voltage matches the programmed output voltage.

- '0' - the Dual Voltage Fan Driver output voltage does not match the programmed output voltage. This bit may be set to '0' because the Fan voltage is ramping to the desired voltage based on a programmed change. Alternately, this bit may be set by a short-circuit condition (which will assert the FAN_SHORT bit in Interrupt Status Register 2).
- '1' - the Dual Voltage Fan Driver output voltage matches the programmed output voltage.

Bit 0 - 3V_DRIVE1 - Indicates which of the pass devices in the Dual Voltage Fan Driver 1 is currently active and providing current to the Fan.

- '0' - the 5V pass device is active and providing current to Fan 1.
- '1' - the 3.3V pass device is active and providing current to Fan 1.

6.14 Beta Configuration Registers

Table 6.17 Beta Configuration Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
38h	External Diode 2 Beta Configuration	-	-	-	AUTO2	BETA2[3:0]				SWL	10h
39h	External Diode 3 Beta Configuration	-	-	-	AUTO3	BETA3[3:0]				SWL	10h
64h	External Diode 4 Beta Configuration	-	-	-	AUTO4	BETA4[3:0]				SWL	10h
65h	External Diode 5 Beta Configuration	-	-	-	AUTO5	BETA5[3:0]				SWL	10h
66h	External Diode 6 Beta Configuration	-	-	-	AUTO6	BETA6[3:0]				SWL	10h

The Beta Configuration Registers hold a value that corresponds to a range of betas that the Beta Correction circuitry can compensate for. The Beta Configuration Registers activate the Beta Compensation circuitry if any value besides '1111' is written.

When the Beta Compensation circuitry is disabled, the diode channels will function with default current levels and will not automatically adjust for beta variation. They will still support the Ideality Configuration and the Resistance Error Correction Features.

Bit 4 - AUTOx - Enables the automatic beta circuitry. This circuitry automatically detects the optimal beta settings to be used for each external diode as it is measured.

- '0' - The automatic beta detection circuitry is disabled. The BETAx[3:0] bits will directly control the beta setting used. Writing to these bits will change the beta setting for the appropriate channel starting with the next conversion.
- '1' (default) - The automatic beta detection circuitry is enabled. The circuitry will automatically select the optimal beta settings for the connected diode. The BETAx[3:0] bits will be updated to reflect the current settings used. Writing to these bits will have no affect on the temperature measurement and the data will not be stored.

Bits 3 - 0 - BETAx[3:0] - These bits represent the current settings of the beta compensation circuitry. when the automatic beta detection circuitry is enabled, they are automatically updated based on the current settings. When the automatic beta detection circuitry is disabled, these bits should be set with a value corresponding to the lowest expected value of beta for the PNP transistor being used as a temperature sensing device. See Table 6.18 for supported beta ranges.

APPLICATION NOTE: A diode connected transistor or an NPN transistor should use the '1111b' setting. For most applications, the automatic beta detection circuitry will determine the optimal settings to be used. Only disable the automatic beta detection circuitry if using a known transistor.

Table 6.18 Beta Compensation Look Up Table

BETAX[2:0]				
3	**2**	**1**	**0**	**MINIMUM BETA**
0	0	0	0	0.050
0	0	0	1	0.066
0	0	1	0	0.087
0	0	1	1	0.114
0	1	0	0	0.150
0	1	0	1	0.197
0	1	1	0	0.260
0	1	1	1	0.342
1	0	0	0	0.449
1	0	0	1	0.591
1	0	1	0	0.778
1	0	1	1	1.024
1	1	0	0	1.348
1	1	0	1	1.773
1	1	1	0	2.333
1	1	1	1	Disabled

6.15 Ideality Configuration Registers

Table 6.19 Ideality Configuration Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
3Bh	External Diode 2 Ideality Configuration	-	-	B5	B4	B3	B2	B1	B0	SWL	12h
3Ch	External Diode 3 Ideality Configuration	-	-	B5	B4	B3	B2	B1	B0	SWL	12h

The Ideality Configuration Registers hold a value that is automatically applied to the corresponding external diode channel. This Ideality Configuration corrects offsets and errors caused by external diode ideality factors that do not match the internally calibrated value. The value is 6 bits and allows for adjustment of the ideality factor based on 000000b being equal to 0.9850. Approximate ideality configuration factors are shown in Table 6.20. The shaded entries indicate the default value.

Table 6.20 Ideality Factor Look Up Table

SETTING	FACTOR		SETTING	FACTOR		SETTING	FACTOR
001000	0.9951		011000	1.0159		101000	1.0377
001001	0.9964		011001	1.0173		101001	1.0391
001010	0.9976		011010	1.0186		101010	1.0404
001011	0.9989		011011	1.0199		101011	1.0418
001100	1.0002		011100	1.0213		101100	1.0432
001101	1.0015		011101	1.0226		101101	1.0446
001110	1.0028		011110	1.0240		101110	1.0460
001111	1.0041		011111	1.0253		101111	1.0475
010000	1.0054		100000	1.0267		110000	1.0489
010001	1.0067		100001	1.0280		110001	1.0503
010010	1.0080		100010	1.0294		110010	1.0517
010011	1.0093		100011	1.0308		110011	1.0531
010100	1.0106		100100	1.0321		110100	1.0546
010101	1.0119		100101	1.0335		110101	1.0560
010110	1.0133		100110	1.0349		110110	1.0574
010111	1.0146		100111	1.0363		110111	1.0589

6.16 PWM Configuration Register

Table 6.21 PWM Configuration Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
3Dh	PWM Configuration	-	-	PWM2_OT	PWM1_OT	PWM2_BASE [1:0]		PWM1_BASE [1:0]		SWL	0Fh

The PWM Configuration Register controls the base PWM frequency range and output options.

Bit 5 - PWM2_OT - Determines the output type of the PWM2 / GPIO1 pin when configured as a PWM output.

- ‘0’ (default) - the PWM2 / GPIO1 pin is configured as an open drain output when configured as a PWM output
- ‘1’ - the PWM2 / GPIO1 pin is configured as a push-pull output when configured as a PWM output.

Bit 4 - PWM1_OT - Determines the output type of the THERMTRIP_SIO / PWM1 / GPIO5 pin when configured as a PWM output.

- '0' (default) - the THERMTRIP_SIO / PWM1 / GPIO5 pin is configured as an open drain output when configured as a PWM output
- '1' - the THERMTRIP_SIO / PWM1 / GPIO5 pin is configured as a push-pull output when configured as a PWM output.

Bits 3 - 2 - PWM2_BASE[1:0] - Determine the frequency range of the PWM 2 fan driver (when enabled) as shown in Table 6.22. Note that at the higher PWM frequencies, the PWM resolution is reduced.

Bits 1 - 0 - PWM1_BASE[1:0] - Determine the frequency range of the PWM 1 fan driver (when enabled) as shown in Table 6.22. Note that at the higher PWM frequencies, the PWM resolution is reduced.

Table 6.22 PWMx_BASE[1:0] Decode

PWMX_BASE[1:0]		PWM FREQUENCY	RESOLUTION
1	**0**		
0	0	26kHz	8-bit
0	1	19.5kHz	10-bit
1	0	4,882Hz	10-bit
1	1	2,441Hz (default)	10-bit

6.17 Company ID Register

Table 6.23 Company ID Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
3Eh	Company ID Register	0	1	0	1	1	1	0	1	No	5Dh

The Company ID Register contains the 8 bit company code.

6.18 Revision Register (3Fh)

Table 6.24 Revision Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
3Fh	Revision	0	0	0	0	0	0	0	0	SWL	00h

The Revision Register contains a 8 bit word that identifies the die revision.

6.19 Lock Start Register

Table 6.25 Lock Start Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
40h	Lock/Start Register	-	-	-	-	-	-	Lock	Start	SWL	01h

The Lock-Start register is included for legacy purposes and controls the Software Locking functionality (see Section 6.1.1, "Lock Entries").

Bit 1 - LOCK - this bit acts on all registers that are designated SWL. When this bit is set, the locked registers become read only and cannot be updated.

Bit 0 - START - The START bit is READ ONLY and is automatically set to '1' based on the 3V_PWROK# pin, VDD_PWRGD pin, and the LPM bit. If the LPM bit is set, then the START bit will be set regardless of the status of the 3V_PWROK# and VDD_PWRGD pins. Conversely, if the LPM bit is not set, then the START bit will only be set to a logic '1' if both the 3V_PWROK# and the VDD_PWRGD pins are asserted.

6.20 Interrupt Status Registers

Table 6.26 Interrupt Status Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
41h	Interrupt Status Register 1	ERR2	TRD2	TINT	TRD1	ERR1	VDD	VCP1	VCP2	No	00h
42h	Interrupt Status Register 2	GPIO	TSD	ERR3	TRD3	LDO_ POK_n	LDO_ SHORT	FAN_ SHORT2	FAN_ SHORT1	No	00h
44h	Interrupt Status Register 3	ERR7	TRD7	ERR6	TRD6	ERR5	TRD5	ERR4	TRD4	No	00h
45h	Interrupt Status Register 4	TACH2	TACH1	-	VIN1	ERR9	TRD9	ERR8	TRD8	No	00h

The Interrupt Status Registers report the operating condition of the EMC4002. Each input bit can be individually enabled or globally disabled. If any of the bits are asserted then the ATF_INT# pin will be asserted low (assuming that the INTEN bit is set to logic '1'). Reading from the status register clears all status bits if the error conditions is removed. If there are no set status bits, then the ATF_INT# pin will be released.

6.20.1 Interrupt Status Register 1 (41h)

Bit 7 - ERR2 - this bit is asserted '1' if there is a diode fault on External Diode 2.

Bit 6 - TRD2 - this bit is asserted '1' if the External Diode 2 Temperature measurement exceeds the high limit or falls below the low limit.

Bit 5 - TINT - this bit is asserted '1' if the Internal temperature channel exceeds the high limit or falls below the low limit.

APPLICATION NOTE: If the LDO or either of the Dual Voltage Fan Driver are active, the die will experience self-heating that will increase the temperature that the Internal diode channel measures. To avoid nuisance interrupts, the Internal Diode channel should not be enabled unless these devices are disabled.

Bit 4 - TRD1 - this bit is asserted ‘1’ if the External Diode 1 Temperature measurement (or the THERM channel measurement if enabled) exceeds the software defined high limit or falls below the software defined low limit. Exceeding the Temperature Programmable Voltage limit does not update the bit unless the temperature also exceeds the software high limit.

Bit 3 - ERR1 - this bit is asserted ‘1’ if there is a diode fault on External Diode 1.

Bit 2 - VDD- this bit is asserted ‘1’ if the VDD voltage exceeds the high limit or drops below the low limit.

Bit 1- VCP1 - this bit is asserted ‘1’ if the VCP1 input voltage exceeds the high limit or drops below the low limit.

Bit 0 -VCP2 - this bit is asserted ‘1’ if the VCP2 input voltage exceeds the high limit or drops below the low limit.

6.20.2 Interrupt Status Register 2 (42h)

Bit 7 - GPIO - this bit is asserted ‘1’ if any of the GPIO channels configured as inputs change states (assuming that they are not masked). The GPIO status bit is always cleared upon a read.

Bit 6 - TSD - this bit is asserted ‘1’ if there is a thermal shutdown condition.

Bit 5 - ERR3 - this bit is asserted ‘1’ if there is a diode fault on External Diode 3

42h - Bit 4 - TRD3 - this bit is asserted ‘1’ if the External Diode 3 Temperature measurement exceeds the high limit or falls below the low limit.

Bit 3 - LDO_POK_n - this bit reflects the inverse of the LDO_POK pin - if this bit is asserted ‘1’, then the LDO output is not being regulated.

Bit 2 - LDO_SHORT - this bit is asserted ‘1’ if the LDO detects a short circuit condition

Bit 1 - FAN_SHORT2 - This bit is asserted ‘1’ if the Dual Voltage Fan Driver 2 circuit detects a short circuit condition.

Bit 0 - FAN_SHORT1 - this bit is asserted ‘1’ if the Dual Voltage Fan Driver 1 circuit detects a short circuit condition.

6.20.3 Interrupt Status Register 3 (44h)

Bit 7 - ERR7 - This bit is asserted ‘1’ if a diode fault is detected on External Diode 7.

Bit 6 - TRD7 - This bit is asserted ‘1’ if the External Diode 7 Temperature measurement exceeds the high limit or falls below the low limit.

Bit 5 - ERR6 - This bit is asserted ‘1’ if a diode fault is detected on External Diode 6.

Bit 4 - TRD6 - This bit is asserted ‘1’ if the External Diode 6 Temperature measurement (or the VIN2 measurement if enabled) exceeds the high limit or falls below the low limit.

- Bit 3 - ERR5 - this bit is asserted ‘1’ if a diode fault is detected on External Diode 5.

Bit 2 - TRD5 - this bit is asserted ‘1’ if the External Diode 5 Temperature measurement exceeds the high limit or falls below the low limit.

Bit 1 - ERR4 - this bit is asserted ‘1’ if a diode fault is detected on External Diode 4.

Bit 0 - TRD4 - this bit is asserted ‘1’ if the External Diode 4 Temperature measurement exceeds the high limit or falls below the low limit.

6.20.4 Interrupt Status Register 4 (45h)

BIt 7 - TACH2 - This bit is asserted ‘1’ if the RPM based Fan Control Algorithm for Fan 2 detects a stalled fan condition, the Spin-up Routine does not detect a valid tach signal, or the fan cannot reach the target fan speed at full drive.

BIt 6 - TACH1 - This bit is asserted ‘1’ if the RPM based Fan Control Algorithm for Fan 1 detects a stalled fan condition, the Spin-up Routine does not detect a valid tach signal, or if the fan cannot reach the target fan speed at full drive.

Bit 4 - VIN1 - This bit is asserted ‘1’ if the VIN1 voltage exceeds the high limit or drops below the low limit.

Bit 3 - ERR9 - this bit is asserted ‘1’ if a diode fault is detected on External Diode 9.

Bit 2 - TRD9 - this bit is asserted ‘1’ if the External Diode 9 Temperature measurement exceeds the high limit or falls below the low limit.

Bit 1 - ERR8 - this bit is asserted ‘1’ if a diode fault is detected on External Diode 8.

Bit 0 - TRD8 - this bit is asserted ‘1’ if the External Diode 8 Temperature measurement exceeds the high limit or falls below the low limit.

6.21 ThermTrip Pin State Register

Table 6.27 ThermTrip Pin State Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
43h	ThermTrip Pin State	DIODE_ MD	LDO_ FAN	ACAVAIL_ CLR	POWER_ SW#	THERM TRIP3#	THERM TRIP2#	THERM TRIP1#	3V_ PWROK#	No	00h

Bit 7 - DIODE_MD - Indicates the select function for the External Diode 1 channel based on the ADDR_MODE pin pull-up resistor.

- ‘0’ - The External Diode 1 channel is measuring a 2N3904 diode connected between the DP1 / VREF_T and DN1/ THERM pins.
- ‘1’ - The External Diode 1 channel is measuring a thermistor input biased via the DP1 / VREF_T pin and measured on the DN1 / THERM pin.

Bit 6 - LDO_FAN - Indicates whether the LDO is active or the 2nd Dual Voltage Fan Driver is active.

- ‘0’ - The LDO is active.
- ‘1’ - The 2nd Dual Voltage Fan Driver is active.

Bit 5 - ACAVAIL_CLR - reflects the state of the ACAVAIL_CLR pin.

Bit 4 - POWER_SW# - reflects the state of the POWER_SW# pin.

Bit 3 - THERMTRIP3# - reflects the state of the THERMTRIP3# pin.

Bit 2 - THERMTRIP2# - reflects the state of the THERMTRIP2# pin.

Bit 1 - THERMTRIP1# - reflects the state of the THERMTRIP1# pin.

Bit 0 - 3V_PWROK# - reflects the state of the 3V_PWROK# pin.

6.22 Voltage Limit Registers

Table 6.28 Voltage Limit Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
46h	VCP1 Low Limit	7	6	5	4	3	2	1	0	SWL	00h
47h	VCP1 High Limit	7	6	5	4	3	2	1	0	SWL	FFh
48h	VDD Low Limit	7	6	5	4	3	2	1	0	SWL	00h
49h	VDD High Limit	7	6	5	4	3	2	1	0	SWL	FFh
4Ah	VCP2 Low Limit	7	6	5	4	3	2	1	0	SWL	00h
4Bh	VCP2 High Limit	7	6	5	4	3	2	1	0	SWL	FFh
4Ch	VIN1 Low Limit	7	6	5	4	3	2	1	0	SWL	00h
4Dh	VIN1 High Limit	7	6	5	4	3	2	1	0	SWL	FFh

The EMC4002 contains both high and low voltage limits for the VDD, VCP1, VCP2, and VIN1voltage inputs. These limits are compared to the appropriate measurement channel after every conversion cycle and whenever the limits are updated. If the high limit is exceeded, or the measured data is below the low limit, then the appropriate Status bit is set.

6.23 Temperature Limit Registers

Table 6.29 Temperature Limit Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
4Eh	External Diode 1 low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
	THERM Low Limit (when enabled)	128	64	32	16	8	4	2	1	SWL	81h (0.4V)
4Fh	External Diode 1 High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)
	THERM High Limit (when enabled)	128	64	32	16	8	4	2	1	SWL	7Fh (0.4V)
50h	Internal Temp Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
51h	Internal Temp High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)
52h	External Diode 2 Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
53h	External Diode 2 High Limit	Sign	64	32	16	8	4	2	1	SWL	46h (+76°C)

Table 6.29 Temperature Limit Registers (continued)

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
54h	External Diode 3 Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
55h	External Diode 3 High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)
56h	External Diode 4 Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
57h	External Diode 4 High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)
58h	External Diode 5 Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
59h	External Diode 5 High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)
5Ah	External Diode 6 Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
	VIN2 Low Limit	128	64	32	16	8	4	2	1	SWL	81h (0.4V)
5Bh	External Diode 6 High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)
	VIN2 High Limit	128	64	32	16	8	4	2	1	SWL	7Fh (0.4V)
5Ch	External Diode 7 Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
5Dh	External Diode 7 High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)
5Eh	External Diode 8 Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
5Fh	External Diode 8 High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)
60h	External Diode 9 Low Limit	Sign	64	32	16	8	4	2	1	SWL	81h (-127°C)
61h	External Diode 9 High Limit	Sign	64	32	16	8	4	2	1	SWL	7Fh (+127°C)

The EMC4002 contains both high and low limits for all temperature channels. The limits are limited to 8 bit values and all comparisons are done with the upper 8 bits of data as appropriate. If any particular temperature channel exceeds the high limit then the appropriate status bit is set. Likewise, if any particular temperature channel drops below the low limit, then the appropriate status bit is set.

The low limits can be used to detect diode fault conditions that are not explicitly detected by circuitry such as a short between DP and DN or a short of DP to ground or a short of DN to VDD. In all of these cases, the ADC will return a high byte value of 80h (diode fault) indicating that the delta V_{BE} is zero.

If the External Diode 1 or External Diode 6 channels are configured to measure a voltage input, then the corresponding External Diode limit registers are checked at the end of each conversion cycle. The data written in these registers must be of the proper data format or extraneous interrupts may occur.

6.24 REC Enable Register

Table 6.30 REC Enable Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
70h	REC Enable	EN_ REC9	EN_ REC8	EN_ REC7	EN_ REC6	EN_ REC5	EN_ REC4	EN_ REC3	EN_ REC2	SWL	FFh

The REC Enable Register enables or disables the Resistance Error Correction circuitry for the corresponding external diode channel.

Bit 7 - EN_REC9 - Enables the REC circuitry on the External Diode 9 channel (if enabled).

- '0' - The Resistance Error Correction circuitry is disabled for External Diode 9.
- '1' - (default) The Resistance Error Correction circuitry is enabled for External Diode 9.

Bit 6 - EN_REC8 - Enables the REC circuitry on the External Diode 8 channel (if enabled).

Bit 5 - EN_REC7 - Enables the REC circuitry on the External Diode 7 channel (if enabled).

Bit 4 - EN_REC6 - Enables the REC circuitry on the External Diode 6 channel (if enabled).

Bit 3 - EN_REC5 - Enables the REC circuitry on the External Diode 5 channel.

Bit 2 - EN_REC4 - Enables the REC circuitry on the External Diode 4 channel.

Bit 1 - EN_REC3 - Enables the REC circuitry on the External Diode 3 channel.

Bit 0 - EN_REC2 - Enables the REC circuitry on the External Diode 2 channel.

6.25 PWM Divide Registers

Table 6.31 PWM Divide Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
72h	PWM 1 Divide	128	64	32	16	8	4	2	1	SWL	28h (40d)
73h	PWM 2 Divide	128	64	32	16	8	4	2	1	SWL	28h (40d)

The PWM Divide Registers determine the final PWM frequency. The base frequency set by the PWM1_BASE[1:0] or PWM2_BASE[1:0] bits is divided by the decimal equivalent of the register settings. The final PWM frequency is given by Equation [1].

$$PWM\_Frequency = \frac{base\_clk}{PWM\_D} \quad [1]$$

Where:

base_clk = The base frequency set by the PWMx_CFG[1:0] bits

PWM_D = the divide setting set by the PWMx Divide Registers

6.26 ThermTrip Temperature Register

Table 6.32 ThermTrip Temperature Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
75h	ThermTrip Temperature	128	64	32	16	8	4	2	1	No	7Fh

The ThermTrip Temperature Register is a read-only register that stores the Voltage Programmable Threshold temperature used in the Voltage Programmable Fail-Safe Temperature Monitor. The contents of the register reflect the calculated temperature based on the VSET voltage. This register is updated at the end of every monitoring cycle based on the current value of VSET. The register value reflects the calculated threshold temperature based on the VSET voltage.

If the External Diode 1 Channel is configured to operate as a thermistor input, then no calculations are done and this register will reflect the current VSET voltage.

6.27 Failsafe Status Register

Table 6.33 FailSafe Status Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
76h	FailSafe Status	-	-	LDO_ FAIL	TSD	TRIP3	TRIP2	TRIP1	HWFS	No	00h

The FailSafe Status Register is a read-only register that indicates which input to the ThermTrip logic block (THERMTRIP3#, THERMTRIP2#, THERMTRIP1#, and HW_FAILSAFE#) was responsible for causing the SYS_SHDN# signal to be asserted. This register and the FailSafe Configuration Register are unique in that they are powered from the RTC_PWR3V pin so that if power is removed from the VDD pin, these registers will not be reset.

In this register, each bit is set to ‘1’ when the corresponding input pin (or signal) is asserted low. Once set, the bits remain set until they are cleared by writing to the CFS bit in the Special Function Register.

This register will not be updated if the 3V_PWROK# and VDD_PWRGD pins are not asserted.

Bit 5 - LDO_FAIL - indicates that the LDO circuit has entered an invalid state. This bit is set any time the LDO_POK pin is asserted low. This bit will not cause the THERMTRIP_SIO or SYS_SHDN# pins to be asserted.

Bit 4 - TSD - indicates that a thermal shutdown event has occurred. This bit will not cause the THERMTRIP_SIO or SYS_SHDN# pins to be asserted.

Bit 3 - TRIP3 - indicates that the THERMTRIP3# input has been asserted low.

Bit 2 - TRIP2 - indicates that the THERMTRIP2# input has been asserted low.

Bit 1 - TRIP1 - indicates that the THERMTRIP1# input has been asserted low.

Bit 0 - HWFS - indicates that the internal HW_FAILSAFE# signal has been asserted low.

6.28 FailSafe Configuration Register

Table 6.34 FailSafe Config Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
77h	FailSafe Config	-	-	-	-	-	-	DIS_WD	LPM	SWL	00h

The FailSafe Configuration Register stores configuration bits that are retained across all power mode including the RTC Power Mode. This register and the FailSafe Status Register are unique in that they are powered from the RTC_PWR3V pin so that if power is removed from the VDD pin, these registers will not be reset.

Bit 1 - DIS_WD - Disables the watchdog timer

- '0' (default) - The Watchdog timer is enabled. Any time that either the 3V_PWROK# and VDD_PWRGD are deasserted, the watchdog is reset and ready. When both the 3V_PWROK# and VDD_PWRGD are re-asserted, then it will start counting.
- '1' - The Watchdog timer is disabled.

Bit 0 - LPM - Determines whether the EMC4002 is placed into low power mode or sleep mode when either the 3V_PWROK# or VDD_PWRGD pins are de-asserted. In both cases, the SYS_SHDN# and THERMTRIP_SIO pins (if enabled) will be blocked.

- '0' (default) - The Low Power Mode is not enabled. When the 3V_PWROK# or VDD_PWRGD pins are de-asserted, all hardware monitoring will cease and the fan drivers will be disabled. The LDO is controlled separately.
- '1' - The Low Power Mode is enabled. When the 3V_PWROK# or VDD_PWRGD pins are de-asserted, the hardware monitoring will continue to function. The fan drivers will still be disabled. The LDO is controlled separately.

6.29 Error Debug Register

Table 6.35 Error Debug Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
7Ah	Error Debug Register	CRC	ARA	STOP	-	-	-	-	NONAC	No	00h

The Error Debug register is used to indicate the invalid SMBus protocol response that causes the device to abort an SMBus transaction and reset the SMBus protocol.

Bit 7 - CRC - A CRC error was detected when communicating via the BC-Link interface.

Bit 6 - ARA - an error was detected during the SMBus Alert Response Address command.

Bit 5 - STOP - indicates that a pre-mature SMBus Stop condition was detected.

Bit 0 - NONAC - indicates that the host did not generate a NACK bit during a Read Byte or Receive Byte command.

6.30 Special Function Register

Table 6.36 Special Function Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
7Ch	Special Function Register	RES	RES	RES	-	CFS	INTEN	RES	RES	No	04h

The Special Function Register controls the interrupt pin and ThermTrip Status register.

Bit 7 - Reserved - This bit is always ‘0’.

Bit 6 - Reserved - This bit is always ‘0’.

Bit 5 - Reserved - This bit is always ‘0’.

APPLICATION NOTE: The CFS bit requires both the 3V_PWROK# and VDD_PWRGD to be asserted before it will clear the Failsafe Status Register. This applies to both Standby and Low Power modes. If the bit is set while the 3V_PWROK# and / or VDD_PWRGD pins are de-asserted, it will remain set and clear the Failsafe Status Register when both the 3V_PWROK# and VDD_PWRGD signals are asserted.

Bit 3 - CFS - clears the Failsafe Status register. When set to ‘1’, the FailSafe Status register is cleared and reset to default values. This bit is NOT self clearing and must be set to ‘0’ in order for the FailSafe Status register to function correctly.

Bit 2 - INTEN - enables all interrupts to assert the ATF_INT# pin low. This bit is automatically cleared when the EMC4002 responds to an ARA command. It must be manually reset in order for interrupts to function.

- ‘0’ - all interrupts are disabled and will not cause ATF_INT# to be asserted low. The status registers will still reflect all interrupt conditions.
- ‘1’ (default) - all interrupts can be individually enabled and disabled.

Bit 1 - Reserved - This bit is always ‘0’.

Bit 0 - Reserved - This bit is always ‘0’.

6.31 Interrupt Status Enable Registers

Table 6.37 Interrupt Enable Registers

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
7Dh	Interrupt Status Enable Register 2	RD7	RD6	RD5	RD4	TSD	LDO	FAN1	RD3	SWL	00h
7Eh	Interrupt Status Enable Register 1	TEMP	RD2	INT	RD1	VOLT	VDD	VCP1	VCP2	SWL	C0h
7Fh	Interrupt Status Enable Register 3	GPIO	-	VIN1	RD9	RD8	TACH2	TACH1	FAN2	SWL	00h

The Interrupt Status Enable Registers determine which interrupt events will update the status registers. If a condition or channel is not enabled, then any error conditions associated with it will be ignored.

6.31.1 Interrupt Status Enable Register 2 (7Dh)

Bit 7 - RD7 - Enables External Diode 7 interrupts including diode faults and out of limit conditions.

Bit 6 - RD6 - Enables External Diode 6 interrupts including diode faults and out of limit conditions. This includes the VIN2 measurement channel if enabled.

Bit 5 - RD5- enables External Diode 5 interrupts including diode faults and out of limit conditions.

Bit 4 - RD4 - enables External Diode 4 interrupts including diode faults and out of limit conditions.

Bit 3 - TSD - enables Thermal Shutdown based interrupts.

Bit 2 - LDO - enables LDO based interrupts including the LDO_POK and LDO_SHORT circuit conditions.

Bit 1 - FAN1 - enable Fan controller based interrupts (i.e. FAN_SHORT) for Fan 1

Bit 0 - RD3 - enables External Diode 3 interrupts including diode faults and out of limit conditions.

6.31.2 Interrupt Status Enable Register 1 (7Eh)

Bit 7 - TEMP - enables all Temperature channels globally from affecting the ATF_INT# pin. The temperature channels are individually enabled/disabled to update the Status register.

- '0' - All temperature channel interrupts will not assert the ATF_INT# pin though they may still be individually enabled to affect the Status Register.
- '1' (default) - All temperature channel interrupts can be enabled and disabled individually to affect both the status register and the ATF_INT# pin.

Bit 6 - RD2 - enables External Diode 2 interrupts including diode faults and out of limit conditions.

Bit 5 - INT - enables Internal diode interrupts.

Bit 4 - RD1 - enables External Diode 1 interrupts including diode faults and out of limit conditions. This includes the THERM measurement channel when enabled.

Bit 3 - VOLT - enables all Voltage channels globally from affecting the ATF_INT# pin. The voltage channels still are individually enabled/disabled to update the Status register.

- '0' - All voltage channel interrupts will not assert the ATF_INT# pin though they may still be individually enabled to affect the Status Register.
- '1' (default) - All voltage channel interrupts can be enabled and disabled individually to affect both the status register and the ATF_INT# pin.

Bit 2 - VDD - enables VDD based interrupts.

Bit 1 - VCP1 - enables VCP1 based interrupts.

Bit 0 - VCP2 - enables VCP2 based interrupts.

6.31.3 Interrupt Status Enable Register 3 (7Fh)

Bit 7 - GPIO - enables GPIO based interrupts.

Bit 5 - VIN1 - enables VIN1 based interrupts.

Bit 4 - RD9 - enables External Diode 9 interrupts including diode faults and out of limit conditions.

Bit 3 - RD8 - Enables External Diode 8 interrupts including diode faults and out of limit conditions.

Bit 2 - TACH2 - Enables tach based interrupts (stalled fan, spin up error, or drive fail) for the RPM based Fan Control Algorithm for Fan 2.

Bit 1 - TACH1 - Enables tach based interrupts (stalled fan, spin up error, or drive fail) for the RPM based Fan Control Algorithm for Fan 2.

Bit 1 - FAN1 - enable Fan controller based interrupts (i.e. FAN_SHORT) for Fan 2

6.32 Fan Driver Setting Registers

Table 6.38 Fan Driver Setting Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
80h	R/W	Fan 1 Driver Setting Low Byte	2	1	-	-	-	-		-	No	00h
81h	R/W	Fan 1 Driver Setting High Byte	512	256	128	64	32	16	8	4	No	00h
90h	R/W	Fan 2 Driver Setting Low Byte	2	1	-	-	-	-		-	No	00h
91h	R/W	Fan 2 Driver Setting High Byte	512	256	128	64	32	16	8	4	No	00h

The Fan Driver Setting Registers are used to control the output of the individual Fan Drivers. The driver setting is the same if the output driver is configured as a PWM or a Dual Voltage Fan Driver and operate independently of the Polarity bit (for the PWM output). That is, a setting of 00_00h will mean that the fan drive is at minimum drive while a value of FF_C0h will mean that the fan drive is at maximum drive.

If the Spin Up Routine is invoked, reading from the registers will return the current fan drive setting that is being used by the Spin Up Routine instead of what was previously written into these registers.

The Fan Driver Setting Registers, when the RPM based Fan Control Algorithm is enabled, are read only. Writing to the register will have no affect and the data will not be stored. Reading from the register will always return the current fan drive setting.

If the 3V_PWROK# or VDD_PWRGD pins are de-asserted, the Fan Setting Registers will be made read only. Writing to the registers will have no affect and reading from the registers will return 00h.

When the RPM based Fan Control Algorithm is disabled, the current fan drive setting that was last used by the algorithm is retained and will be used.

If the Fan Setting Registers are set to a value of 00_00h, then all tachometer related status bits will be masked until the setting is changed. Likewise, the FAN_SHORT bit will be cleared and masked until the setting is changed.

6.33 Fan Configuration 1 Registers

Table 6.39 Fan Configuration 1 Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
82h	R/W	Fan 1 Configuration 1	EN_ ALGO	RANGE[1:0]		EDGES[1:0]		UPDATE[2:0]			SWL	2Bh
92h	R/W	Fan 2 Configuration 1	EN_ ALGO	RANGE[1:0]		EDGES[1:0]		UPDATE[2:0]			SWL	2Bh

The Fan Configuration Register 1controls the general operation of the RPM based Fan Control Algorithm used both fan drivers.

Bit 7 - EN_ALGO - enables the RPM based Fan Control Algorithm. If the TACH1 / GPIO3 bit is set, then this bit is automatically cleared for Fan 1. If the TACH2 / GPIO4 bit is set, then this bit is automatically cleared for Fan 2.

- ‘0’ - (default) the control circuitry is disabled and the fan driver output is determined by the Fan Driver Setting Register for the appropriate fan driver.
- ‘1’ - the control circuitry is enabled and the Fan Driver output will be automatically updated to maintain the programmed fan speed as indicated by the TACH Target Register.

Bits 6- 5 - RANGE[1:0] - Adjusts the range of reported and programmed tachometer reading values. The RANGE bits determine the weighting of all TACH values (including the Valid TACH Count, TACH Target, and TACH reading) as shown in Table 6.40, "Range Decode".

Table 6.40 Range Decode

RANGE[1:0]		REPORTED MINIMUM RPM	TACH COUNT MULTIPLIER
1	0		
0	0	500	1
0	1	1000 (default)	2
1	0	2000	4
1	1	4000	8

Bits 4-3 - EDGES[1:0] - determines the minimum number of edges that must be detected on the TACHx signal to determine a single rotation. A typical fan measured 5 edges (for a 2-pole fan).

Increasing the number of edges measured with respect to the number of poles of the fan will cause the TACH Reading registers to indicate a fan speed that is higher or lower than the actual speed. In order for the FSC Algorithm to operate correctly, the TACH Target must be updated by the user to accommodate this shift. The Effective Tach Multiplier shown in Table 6.41, "Minimum Edges for Fan Rotation" is used as a direct multiplier term that is applied to the Actual RPM to achieve the Reported RPM. It should only be applied if the number of edges measured does not match the number of edges expected based on the number of poles of the fan (which is fixed for any given fan).

Contact Microchip for recommended settings when using fans with more or less than 2 poles.

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Table 6.41 Minimum Edges for Fan Rotation

EDGES[1:0]		MINIMUM TACH EDGES	NUMBER OF FAN POLES	EFFECTIVE TACH MULTIPLIER (BASED ON 2 POLE FANS) IF EDGES CHANGED
1	0			
0	0	3	1 pole	0.5
0	1	5	2 poles (default)	1
1	0	7	3 poles	1.5
1	1	9	4 poles	2

Bit 2-0 - UPDATE - determines the base time between fan driver updates. The Update Time, along with the Fan Step Register, is used to control the ramp rate of the drive response to provide a cleaner transition of the actual fan operation as the desired fan speed changes. The Update Time is set as shown in Table 6.42.

APPLICATION NOTE: This ramp rate control applies for all changes to the active PWM output including when the RPM based Fan Speed Control Algorithm is disabled.

Table 6.42 Update Time

UPDATE[2:0]			UPDATE TIME
2	1	0	
0	0	0	100ms
0	0	1	200ms
0	1	0	300ms
0	1	1	400ms (default)
1	0	0	500ms
1	0	1	800ms
1	1	0	1200ms
1	1	1	1600ms

6.34 Fan Configuration 2 Registers

Table 6.43 Fan Configuration 2 Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
83h	R/W	Fan 1 Configuration 2	EN_ RRC1	DIS_ GLITCH1	DER_OPT 1 [1:0]		ERR_RNG [1:0]		POLA RITY1	FAN1 / PWM1	SWL	34h
93h	R/W	Fan 2 Configuration 2	EN RRC2	DIS_ GLITCH2	DER_OPT 2 [1:0]		ERR_RNG [1:0]		POLA RITY2	FAN2 / PWM2	SWL	34h

The Fan Configuration 2 Registers control the tachometer measurement and advanced features of the RPM based Fan Control Algorithm.

Bit 7 - EN_RRCx - Enables the ramp rate control circuitry during the Manual Mode of operation.

- '0' (default) - The ramp rate control circuitry for the Manual Mode of operation is disabled. When the Fan Drive Setting values are changed and the RPM based Fan Control Algorithm is disabled, the fan drivers will be set to the new setting immediately.
- '1' - The ramp rate control circuitry for the Manual Mode of operation is enabled. When the Fan Drive Setting values are changed, the change is compared against the Fan Step Register settings. If the change is larger than the Fan Step, then the fan drivers will be incrementally updated based on the update time until the final programmed Fan Drive Setting value is reached. See Figure 6.1, "Ramp Rate Control"

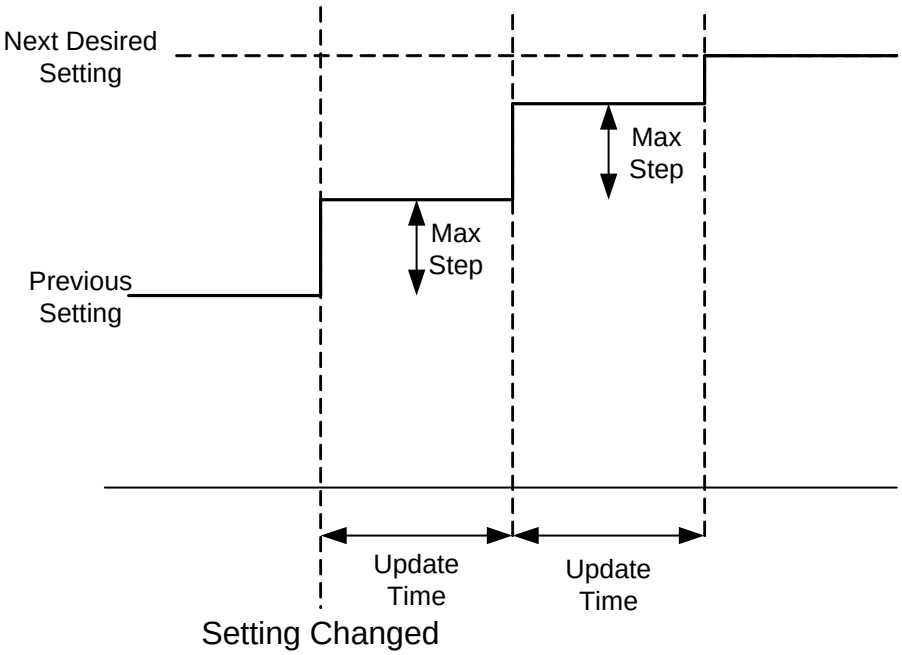

Figure 6.1 Ramp Rate Control

Bit 6 - DIS_GLITCHx - Disables the low pass glitch filter that removes high frequency noise injected on the TACHx pin(s).

- '0' (default) - The glitch filter is enabled.
- '1' - The glitch filter is disabled.

Bits 5 - 4 - DER_OPTx[1:0] - Control some of the advanced options that affect the derivative portion of the RPM based fan control algorithm as shown in Table 6.44, "Derivative Options". These bits only apply if the Fan Speed Control Algorithm is used.

Table 6.44 Derivative Options

DER_OPTX[1:0]		OPERATION
1	**0**	
0	0	No derivative options used
0	1	Basic derivative. The derivative of the error from the current drive setting and the target is added to the iterative PWM drive setting (in addition to proportional and integral terms)
1	0	Step derivative. The derivative of the error from the current drive setting and the target is added to the iterative PWM drive setting and is not capped by the maximum PWM drive step. This allows for very fast response times
1	1	Both the basic derivative and the step derivative are used effectively causing the derivative term to have double the effect of the derivative term (default).

Bit 3 - 2 - ERR_RNGx[1:0] - Control some of the advanced options that affect the error window. When the measured fan speed is within the programmed error window around the target speed, then the fan drive setting is not updated. These bits only apply if the Fan Speed Control Algorithm is used.

Table 6.45 Error Range Options

ERR_RNGX[1:0]		OPERATION
1	**0**	
0	0	0 RPM
0	1	50 RPM (default)
1	0	100 RPM
1	1	200 RPM

Bit 1 - POLARITY - Determines the polarity of the respective PWM driver. This does NOT affect the drive setting registers. A setting of 0% drive will still correspond to 0% drive independent of the polarity.

- ‘0’ (default) - the Polarity of the PWM driver is normal. A drive setting of 00h will cause the output to be set at 0% duty cycle and a drive setting of FFh will cause the output to be set at 100% duty cycle.
- ‘1’ - The Polarity of the PWM driver is inverted. A drive setting of 00h will cause the output to be set at 100% duty cycle and a drive setting of FFh will cause the output to be set at 0% duty cycle.

Bit 0 - FANx / PWMx - Determines whether the RPM based Fan Control Algorithm will drive a PWM output or the Dual Voltage Fan Driver Output.

- ‘0’ (default) - The RPM based Fan Control Algorithm will drive the Dual Voltage Fan Driver circuitry using a 10-bit DAC to set the output voltage. The corresponding PWM output pin (PWM1 or PWM2 respectively) will automatically be configured as a GPIO and is controlled by the GPIO Registers.
- ‘1’ - The RPM based Fan Control Algorithm will use a PWM output. The Dual Voltage Fan Driver will be disabled. The corresponding PWM output pin will be automatically configured as a PWM output and controlled by the PWM Config Register and the PWM Divide Registers.

6.35 Gain Registers

Table 6.46 Gain Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
84h	R/W	Gain 1 Register	-	-	GAIND[1:0]		GAINI[1:0]		GAINP[1:0]		SWL	2Ah
94h	R/W	Gain 2 Register	-	-	GAIND[1:0]		GAINI[1:0]		GAINP[1:0]		SWL	2Ah

The Gain Registers store the gain terms used by the proportional and integral portions of each of the RPM based Fan Control Algorithms. These registers only apply if the Fan Speed Control Algorithm is used.

Table 6.47 Gain Decode

GAIND OR GAINP OR GAINI [1:0]		RESPECTIVE GAIN FACTOR
1	**0**	
0	0	1x
0	1	2x
1	0	4x (default)
1	1	8x

6.36 Fan Spin Up Configuration Registers

Table 6.48 Fan TACH Configuration Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
85h	R/W	Fan 1 Spin Up Configuration	DRIVE_FAIL_CNT1[1:0]		NOK ICK1	SPIN_LVL[2:0]			SPINUP_TIME [1:0]		SWL	19h
95h	R/W	Fan 2 Spin up Configuration	DRIVE_FAIL_CNT[1:0]		NOK ICK2	SPIN_LVL[2:0]			SPINUP_TIME [1:0]		SWL	19h

The Fan Spin Up Configuration Register controls the settings of Spin Up Routine.

Bit 7 - 6 - DRIVE_FAIL_CNT[1:0] - Determines how many update cycles are used for the Drive Fail detection function as shown in Table 6.49. This circuitry determines whether the fan can be driven to the desired tach target. These settings only apply if the Fan Speed Control Algorithm is enabled.

Table 6.49 DRIVE_FAIL_CNT[1:0] Bit Decode

DRIVE_FAIL_CNT[1:0]		NUMBER OF UPDATE PERIODS
1	**0**	
0	0	Disabled - the Drive Fail detection circuitry is disabled
0	1	16 - the Drive Fail detection circuitry will count for 16 update periods
1	0	32 - the Drive Fail detection circuitry will count for 32 update periods
1	1	64 - the Drive Fail detection circuitry will count for 64 update periods

Bit 5 - NOKICKx - Determines if the Spin Up Routine will drive the fan to 100% duty cycle for 1/4 of the programmed spin up time before driving it at the programmed level.

- '0' (default) - The Spin Up Routine will drive the PWM to 100% for 1/4 of the programmed spin up time before reverting to the programmed spin level.
- '1' - The Spin Up Routine will not drive the PWM to 100%. It will set the drive at the programmed spin level for the entire duration of the programmed spin up time.

Bits 4 - 2 - SPIN_LVL[2:0] - Determines the final drive level that is used by the Spin Up Routine as shown in Table 6.50.

Table 6.50 Spin Level

SPIN_LVL[2:0]			SPIN UP DRIVE LEVEL
2	**1**	**0**	
0	0	0	30%
0	0	1	35%
0	1	0	40%
0	1	1	45%
1	0	0	50%
1	0	1	55%
1	1	0	60% (default)
1	1	1	65%

Bit 1 -0 - SPINUP_TIME[1:0] - determines the maximum Spin Time that the Spin Up Routine will run for (see Section Figure 5.3, "Spin Up Routine"). If a valid tachometer measurement is not detected before the Spin Time has elapsed, then an interrupt will be generated. When the RPM based Fan Control Algorithm is active, the fan driver will attempt to re-start the fan immediately after the end of the last spin up attempt.

The Spin Time is set as shown in Table 6.51.

Table 6.51 Spin Time

SPINUP_TIME[1:0]		TOTAL SPIN UP TIME
1	**0**	
0	0	250 ms
0	1	500 ms (default)
1	0	1 sec
1	1	2 sec

6.37 Fan Step Registers

Table 6.52 Fan Step Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
86h	R/W	Fan 1 Max Step	128	64	32	16	8	4	2	1	SWL	10h
96h	R/W	Fan 2 Max Step	128	64	32	16	8	4	2	1	SWL	10h

The Fan Step Registers, along with the Update Time, control the ramp rate of the fan driver response calculated by the RPM based Fan Control Algorithm. The value of the registers represents the maximum step size each fan driver will take between update times (see Section 6.33, "Fan Configuration 1 Registers").

APPLICATION NOTE: The UPDATE bits and Fan Step Register settings operate independently of the RPM based Fan Speed Control Algorithm and will always limit the PWM setting. That is, if the programmed PWM setting (either in determined by the RPM based Fan Speed Control Algorithm or by manual settings) exceeds the current PWM setting by greater than the Fan Step Register setting, the EMC4002 will limit the PWM change to the value of the Fan Step Register. It will use the Update Time to determine how often to update the drive settings.

APPLICATION NOTE: If the Fan Speed Control Algorithm is used, the default settings in the Fan Configuration 2 Register will cause the maximum fan step settings to be ignored.

If the necessary fan driver delta is larger than the Fan Step, it will be capped at the Fan 1 or 2 Max Step setting and updated every Update Time ms.

6.38 Fan Minimum Drive Registers

Table 6.53 Minimum Fan Drive Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
87h	R/W	Fan 1 Minimum Drive	512	256	128	64	32	16	8	4	SWL	66h
97h	R/W	Fan 2 Minimum Drive	512	256	128	64	32	16	8	4	SWL	66h

The Fan Minimum Drive Registers store the minimum drive setting for each RPM based Fan Control Algorithm. The RPM based Fan Control Algorithm will not drive the fan at a level lower than the minimum drive unless the target Fan Speed is set at FF_00h (see Section 6.41, "TACH Target Registers").

During normal operation, if the fan stops for any reason (including low drive), the RPM based Fan Control Algorithm will attempt to restart the fan. Setting the Fan Minimum Drive Registers to a setting that will maintain fan operation is a useful way to avoid potential fan oscillations as the control circuitry attempts to drive it at a level that cannot support fan operation.

These registers only apply if the Fan Speed Control Algorithm is used.

6.39 Valid TACH Count Registers

Table 6.54 Valid TACH Count Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	LOCK	DEFAULT
88h	R/W	Valid TACH Count 1	4096	2048	1024	512	256	128	64	32	SWL	SWL	F5h
98h	R/W	Valid TACH Count 2	4096	2048	1024	512	256	128	64	32	SWL	SWL	F5h

The Valid TACH Count Registers store the maximum TACH Reading Register value to indicate that the each fan is spinning properly. The value is referenced at the end of the Spin Up Routine to determine if the fan has started operating and decide if the device needs to retry. See Equation [2] for translating the RPM to a count.

If the TACH Reading Register value exceeds the Valid TACH Count Register (indicating that the Fan RPM is below the threshold set by this count) then a stalled fan is detected. In this condition, the algorithm will automatically begin its Spin Up Routine.

If a TACH Target setting is set above the Valid TACH Count setting then that setting will be ignored and the algorithm will use the current fan drive setting.

These registers only apply if the Fan Speed Control Algorithm is used.

6.40 Fan Drive Fail Band Registers

Table 6.55 Fan Drive Fail Band Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
89h	R/W	Fan 1 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	SWL	00h
8Ah	R/W	Fan 1 Drive Fail Band High Byte	4096	2048	1024	512	256	128	64	32	SWL	00h
99h	R/W	Fan 2 Drive Fail Band Low Byte	16	8	4	2	1	-	-	-	SWL	00h
9Ah	R/W	Fan 2 Drive Fail Band High Byte	4096	2048	1024	512	256	128	64	32	SWL	00h

The Fan Drive Fail Band Registers store the number of tach counts used by the Fan Drive Fail detection circuitry. This circuitry is activated when the fan drive setting high byte is at FFh. When it is enabled, the actual measured fan speed is compared against the target fan speed.

This circuitry is used to indicate that the target fan speed at full drive is higher than the fan is actually capable of reaching. If the measured fan speed does not exceed the target fan speed minus the Fan Drive Fail Band Register settings for a period of time longer than set by the DRIVE_FAIL_CNTx[1:0] bits then the DRIVE_FAIL status bit will be set and an interrupt generated.

These registers only apply if the Fan Speed Control Algorithm is used.

6.41 TACH Target Registers

Table 6.56 TACH Target Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
8Bh	R/W	TACH Target 1 Low Byte	16	8	4	2	1	-	-	-	No	F8h
8Ch	R/W	TACH Target 1 High Byte	4096	2048	1024	512	256	128	64	32	No	FFh
9Bh	R/W	TACH Target 2 Low Byte	16	8	4	2	1	-	-	-	No	F8h
9Ch	R/W	TACH Target 2 High Byte	4096	2048	1024	512	256	128	64	32	No	FFh

The TACH Target Registers hold the target tachometer value that is maintained each of the RPM based Fan Control Algorithms.

If one of the algorithms is enabled and then setting the TACH Target Register High Byte to FFh will disable the fan driver (or set the PWM duty cycle to 0%). Setting the TACH Target to any other value (from a setting of FFh) will cause the algorithm to invoke the Spin Up Routine after which it will function normally.

These registers only apply if the Fan Speed Control Algorithm is used.

These registers are synchronized in that the TACH Target is not applied until the high byte is written.

6.42 TACH Reading Registers

Table 6.57 TACH Reading Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
8Dh	R/W	Fan 1 TACH Reading High Byte	4096	2048	1024	512	256	128	64	32	No	FFh
8Eh	R/W	Fan 1 TACH Reading Low Byte	16	8	4	2	1	-	-	-	No	F8h
9Dh	R/W	Fan 2 TACH Reading High Byte	4096	2048	1024	512	256	128	64	32	No	FFh
9Eh	R/W	Fan 2 TACH Reading Low Byte	16	8	4	2	1	-	-	-	No	F8h

The TACH Reading Registers' contents describe the current tachometer reading for each of the fan. By default, the data represents the fan speed as the number of 32.768kHz clock periods that occur for a single revolution of the fan.

Equation [2] shows the detailed conversion from tachometer measurement (COUNT) to RPM while Equation [3] shows the simplified translation of TACH Reading Register count to RPM assuming a 2-pole fan, measuring 5 edges, with a frequency of 32.768kHz.

These registers are synchronized. Any time that the high byte is read, the low byte is placed into an internal shadow register so that when the low byte is read, it will always be associated with the high byte. The low byte need not be read.

$$RPM = \frac{1}{(poles)} \times \frac{(n-1)}{COUNT \times \frac{1}{m}} \times f_{TACH} \times 60$$

where:

poles = number of poles of the fan (typically 2)

f_{TACH} = the frequency of the tachometer measurement clock (typically 32.768kHz)

n = number of edges measured (typically 5 for a 2 pole fan)

m = the multiplier defined by the RANGE bits

COUNT = TACH Reading Register value (in decimal)

[2]

$$RPM = \frac{3{,}932{,}160 \times m}{COUNT}$$

[3]

Note 6.2 The vdd_RTC power domain may read lower than the actual value. This is due to a fix in the testmux block in the analog to block RTC current into a parasitic diode when VDD is removed.

6.43 Product ID Register (FDh)

Table 6.58 Product ID Register

ADDR	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	LOCK	DEFAULT
FDh	Product ID Register	0	0	0	1	0	0	1	1	No	13h

The Product ID Register contains a unique 8 bit word that identifies the product.

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Chapter 7 Package Diagram

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

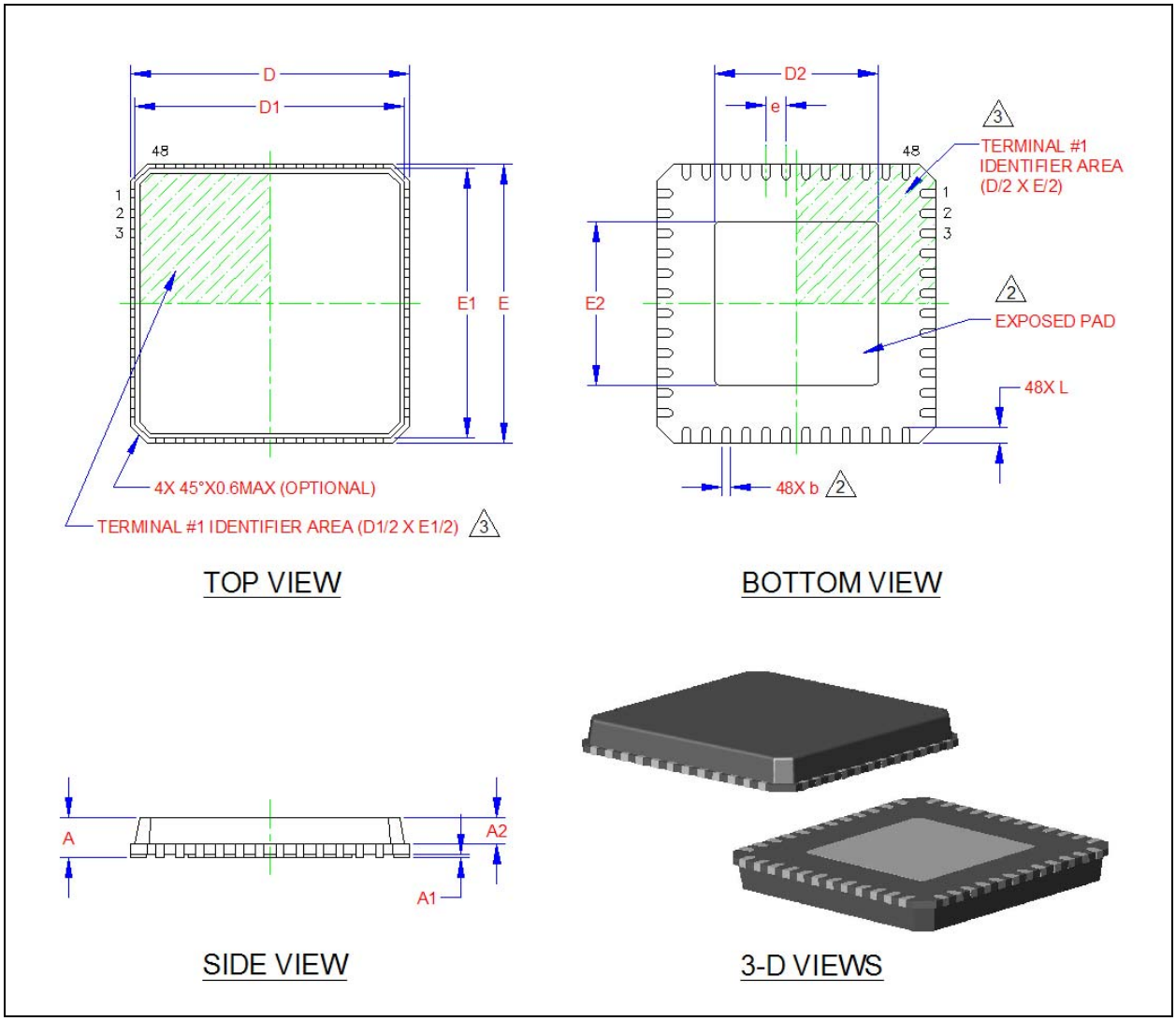

Figure 7.1 48-Pin QFN 7mm x 7mm Package Drawing

Table 7.1 48-Pin QFN 7mm x 7mm Package Dimensions

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	-	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	-	-	0.90	-	MOLD CAP THICKNESS
D/E	6.85	7.00	7.15	-	X/Y BODY SIZE
D1/E1	6.55	-	6.95	-	X/Y MOLD CAP SIZE
D2/E2	SEE VARIATIONS			2	X/Y EXPOSED PAD SIZE
L	0.30	-	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e	0.50 BSC			-	TERMINAL PITCH

D2/E2 VARIATIONS				
MIN	NOM	MAX	NOTE	CATALOG PART #
3.95	4.10	4.25	-	USB2503, USB2503A & EMC4001

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Chapter 8 XOR Test Tree

The EMC4002 contains an XOR test tree that can be used to verify system connectivity of all digital pins. The XOR test tree is enabled by asserting the XEN pin high at any time. Once the XOR test tree is enabled, driving any of the inputs to a '1' will cause the output to be asserted to '1'. Enabling the XOR test tree will not affect the register contents and will not reset the device.

Due to the XOR functionality, any odd number of inputs high forces the output high, and any even number of inputs high forces the output low.

8.1 Inputs

The XOR Test Tree inputs are:

1. ATF_INT# / BC-LINK_IRQ#
2. THERMTRIP_SIO / PWM1 / GPIO5
3. ACAVAIL_CLR
4. POWER_SW#
5. THERMTRIP1#
6. THERMTRIP2#
7. THERMTRIP3#
8. 3V_PWROK#
9. PWM2 / GPIO1
10. TACH2 / GPIO4
11. TACH1 / GPIO3
12. CLK_IN / GPIO2
13. SMDATA / BC-LINK_DATA
14. SMCLK / BC-LINK_CLK
15. VDD_PWRGD
16. LDO_POK
17. LDO_SHDN#

8.2 Output

The XOR Test Tree output is the SYS_SHDN# pin.

8.3 Enabling/Disabling

The XOR test tree is enabled by driving the ADDR_SEL / XEN pin to +5V at any time. When the ADDR_SEL / XEN pin is returned to a value $\leq$ 3.3V, then the XOR test tree is removed. Changing the ADDR_SEL / XEN pin will not affect the ThermTrip logic selection (which is latched upon power up).

Appendix AThermistors

The EMC4002 can monitor thermistor inputs on VCP1, VCP2, VIN1, and VIN2 pins as well as supporting a thermistor option on the DP1/ VREF_T and DN1 / THERM pins. The Thermistors can be connected as shown in Figure A.1.

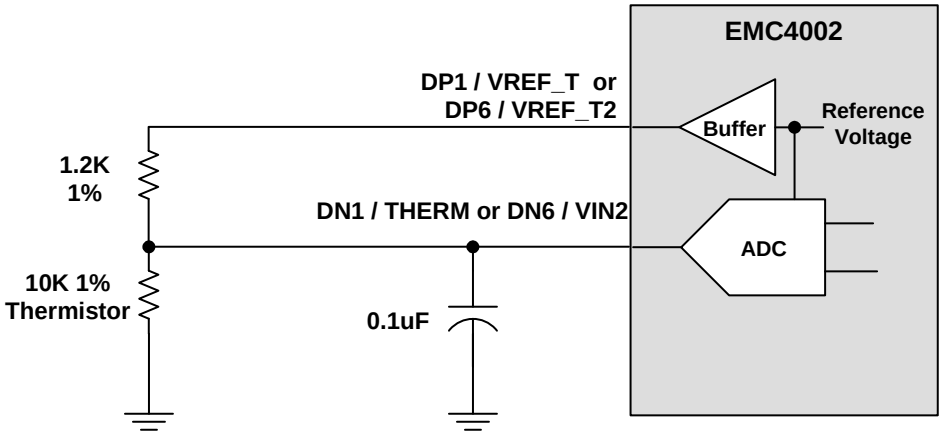

Figure A.1 “Low Side” Thermistor Connection

The relationship between voltage and temperature is roughly linear. The measured voltage by the EMC4002 will be inversely proportional to temperature (as shown in the example depicted in Figure A.1).

For a 10k Ohm type 3370 Thermistor and a 1.2k ohm ±1% setting resistor, the output response corresponding to a thermistor configured as shown in Figure A.1 is tabulated in Table A.1. This table only applies for the VIN2 input if it is not inverted. The THERM input and the inverted VIN2 input output response is tabulated in Table A.2.

The EMC4002 does not perform any numerical calculations on the thermistor value if a thermistor is monitored on VCP1, VCP2, VIN1, or VIN2. If the External Diode 1 channel is configured to monitor a thermistor, it must be configured as shown in Figure A.1.

A.1 Thermistor Look Up Tables

Table A.1 “Low Side” Thermistor Look Up Table

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-45	254	15	235	75	157	135	72
-44	253	16	235	76	155	136	71
-43	253	17	234	77	154	137	70
-42	253	18	233	78	152	138	69
-41	253	19	232	79	150	139	68
-40	253	20	231	80	148	140	67

Table A.1 "Low Side" Thermistor Look Up Table (continued)

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-39	253	21	231	81	146	141	66
-38	253	22	230	82	145	142	65
-37	252	23	229	83	143	143	64
-36	252	24	228	84	141	144	63
-35	252	25	227	85	139	145	62
-34	252	26	226	86	138	146	61
-33	252	27	225	87	136	147	60
-32	252	28	224	88	135	148	59
-31	252	29	223	89	133	149	59
-30	252	30	222	90	131	150	58
-29	251	31	221	91	129	151	57
-28	251	32	220	92	128	152	56
-27	251	33	219	93	126	153	55
-26	251	34	218	94	124	154	54
-25	251	35	217	95	123	155	54
-24	251	36	216	96	121	156	53
-23	250	37	215	97	119	157	52
-22	250	38	213	98	118	158	51
-21	250	39	212	99	116	159	51
-20	250	40	211	100	114	160	50
-19	250	41	210	101	113	161	49
-18	249	42	208	102	111	162	48
-17	249	43	207	103	110	163	48
-16	249	44	206	104	108	164	47
-15	249	45	205	105	106	165	46
-14	248	46	203	106	105	166	46
-13	248	47	202	107	103	167	45
-12	248	48	200	108	102	168	44
-11	247	49	199	109	100	169	44
-10	247	50	198	110	99	170	43
-9	247	51	196	111	97	171	43
-8	246	52	195	112	96	172	42

Table A.1 "Low Side" Thermistor Look Up Table (continued)

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-7	246	53	193	113	95	173	41
-6	246	54	192	114	93	174	41
-5	245	55	190	115	92	175	40
-4	245	56	189	116	90	176	40
-3	245	57	187	117	89	177	39
-2	244	58	185	118	88	178	38
-1	244	59	184	119	86	179	38
0	243	60	182	120	85	180	37
1	243	61	181	121	84	181	37
2	243	62	179	122	82	182	36
3	242	63	177	123	81	183	36
4	242	64	176	124	80	184	35
5	241	65	174	125	79	185	35
6	241	66	172	126	82	186	34
7	240	67	171	127	81	187	34
8	240	68	169	128	80	188	33
9	239	69	167	129	78	189	33
10	238	70	166	130	77	190	32
11	238	71	164	131	76	191	32
12	237	72	162	132	75		
13	237	73	160	133	74		
14	236	74	159	134	73		

Table A.2 Inverted Thermistor Look Up Table

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-45	0	15	19	75	97	135	182
-44	1	16	20	76	99	136	183
-43	1	17	20	77	100	137	184
-42	1	18	21	78	102	138	185
-41	1	19	22	79	104	139	186
-40	1	20	23	80	106	140	187

Table A.2 Inverted Thermistor Look Up Table (continued)

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-39	1	21	23	81	108	141	188
-38	1	22	24	82	109	142	189
-37	2	23	25	83	111	143	190
-36	2	24	26	84	113	144	191
-35	2	25	27	85	115	145	192
-34	2	26	28	86	116	146	193
-33	2	27	29	87	118	147	194
-32	2	28	30	88	120	148	195
-31	2	29	31	89	121	149	195
-30	2	30	32	90	123	150	196
-29	3	31	33	91	125	151	197
-28	3	32	34	92	126	152	198
-27	3	33	35	93	128	153	199
-26	3	34	36	94	130	154	200
-25	3	35	37	95	131	155	200
-24	3	36	38	96	133	156	201
-23	4	37	39	97	135	157	202
-22	4	38	41	98	136	158	203
-21	4	39	42	99	138	159	203
-20	4	40	43	100	140	160	204
-19	4	41	44	101	141	161	205
-18	5	42	46	102	143	162	206
-17	5	43	47	103	144	163	206
-16	5	44	48	104	146	164	207
-15	5	45	50	105	148	165	208
-14	6	46	51	106	149	166	208
-13	6	47	52	107	151	167	209
-12	6	48	54	108	152	168	210
-11	7	49	55	109	154	169	210
-10	7	50	56	110	155	170	211
-9	7	51	58	111	157	171	211
-8	8	52	59	112	158	172	212

Table A.2 Inverted Thermistor Look Up Table (continued)

T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE	T (°C)	ADC CODE
-7	8	53	61	113	159	173	213
-6	8	54	62	114	161	174	213
-5	9	55	64	115	162	175	214
-4	9	56	65	116	164	176	214
-3	9	57	67	117	165	177	215
-2	10	58	69	118	166	178	216
-1	10	59	70	119	168	179	216
0	11	60	72	120	169	180	217
1	11	61	73	121	170	181	217
2	11	62	75	122	172	182	218
3	12	63	77	123	173	183	218
4	12	64	78	124	174	184	219
5	13	65	80	125	175	185	219
6	13	66	82	126	172	186	220
7	14	67	83	127	173	187	220
8	15	68	85	128	174	188	221
9	15	69	87	129	176	189	221
10	16	70	88	130	177	190	222
11	16	71	90	131	178	191	222
12	17	72	92	132	179		
13	18	73	94	133	180		
14	18	74	95	134	181		

Appendix B RPM to Tachometer Count Look Up Tables

B.1 1k RPM Range

The Look Up Table is an example based on the assumption that the fan being measured has 2-poles and is measuring 5 edges using the 1k RPM range settings. The data presented in the reading is only the high byte data and the decimal count value only represents high byte data.

Table B.1 Tachometer Count to RPM Look Up Table (Range = 1000 RPM)

TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)	TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)
0	00	Disabled	4096	80	1920
32	01	245760	4128	81	1905
64	02	122880	4160	82	1890
96	03	81920	4192	83	1876
128	04	61440	4224	84	1862
160	05	49152	4256	85	1848
192	06	40960	4288	86	1834
224	07	35109	4320	87	1820
256	08	30720	4352	88	1807
288	09	27307	4384	89	1794
320	0A	24576	4416	8A	1781
352	0B	22342	4448	8B	1768
384	0C	20480	4480	8C	1755
416	0D	18905	4512	8D	1743
448	0E	17554	4544	8E	1731
480	0F	16384	4576	8F	1719
512	10	15360	4608	90	1707
544	11	14456	4640	91	1695
576	12	13653	4672	92	1683
608	13	12935	4704	93	1672
640	14	12288	4736	94	1661
672	15	11703	4768	95	1649
704	16	11171	4800	96	1638
736	17	10685	4832	97	1628

Table B.1 Tachometer Count to RPM Look Up Table (Range = 1000 RPM) (continued)

TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)	TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)
768	18	10240	4864	98	1617
800	19	9830	4896	99	1606
832	1A	9452	4928	9A	1596
864	1B	9102	4960	9B	1586
896	1C	8777	4992	9C	1575
928	1D	8474	5024	9D	1565
960	1E	8192	5056	9E	1555
992	1F	7928	5088	9F	1546
1024	20	7680	5120	A0	1536
1056	21	7447	5152	A1	1526
1088	22	7228	5184	A2	1517
1120	23	7022	5216	A3	1508
1152	24	6827	5248	A4	1499
1184	25	6642	5280	A5	1489
1216	26	6467	5312	A6	1480
1248	27	6302	5344	A7	1472
1280	28	6144	5376	A8	1463
1312	29	5994	5408	A9	1454
1344	2A	5851	5440	AA	1446
1376	2B	5715	5472	AB	1437
1408	2C	5585	5504	AC	1429
1440	2D	5461	5536	AD	1421
1472	2E	5343	5568	AE	1412
1504	2F	5229	5600	AF	1404
1536	30	5120	5632	B0	1396
1568	31	5016	5664	B1	1388
1600	32	4915	5696	B2	1381
1632	33	4819	5728	B3	1373
1664	34	4726	5760	B4	1365
1696	35	4637	5792	B5	1358
1728	36	4551	5824	B6	1350

Table B.1 Tachometer Count to RPM Look Up Table (Range = 1000 RPM) (continued)

TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)	TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)
1760	37	4468	5856	B7	1343
1792	38	4389	5888	B8	1336
1824	39	4312	5920	B9	1328
1856	3A	4237	5952	BA	1321
1888	3B	4165	5984	BB	1314
1920	3C	4096	6016	BC	1307
1952	3D	4029	6048	BD	1300
1984	3E	3964	6080	BE	1293
2016	3F	3901	6112	BF	1287
2048	40	3840	6144	C0	1280
2080	41	3781	6176	C1	1273
2112	42	3724	6208	C2	1267
2144	43	3668	6240	C3	1260
2176	44	3614	6272	C4	1254
2208	45	3562	6304	C5	1248
2240	46	3511	6336	C6	1241
2272	47	3461	6368	C7	1235
2304	48	3413	6400	C8	1229
2336	49	3367	6432	C9	1223
2368	4A	3321	6464	CA	1217
2400	4B	3277	6496	CB	1211
2432	4C	3234	6528	CC	1205
2464	4D	3192	6560	CD	1199
2496	4E	3151	6592	CE	1193
2528	4F	3111	6624	CF	1187
2560	50	3072	6656	D0	1182
2592	51	3034	6688	D1	1176
2624	52	2997	6720	D2	1170
2656	53	2961	6752	D3	1165
2688	54	2926	6784	D4	1159
2720	55	2891	6816	D5	1154

Table B.1 Tachometer Count to RPM Look Up Table (Range = 1000 RPM) (continued)

TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)	TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)
2752	56	2858	6848	D6	1148
2784	57	2825	6880	D7	1143
2816	58	2793	6912	D8	1138
2848	59	2761	6944	D9	1133
2880	5A	2731	6976	DA	1127
2912	5B	2701	7008	DB	1122
2944	5C	2671	7040	DC	1117
2976	5D	2643	7072	DD	1112
3008	5E	2614	7104	DE	1107
3040	5F	2587	7136	DF	1102
3072	60	2560	7168	E0	1097
3104	61	2534	7200	E1	1092
3136	62	2508	7232	E2	1087
3168	63	2482	7264	E3	1083
3200	64	2458	7296	E4	1078
3232	65	2433	7328	E5	1073
3264	66	2409	7360	E6	1069
3296	67	2386	7392	E7	1064
3328	68	2363	7424	E8	1059
3360	69	2341	7456	E9	1055
3392	6A	2318	7488	EA	1050
3424	6B	2297	7520	EB	1046
3456	6C	2276	7552	EC	1041
3488	6D	2255	7584	ED	1037
3520	6E	2234	7616	EE	1033
3552	6F	2214	7648	EF	1028
3584	70	2194	7680	F0	1024
3616	71	2175	7712	F1	1020
3648	72	2156	7744	F2	1016
3680	73	2137	7776	F3	1011
3712	74	2119	7808	F4	1007

Table B.1 Tachometer Count to RPM Look Up Table (Range = 1000 RPM) (continued)

TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)	TACH COUNT (DECIMAL)	HIGH BYTE REGISTER READING (HEX)	FAN SPEED (RPM)
3744	75	2101	7840	F5	1003
3776	76	2083	7872	F6	999
3808	77	2065	7904	F7	995
3840	78	2048	7936	F8	991
3872	79	2031	7968	F9	987
3904	7A	2014	8000	FA	983
3936	7B	1998	8032	FB	979
3968	7C	1982	8064	FC	975
4000	7D	1966	8096	FD	971
4032	7E	1950	8128	FE	968
4064	7F	1935	8160	FF	Fan Stopped

Chapter 9 EMC4002 Data Sheet Revision History

Table 9.1 Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
REV A (03-05-14)	REV A replaces previous SMSC version Rev. 1.03 (03-07-08)	

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