2.5A Synchronous Buck Li-ion Battery Charger

General Description

The EMC5090 is a switch mode lithium-ion battery charger. It utilities a 1.5MHz synchronous buck converter topology to reduce power dissipation during charging. The internal MOS switch delivers current up to 2.5A to charge the battery. The built in pre-charge safety timer automatically terminates charging once the adjustable time limit has been reached. The EMC5090 includes complete charge termination circuitry, automatic recharge and a ±1% of 4.2V float voltage.

This device is available in packages of TQFN-16L (4mmx4mm) for space-saving application.

Features

- 2.5A maximum Charge Current
- No external MOSFET, sense resistor or blocking Diode Required
- Programmable Trickle Charge Termination Timer
- Programmable Charge Current
- Programmable End-of-Charge Current
- Automatic Recharge
- Thermistor Input for Temperature Qualified Charging

Applications

- PDAs, Tablet, Cell Phones and Smart Phones
- Digital Camera, MP3 and Handheld Gamming
- Portable Instruments including Medical Handhelds
- Self-Charging Battery Packs
- Stand-Alone Chargers or USB Port Chargers

Typical Application

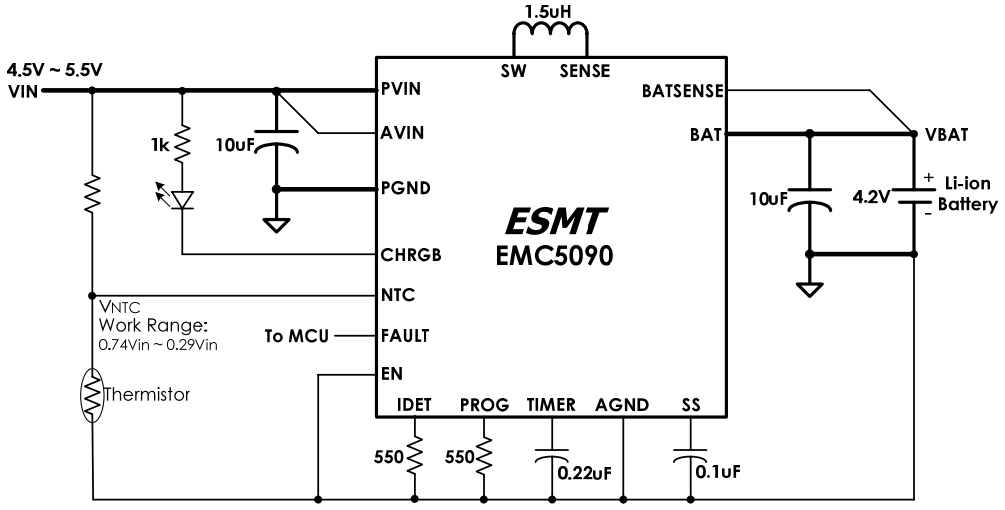
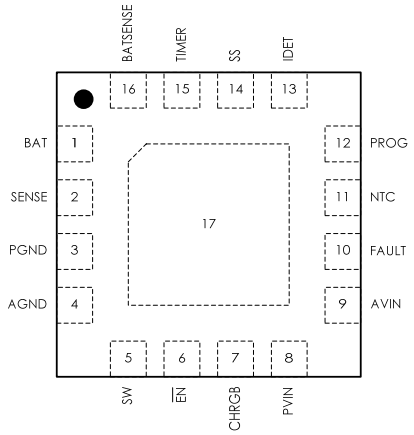


Fig. 1

Package Configuration

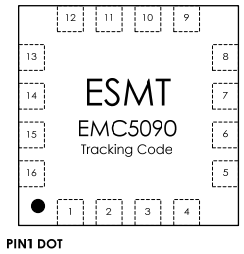


TQFN-16L (4x4mm)

EMC5090-42HI16NRR

42	Output Voltage
HI16	TQFN-16L (4x4mm) Package
NRR	RoHS & Halogen free package
	Commercial Grade Temperature
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
TQFN-16L (4x4mm)	4.2V	EMC5090-42HI16NRR		Tape & Reel 3K units

Function Blocks

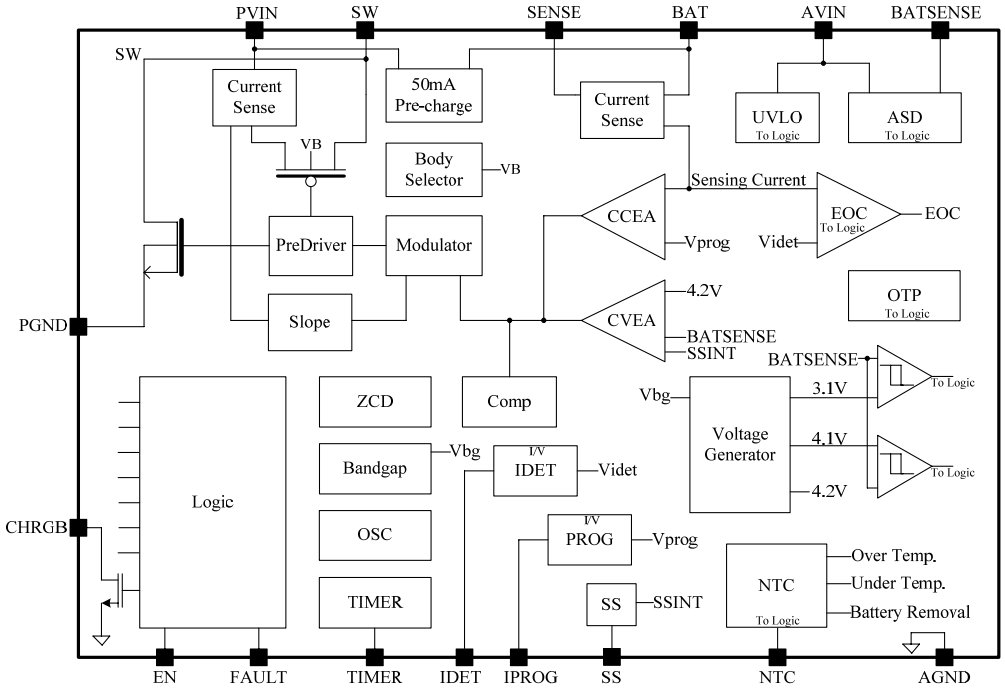


Fig. 2

Pin Functions

Pin Name	TQFN-16L	Function
BAT	1	Battery Charger Output terminal.
SENSE	2	Current Sense Node, Connect to external inductor
PGND	3	Power Ground
AGND	4	Ground Sense. Connect this pin to the battery negative battery termination
SW	5	Switch Node.
EN	6	Chip enable pin
CHRGB	7	Open Drain Charge Status Output
PVIN	8	Positive Supply Voltage Input
AVIN	9	Positive Supply Sense Input
FAULT	10	Battery Fault Indicator
NTC	11	Termistor Temperature Monitoring Circuit.
PROG	12	Program Charge Current
IDET	13	Program End of Charge Threshold
SS	14	Programmable Soft start
TIMER	15	Programmable Trickle Charge Timer
BATSENSE	16	Battery Sense Input
EXPOSED	17	Ground

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

IN ---------- – 0.3V to 6.5V
EN ---------- – 0.3V to V_{IN} + 0.3V)
Other Pin Voltage ---------- – 0.3V to (V_{IN} + 0.3V)
Charger Current ---------- 2.5A
Lead Temperature (Soldering, 10 sec)---------- 260°C

Operating Temperature Range ---------- –40°C to 85°C
Junction Temperature (Note 1) ---------- 150°C
Storage Temperature Range ---------- – 65°C to 150°C
ESD Susceptibility HBM ---------- 2KV
MM ---------- 200V

Thermal data

Package	Thermal resistance	Parameter	Value
TQFN-16L (4x4mm)	θ_{JA} (Note 2)	Junction-ambient	45°C/W
	θ_{JT} (Note 3)	Junction-case	26°C/W

Electrical Characteristics

V_{IN}=5V and T_A = 25°C for the typical values. unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Operating Voltage Range	V_{IN}		4.0		5.5	V
	I_{IN}	PV_{IN} Connected to $V_{INSENSE}$, PROG and IDET Pins Open, Charger On		550	2000	uA
		Shutdown, $\overline{EN}$ = VIN			50	uA
VBAT Regulated Float Voltage	V_{FLOAT}	Measured from BATSENS to GNDSENS	4.158	4.2	4.242	V
Switching Mode Charge Current	I_{BAT}	R_{PROG}=440ohm, VBAT=3.5V	2.25	2.5	2.75	A
		R_{PROG}=1100ohm, VBAT=3.5V	0.9	1	1.1	A
		Shutdown, $\overline{EN}$ = VIN			±5	uA
Trickle Charge Current	I_{TRIKL}	VBAT=2V	35	50	65	mA
Trickle Charge Threshold	V_{TRIKL}	VBAT Rising	2.85	2.9	3.0	V
		VBAT Falling	2.65	2.8	2.85	
Under Voltage Lockout Voltage	V_{UVLO}	V_{IN} Rising, Measured from $V_{INSENSE}$ to GNDSENS	2.7		2.82	V
UVLO Hysteresis	ΔV_{UVLO}	Measured from $V_{INSENSE}$ to GNDSENS		100		mV
Automatic Shutdown Threshold voltage	V_{ASD}	$V_{INSENSE}$ – $V_{BATSENS}$ Rising (Turn-On), VBATSENSE = 4V	200	250	300	mV
		$V_{INSENSE}$ – $V_{BATSENS}$ Falling(Turn-Off), VBATSENSE = 4V	15	30	60	
R_{DSON} of PMOS	R_{PFET}	Measured from PV_{IN} to SW		85		mΩ
R_{DSON} of NMOS	R_{NFET}	Measured from SW to PGND		65		mΩ
Timer Accuracy	t_{TIMER}	C_{TIMER}=0.22uF		±10		%
Enable Input Threshold Voltage	$V\overline{EN}$	$V\overline{EN}$ Rising	0.6	0.8	1	V
Enable Input Voltage Hysteresis	$\Delta V\overline{EN}$			100		mV
PROG Pin Voltage	V_{PROG}	R_{PROG}=550Ω		1.195		V
IDET Pin Voltage	V_{IDET}	R_{IDET}=550Ω		1.195		V
IDET Threshold	I_{IDET}	R_{IDET}=550Ω	150	200	250	mA
CHRGB Pin weak pull down current	$I\overline{CHRG}$	$V\overline{CHRG}$ = 1V	15	30	50	uA
CHRGB Pin Output Low Voltage	$V\overline{CHRG}$	$I\overline{CHRG}$ = 5mA		0.2	0.4	V
Recharge Battery Threshold Voltage	$V_{RECHARGE}$	V_{FLOAT}-V_{RECHRG} V_{BAT} Falling	50	100	135	mV
Soft Start Ramp Current	I_{SS}	V_{BAT} < V_{FLOAT} – 100mV, V_{BAT} Across BATSENS and GNDSENS Pins	6	12.8	16	uA
Oscillator Frequency	f_{OSC}		1.3	1.5	1.7	MHz

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D) * \theta_{JA}$)).

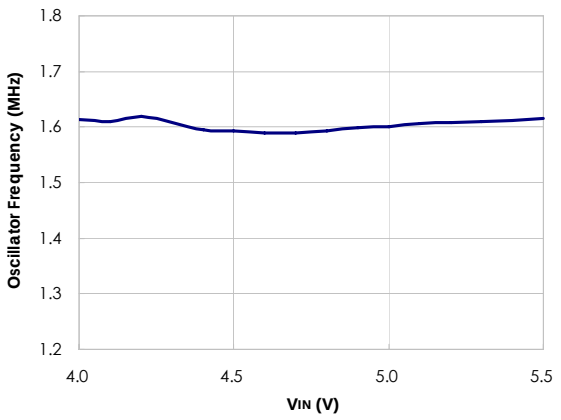
Note 2: θ_{JA} is measured in the natural convection at T_A=25℃ on a highly effective thermal conductivity test board (2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.

Note 3: θ_{JT} represents the heat resistance between the chip and the center of package top.

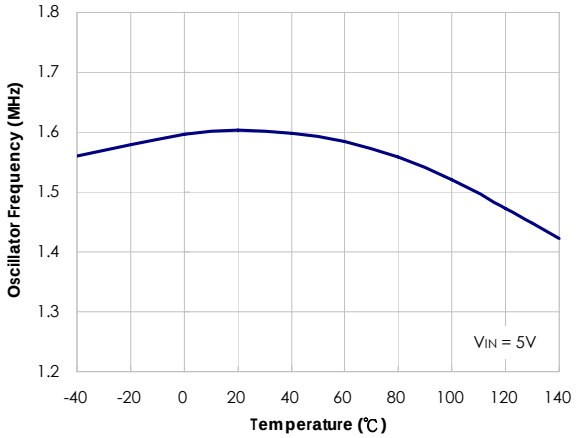
Typical Performance Characteristics

V_{IN}=5V and T_A = 25°C for the typical values. unless otherwise noted.

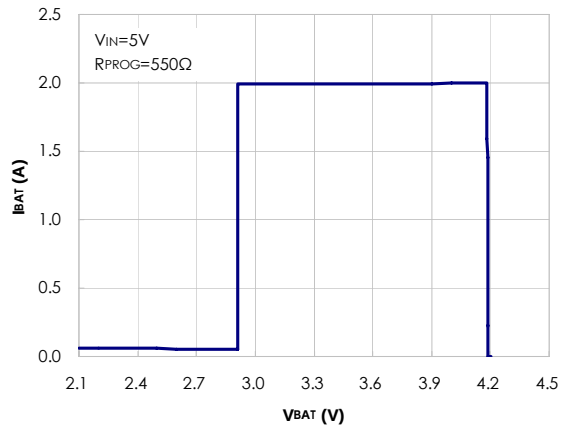
Oscillator Frequency vs. V_{IN} (Fig. 3)



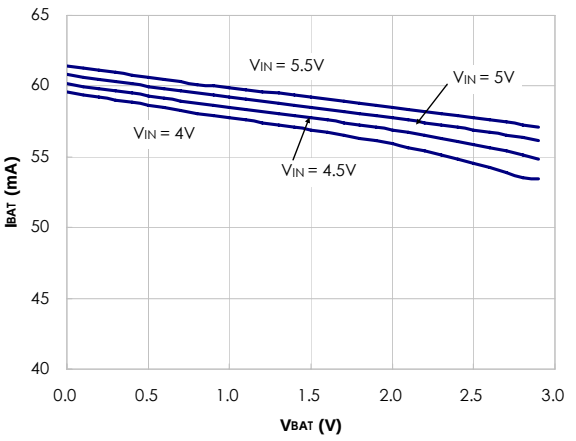
Oscillator Frequency vs. Temperature (Fig. 4)



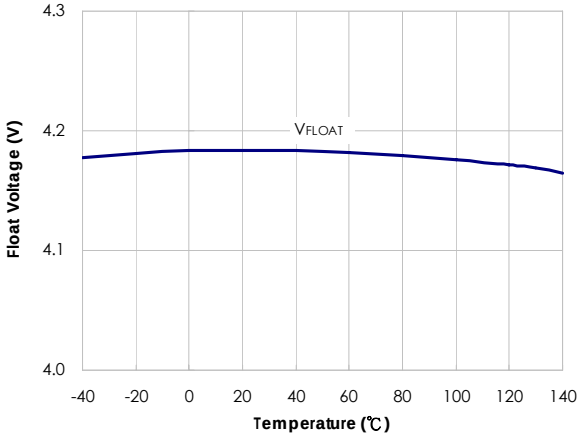
Charge Current vs. Charge Voltage (Fig. 5)



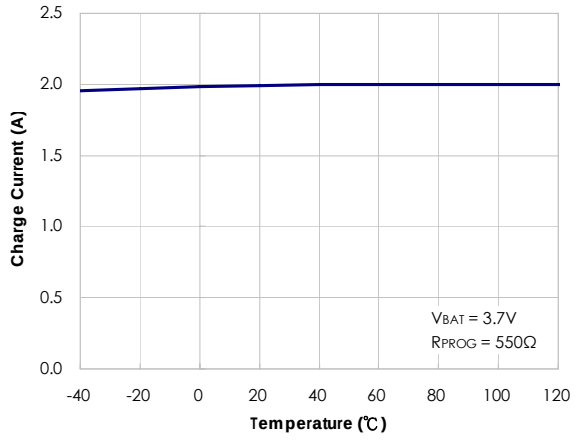
Trickle Charge Current vs. V_{BAT} (Fig. 6)



V_{FLOAT} vs. Temperature (Fig. 7)



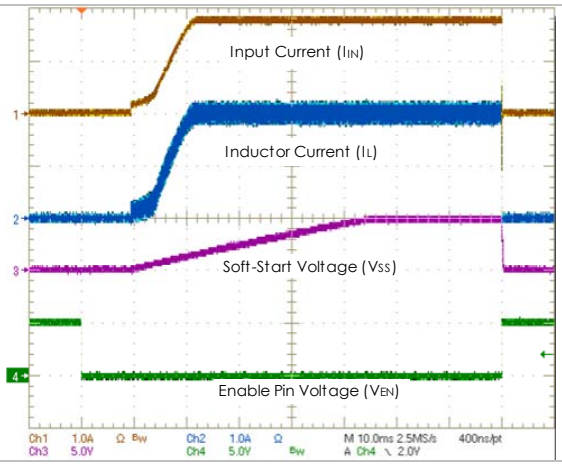
Charge Current vs. Temperature (Fig. 8)



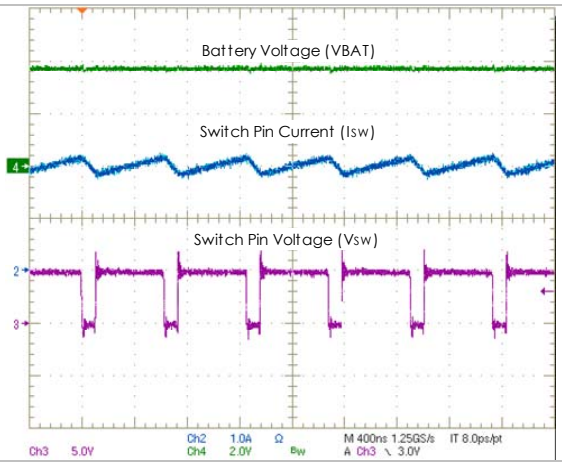
Typical Performance Characteristics

V_{IN}=5V and T_A = 25°C for the typical values. unless otherwise noted.

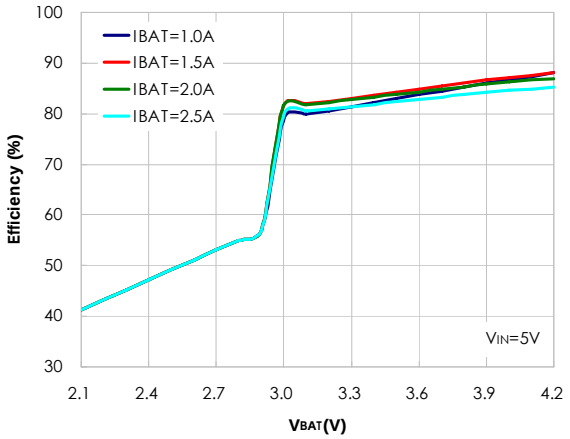
Soft-Start (Fig. 9)



Switching-Mode Operation (Fig.10)



Efficiency vs. V_{BAT} (Fig. 11)



Application Information

Charger Mode Select v.s. Charging Flow.

EMC5090 provides two mode charging applications:

Mode 1: TIMER Pin connects a capacitor to set tickle-charge safety timer.

Mode 1 application provides Trickle Charge and End Of Charge (EOC) Safety Timer, where TIMER pin can adjust timer period. Fig 12 shows. When VBAT is less than 3V trickle charge threshold, the charger goes into 50mA trickle charge mode using a linear charger. In Mode1 application, if trickle charge time longer than Safety Timer setting, charger terminate battery charging operation until VBAT exceed trickle charge threshold 3.1V (3.0V + HYS 0.1V). And the End of charge Timer triggered by VBAT exceeds 4.1V. When VBAT approaches the float voltage, the charge current will start to decrease (CV Mode Regulation). When the charge current drops below end of charge threshold (set via the IDET Pin) for more than 10ms, the CHRGB indication change state. Whatever charge current is lower than EOC Threshold or charging time runs longer than EOC Safety Timer, Both all change CHRGB's state. The Real End of charge only when charger runs reach EOC Safety timer.

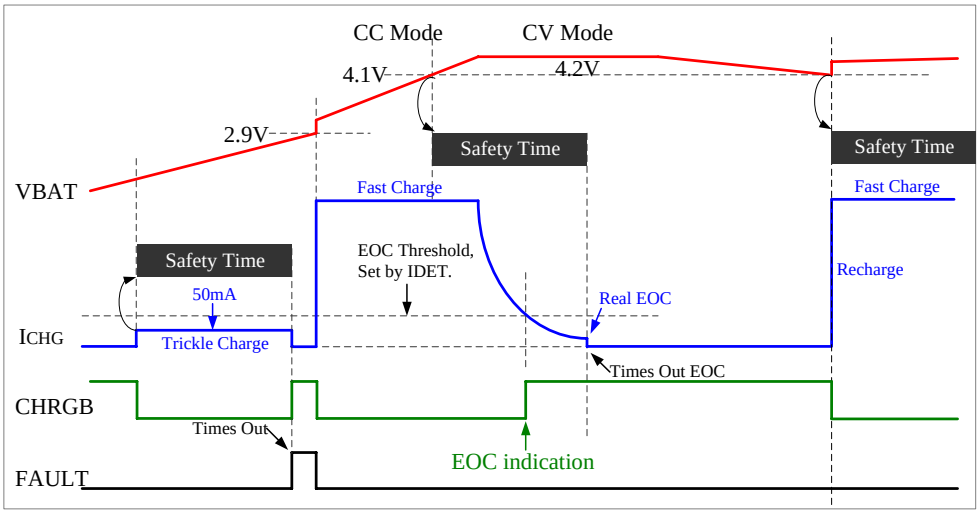


Fig. 12

Mode 2: TIMER Pin connects to AGND to end battery charging when ICHG drops below EOC threshold.

Mode 2 application is the mostly common charger topology. Fig 13 shows the whole charging flow has no safety TIMER. All states charging are determined by VBAT level. VBAT is less than 3.0V into Trickle charge mode, exceeds than 3.1V into Fast-charge mode. When VABT enter into CV Mode, ICHG drops below EOC threshold (set via the IDET Pin) the indication change state and charging terminate until VBAT drops below Recharge voltage threshold (Vfloat's 97.5% ~= 4.1V). A new charge cycle will begin.

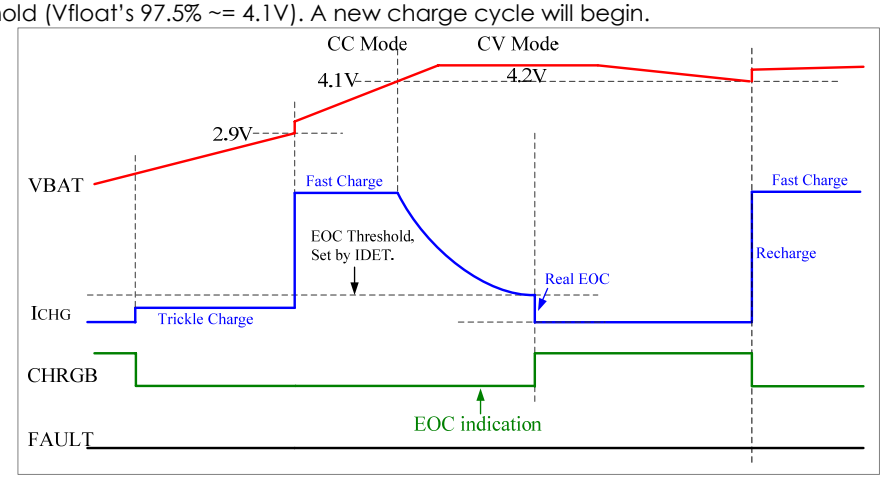


Fig. 13

Mode3: TIMER Pin connects to IDET Pin can disable Safety Timer function. As Fig 14 shown.

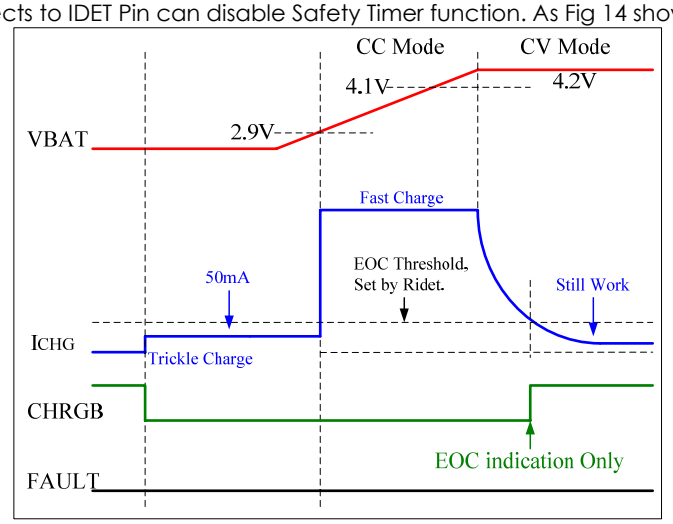


Fig. 14

CHRGB Indicators

Open-Drain Charge States Output. When the battery is being charged, CHRGB is pulled low by an internal NMOS. When the charge current drops below the EOC threshold (Set by R_{IDET}) for more than fixed deglitch time, the NMOS turns off. The EOC signal is latched and reset by initialing a new cycle, which determined by VBAT touch recharge threshold 4.1V or not. When NTC occur, the fault condition causes this pin to blink.

FAULT Indicators

Battery fault indicator. This pin indicated by an internal buffer. When NTC error (temperature Error) or trickle current timer times out occur, fault pin flag will raise. A temperature fault occurs with the temperature monitor circuit enabled and the themistor temperature is either below 0 degC above 50 degC.

NTC Function

Input to the NTC (Negative Temperature Coefficient) Thermistor Temperature Monitoring Circuit. Under normal operation, tie a thermistor from the NTC pin to the AGND pin and a resistor of equal value from NTC to VIN. When the voltage on this pin is above 0.74VIN (Cold, 0°C) or below 0.29VIN (Hot, 50°C), charging is disabled and the CHRG pin blinks. When the voltage on NTC comes back between 0.74VIN and 0.29VIN, the timer continues where it left off and charging resumes. There is approximately 3°C of temperature hysteresis associated with each of the input comparators. **If the NTC function is not used connect the NTC pin to AGND. This will disable all of the NTC functions. NTC should never be pulled above VIN**.

Charge Current Program

The R_{PROG} resistor connects from R_{PROG} pin to AGND, setting the current as follow:

$$I_{CHG} = \frac{1.100k}{R_{PROG}}$$

Where I_{CHG} is the battery charge current which is under switching mode.

For example: Choose 550 Ohm to set I_{CHG}, the fast charging current is 2A.

End of Charge Current Program

Choose R_{IDET} to program end of charge threshold, the threshold equation as follow:

$$I_{EOC} = \frac{0.110k}{R_{IDET}}$$

If R_{IDET} = R_{PROG}, CHRGB provides an I_{CHG}/10 indication equals 200mA.

For example: Choose 1.1k Ohm to set EOC threshold, the threshold is 100mA.

Soft-Start Time Program

The chose Capacitor Css connects from SS to AGND to determine enter switching mode soft start time, the recommend capacitor CSS value is from 0.1uF to 1uF. Css value is not allowed larger than 1uF.

Safety Timer

The Timer period is set by placing a capacitor, C_{TIMER}, to AGND. Set C_{TIMER} to:

$$C_{TIMER} = Time(Hrs) \cdot 0.0733(\mu F)$$

Where time is the desired charging time. Connect TIMER pin to IDET to disable the timer. Connect this pin to AGND to end battery charging when I_{CHG} drops below the IDET setting EOC threshold.

Using Ceramic Input and Output Capacitors

Care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush current through the long wires can potentially cause a voltage spike at V_{IN}, which may large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R or X7R specification. Their dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Over Temperature Protection

The internal high-side MOSFET is turned off when the internal thermal sensor detects that the junction temperature exceeds 165℃, entering the Over Temperature Protection mode (OTP). The OTP mode is unlocked at 130℃, i.e. a 35℃ hysteresis.

Under Voltage Lock Out

The under-voltage lockout (UVLO) circuitry ensures that the EMC5090 starts up with adequate voltage. The regulator output is disabled whenever VIN is below UVLO. The hysteresis of UVLO is designed to be 100 mV.

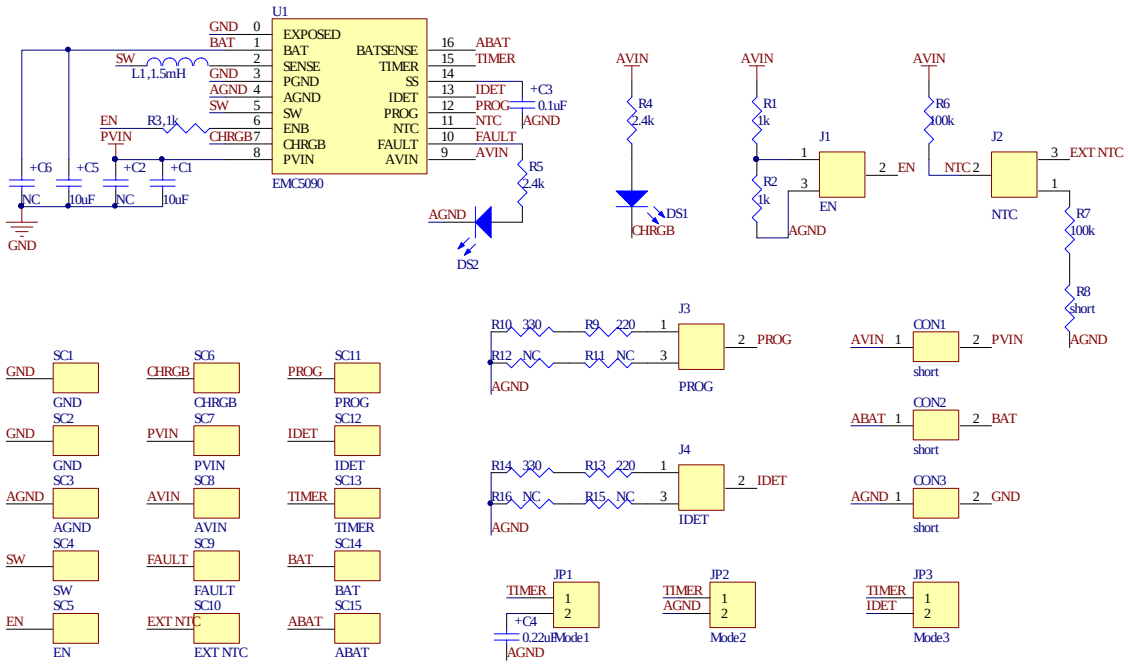
Applications

PCB Layout Guidelines

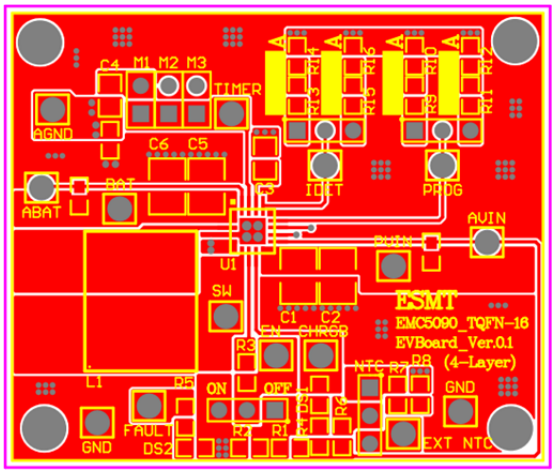
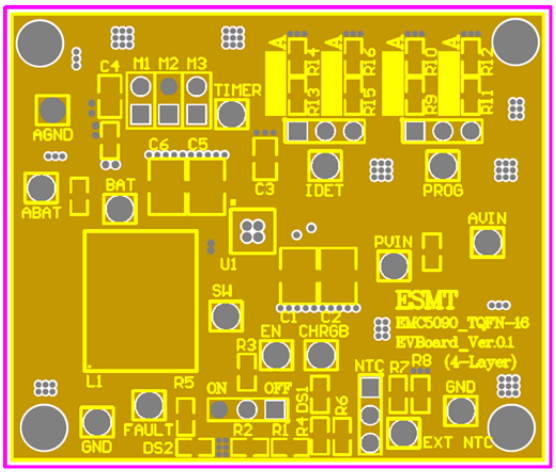
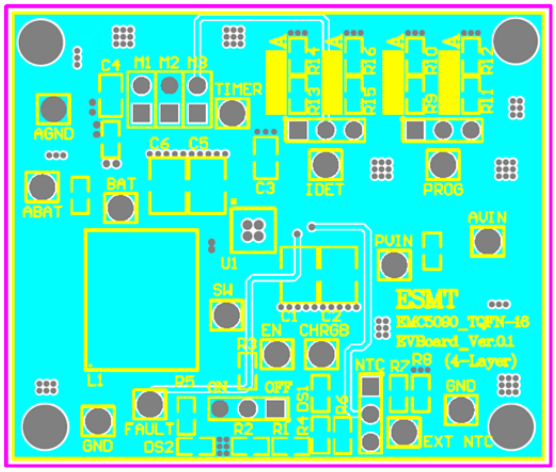
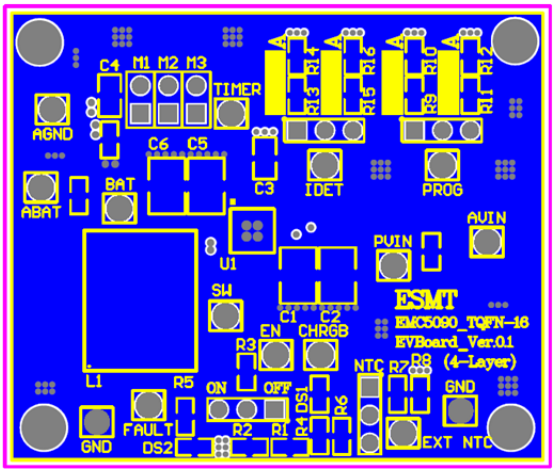
When laying out the printed circuit board, the following checklist should be used to optimize the performance of EMC5090.

1. The input bypass capacitor leads (between PVIN and PGND) should be kept as close as possible.
2. The Exposed Pad should be connected to the ground plane for proper power dissipation.
3. Used a ground plane under the switching circuitry to prevent interplane coupling.
4. All components must return to AGND except the input and output filter capacitors (which should be connected to PGND).

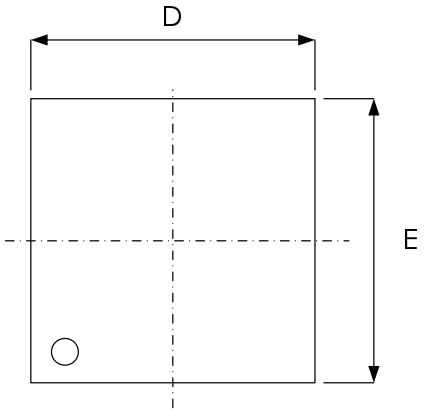
Typical Schematic for PCB Layout



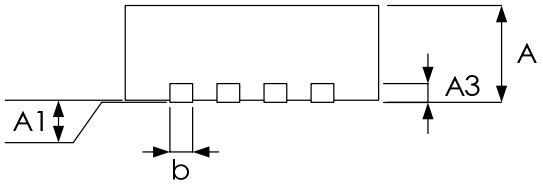
Typical Schematic for PCB Layout (cont.)

Top Layer	Mid-1 Layer
	
Mid-2 Layer	**Bottom Layer**
	

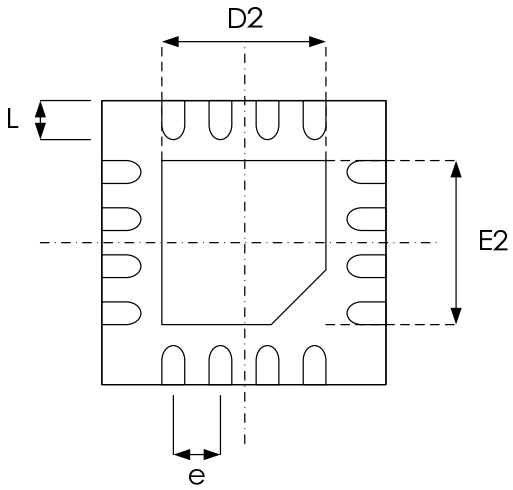
Package Outline Drawing
TQFN-16L (4x4 mm)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.18	0.25
b	0.25	0.35
D	3.90	4.10
E	3.90	4.10
e	0.65 BSC	
L	0.35	0.45

Exposed pad

	Dimension in mm	
	Min	Max
D2	2.00	2.20
E2	2.00	2.20

Revision History

Revision	Date	Description
0.1	2015.10.14	Original version.
1.0	2016.07.28	1.Remove preliminary word and modify version to 1.0 2.Remove TSSOP-16E package product information

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