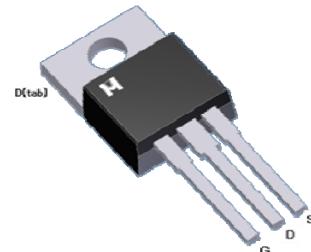
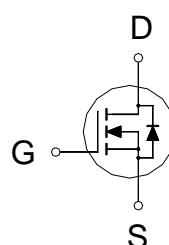


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	60V
R _{DSON} (MAX.)	3.1mΩ
I _D	191A



UIS, R_G 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±30	V
Continuous Drain Current	T _C = 25 °C	I _D	191	A
	T _C = 100 °C		134	
Pulsed Drain Current ¹		I _{DM}	540	
Avalanche Current		I _{AS}	90	
Avalanche Energy	L = 0.1mH, ID=90A, RG=25Ω	E _{AS}	405	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	202	
Power Dissipation	T _C = 25 °C	P _D	277	W
	T _C = 100 °C		111	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=30V, L=0.1mH, V_G=10V, I_L=60A, Rated V_{DS}=60V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	0.45	62.5	°C / W
Junction-to-Ambient	R _{θJA}			

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

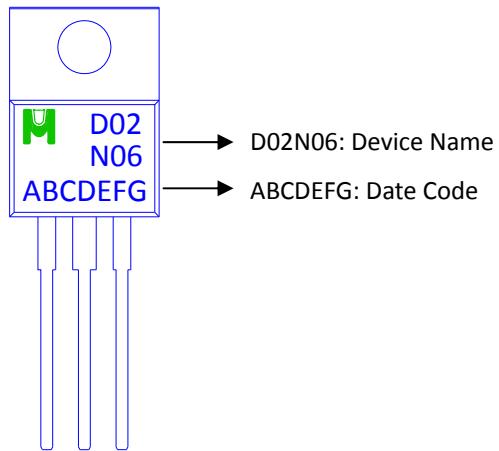
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2	3	4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 30V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48V, V_{GS} = 0V$			1	μA
		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 10V, V_{GS} = 10V$	191			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = 10V, I_D = 50A$		2.8	3.1	$\text{m}\Omega$
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 20A$		62		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 30V, f = 1\text{MHz}$		7935		pF
Output Capacitance	C_{oss}			1082		
Reverse Transfer Capacitance	C_{rss}			248		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		1.7		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 30V, V_{GS} = 10V, I_D = 20A$		91		nC
Gate-Source Charge ^{1,2}	Q_{gs}			50		
Gate-Drain Charge ^{1,2}	Q_{gd}			16		
Turn-On Delay Time ^{1,2}	$t_{d(\text{on})}$	$V_{DS} = 30V, I_D = 20A, V_{GS} = 10V, R_{GS} = 6\Omega$		100		nS
Rise Time ^{1,2}	t_r			180		
Turn-Off Delay Time ^{1,2}	$t_{d(\text{off})}$			110		
Fall Time ^{1,2}	t_f			200		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ\text{C}$)						
Continuous Current	I_S				191	A
Pulsed Current ³	I_{SM}				540	
Forward Voltage ¹	V_{SD}	$I_F = 50A, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 20A, dI_F/dt = 100A/\mu\text{s}$		36		nS
Reverse Recovery Charge	Q_{rr}			280		nC

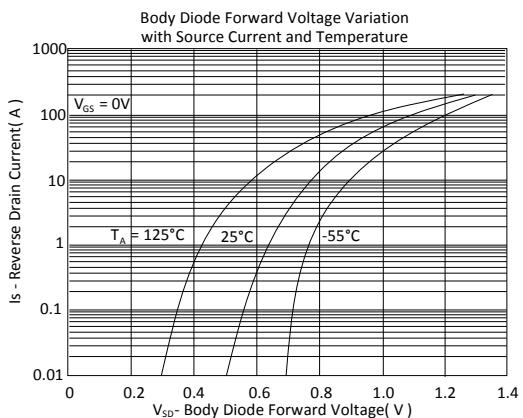
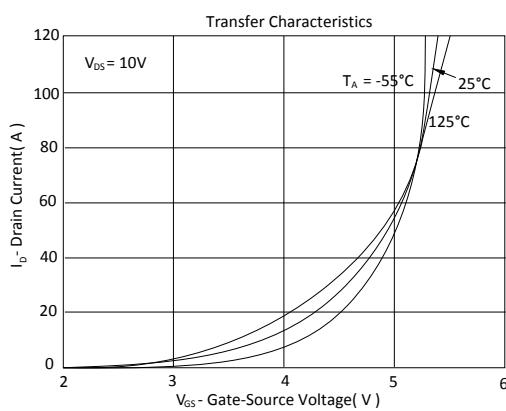
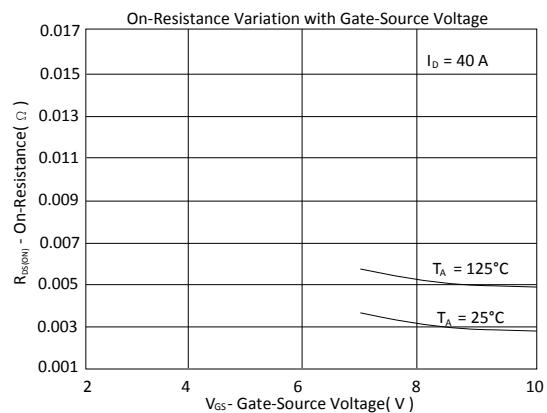
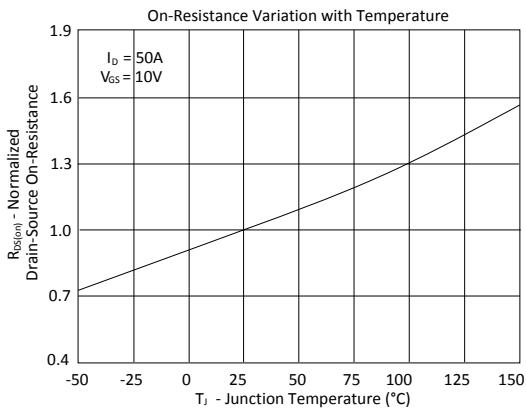
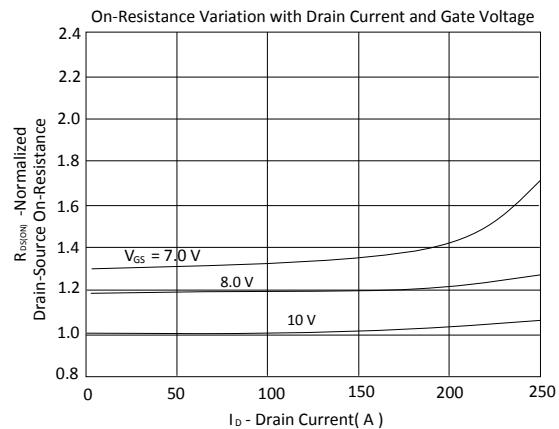
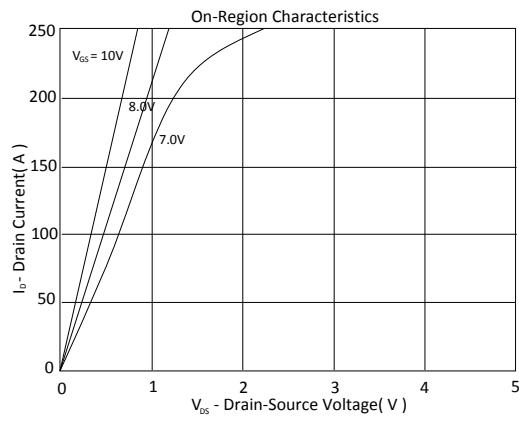
¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.³Pulse width limited by maximum junction temperature.

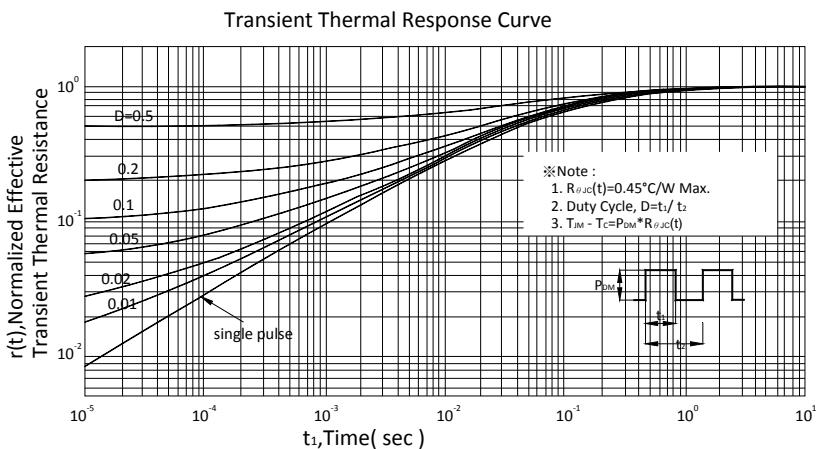
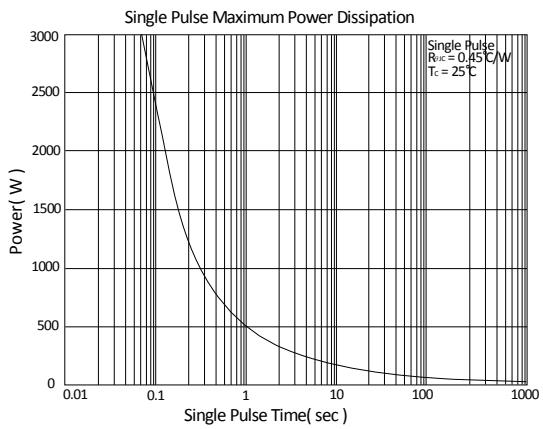
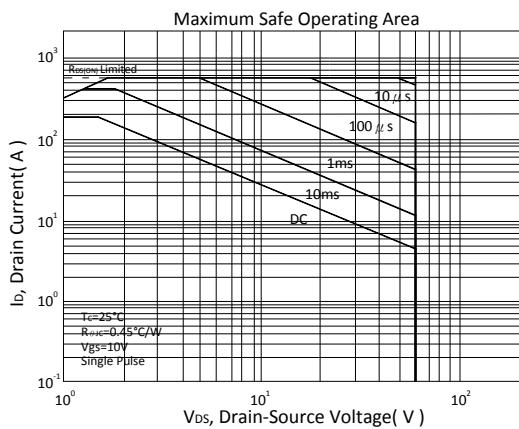
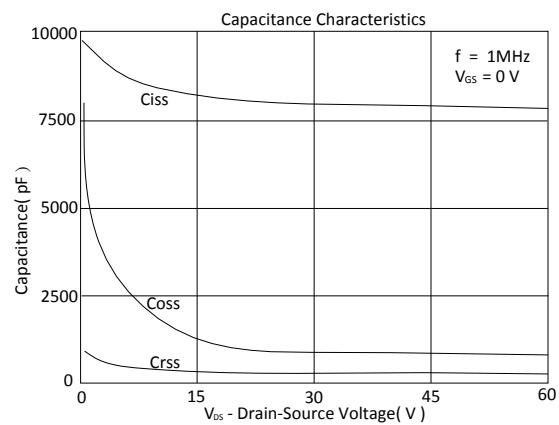
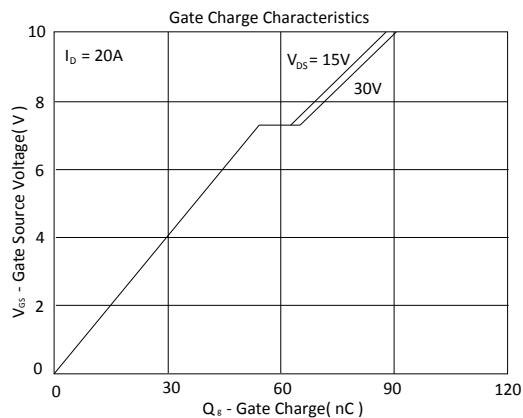
Ordering & Marking Information:

Device Name: EMD02N06E for TO-220

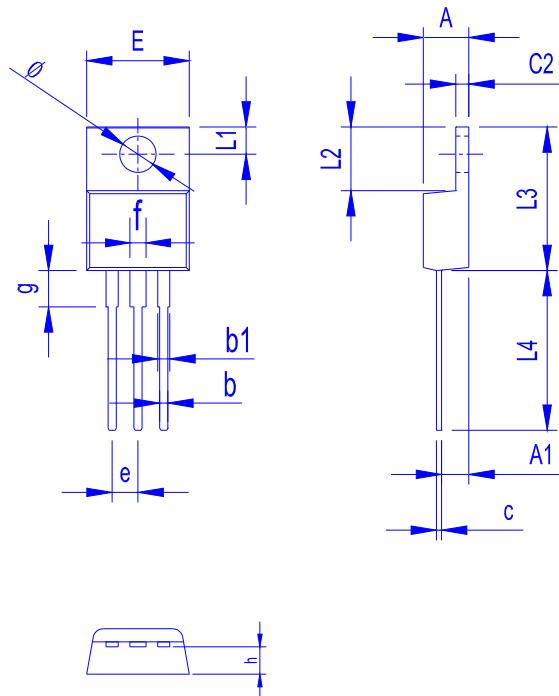


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	b	b1	c	c2	E	L1	L2	L3	L4	Ø	e	f	g	h
Min.	4.20	0.70	0.90	0.30	1.10	9.80	2.55	6.10	14.80	13.50	3.40	2.35	1.30	3.40	2.40
Max.	4.80	1.10	1.50	0.70	1.50	10.50	2.85	6.50	15.40	14.50	3.80	2.75	1.90	3.80	3.00