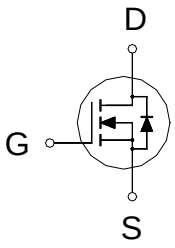
杰力科技股份有限公司
Excelliance MOS Corporation

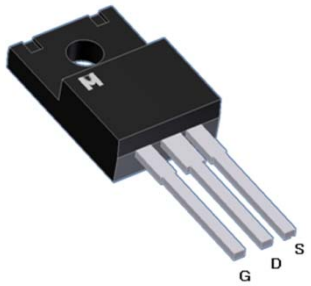
EMD03N90F

N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	900V
$R_{DSON\ (MAX.)}$	4Ω
I_D	3.5A





UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 °C	I_D	3.5	A
	T_C = 100 °C		2.2	
Pulsed Drain Current[1]		I_{DM}	14	
Avalanche Current		I_{AS}	3	
Avalanche Energy	L = 3mH, I_D=3A, R_G=25Ω	E_{AS}	13.5	mJ
Repetitive Avalanche Energy[2]	L = 0.5mH	E_{AR}	2.25	
Power Dissipation	T_C = 25 °C	P_D	32	W
	T_C = 100 °C		13	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		3.8	°C / W
Junction-to-Ambient	$R_{\theta JA}$		80	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	900			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2	3	4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 900V, V_{GS} = 0V			10	μA
		V_{DS} = 720V, V_{GS} = 0V, T_J = 125 °C			25	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 1.8A		3.2	4	Ω
Forward Transconductance[1]	g_{fs}	V_{DS} = 25V, I_D = 1.8A		3.6		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		605		pF
Output Capacitance	C_{oss}			64		
Reverse Transfer Capacitance	C_{rss}			3.3		
Total Gate Charge[1,2]	Q_g	V_{DS} = 450V, V_{GS} = 15V, I_D = 1.8A		10.4		nC
Gate-Source Charge[1,2]	Q_{gs}			2.6		
Gate-Drain Charge[1,2]	Q_{gd}			2.8		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 400V, I_D = 1A, V_{GS} = 15V, R_{GS} = 10Ω		10		nS
Rise Time[1,2]	t_r			9		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			15		
Fall Time[1,2]	t_f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				3.5	A
Pulsed Current[3]	I_{SM}				14	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		0.5		μS
Reverse Recovery Charge	Q_{rr}			2		nC

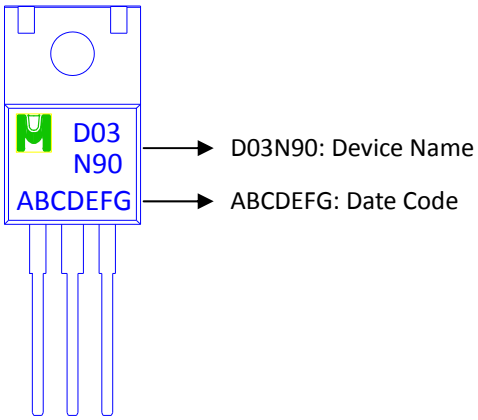
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

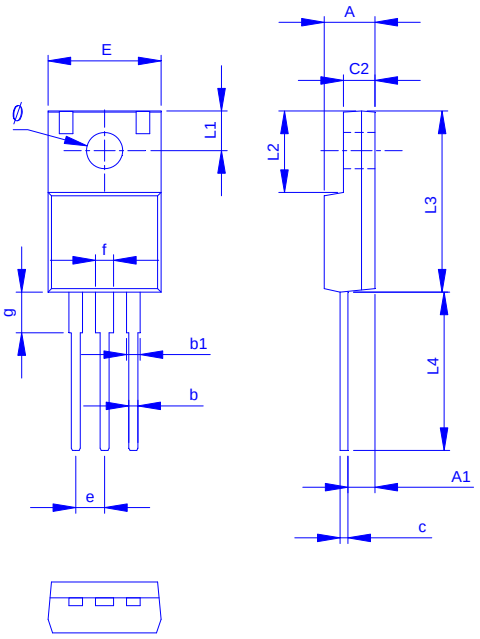
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMD03N90F for TO-220F



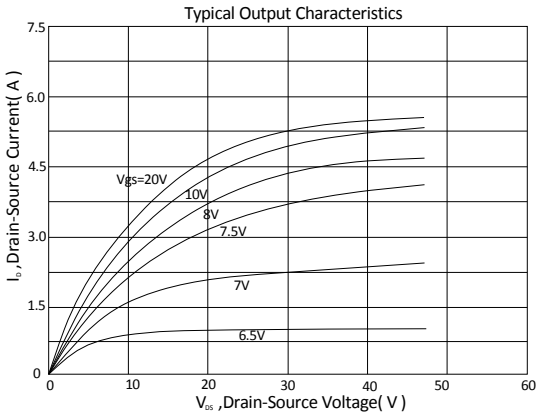
Outline Drawing

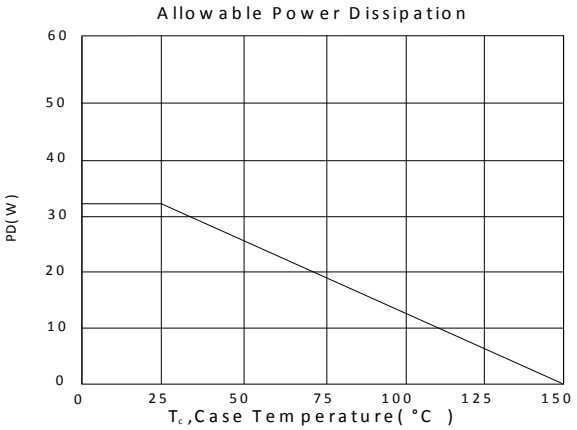


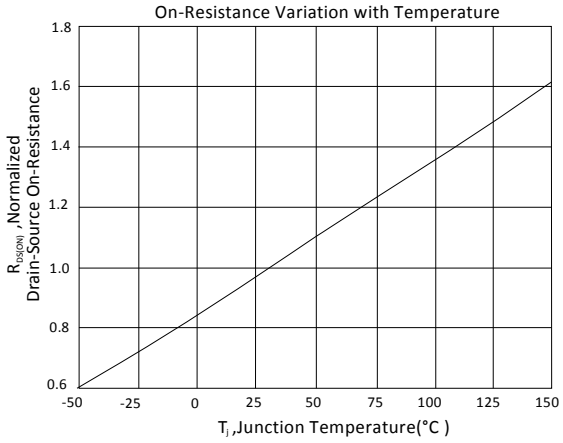
Dimension in mm

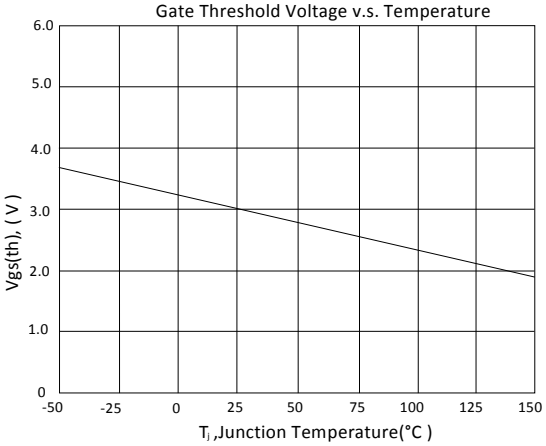
Dimension	A	A1	b	b1	c	c2	E	L1	L2	L3	L4	ø	e	f	g
Min.	4.20	1.95	0.50	0.90	0.45	2.34	9.70	2.70	6.48	14.80	12.68	3.00	2.35	1.18	3.13
Max.	4.90	2.96	1.05	1.50	0.80	3.20	10.66	3.80	7.50	16.30	14.50	3.50	2.75	1.90	4.00

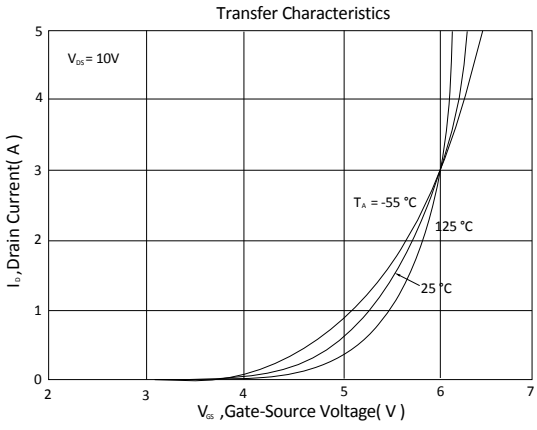
TYPICAL CHARACTERISTICS

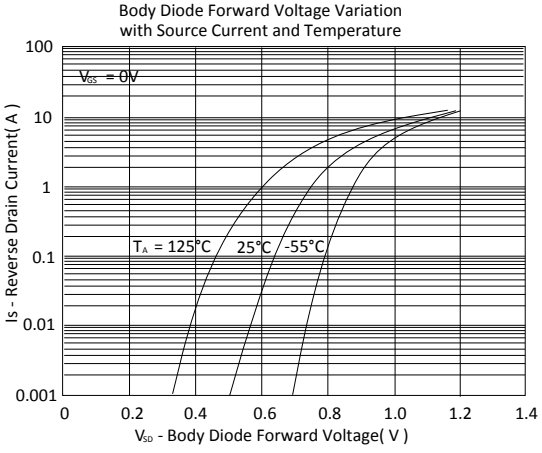


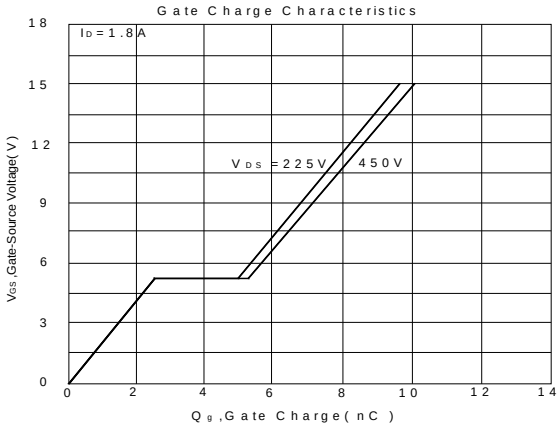


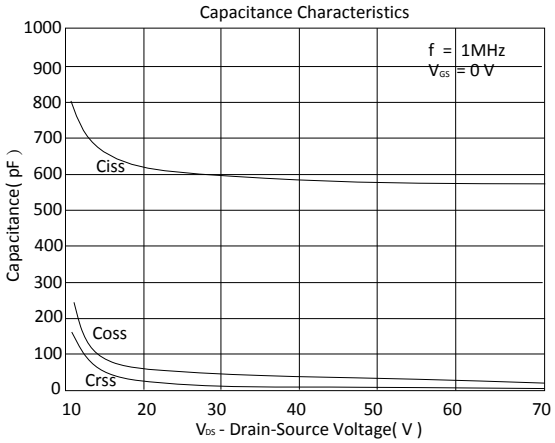


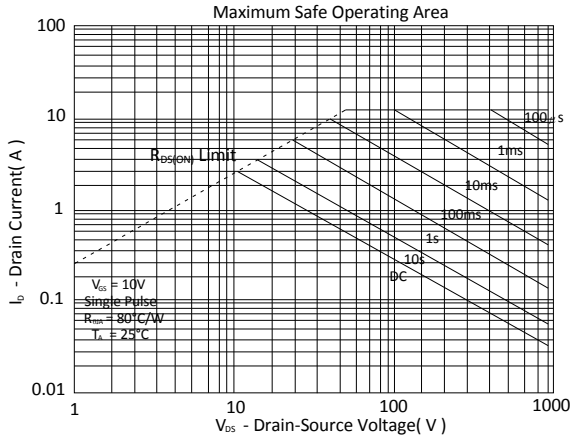


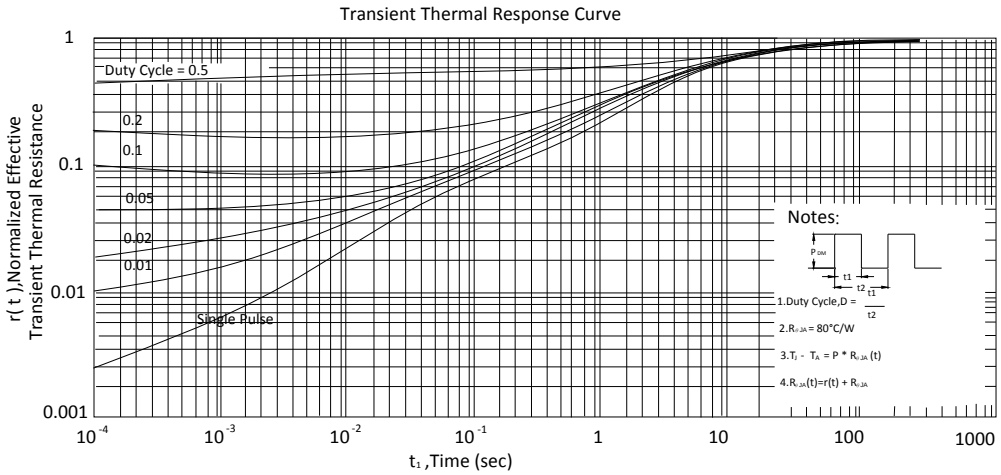





Gate Charge Characteristics
ID = 1.8A
VDS = 225V
450V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)


Capacitance Characteristics
f = 1MHz
VGS = 0 V
Ciss
Coss
Crss
Capacitance(pF)
VDS - Drain-Source Voltage(V)


Maximum Safe Operating Area
RDS(ON) Limit
100μs
1ms
10ms
100ms
1s
10s
DC
VGS = 10V
Single Pulse
RθJA = 80°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.RθJA = 80°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) + RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)