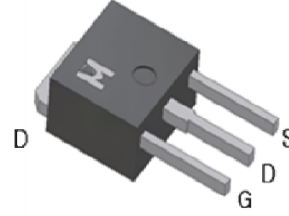


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	600V
$R_{DS(on)} (MAX.)$	2.4Ω
I_D	4A



UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	4	A
	$T_C = 100^\circ\text{C}$		3.2	
Pulsed Drain Current ¹		I_{DM}	16	
Avalanche Current		I_{AS}	4	
Avalanche Energy	$L = 3\text{mH}, I_D = 4\text{A}, R_G = 25\Omega$	E_{AS}	24	mJ
Repetitive Avalanche Energy ²	$L = 0.5\text{mH}$	E_{AR}	4	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	30	W
	$T_C = 100^\circ\text{C}$		12	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		4.2	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		110	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	600			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.5	3.5	4.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600V, V _{GS} = 0V			10	μA
		V _{DS} = 480V, V _{GS} = 0V, T _J = 125 °C			25	
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 2A		2.1	2.4	Ω
Forward Transconductance ¹	g _{fs}	V _{DS} = 25V, I _D = 2A		2		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		548		pF
Output Capacitance	C _{oss}			57		
Reverse Transfer Capacitance	C _{rss}			9		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		3.5	6.5	Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 300V, V _{GS} = 10V, I _D = 2A		11.9		nC
Gate-Source Charge ^{1,2}	Q _{gs}			3.5		
Gate-Drain Charge ^{1,2}	Q _{gd}			5.4		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 300V, I _D = 1A, V _{GS} = 10V, R _G = 20Ω		15		nS
Rise Time ^{1,2}	t _r			25		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			20		
Fall Time ^{1,2}	t _f			30		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				4	A
Pulsed Current ³	I _{SM}				16	
Forward Voltage ¹	V _{SD}	I _F = 2A, V _{GS} = 0V			1.4	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		0.3		μS
Reverse Recovery Charge	Q _{rr}				1.0	

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

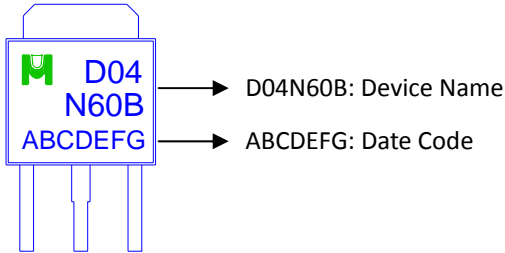
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

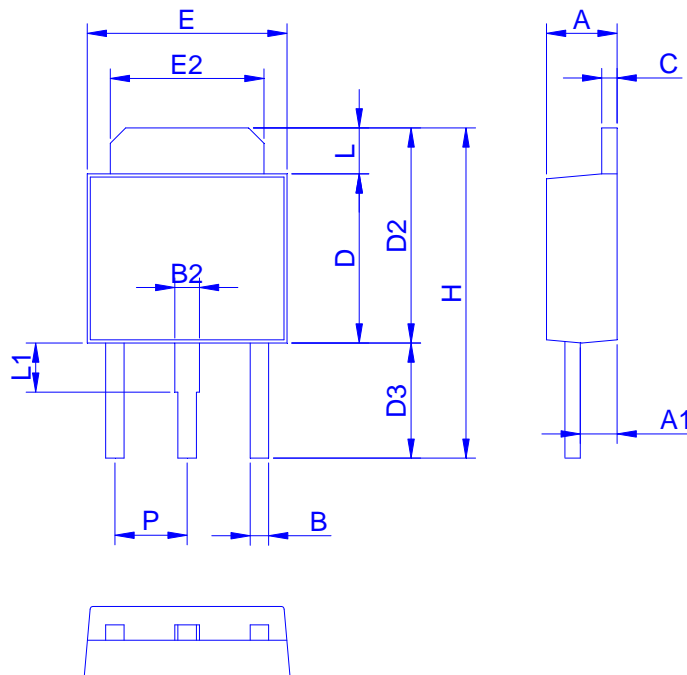


Ordering & Marking Information:

Device Name: EMD04N60CSB for IPAK (TO-251)



Outline Drawing

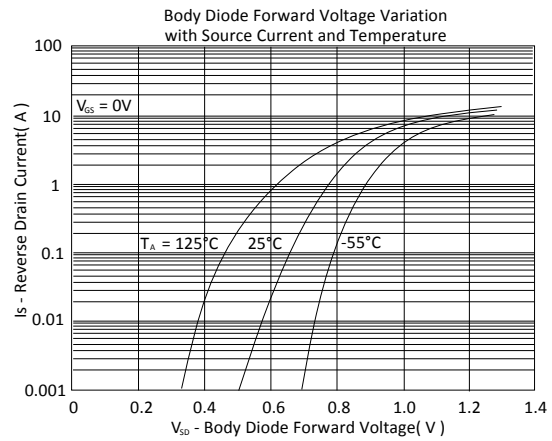
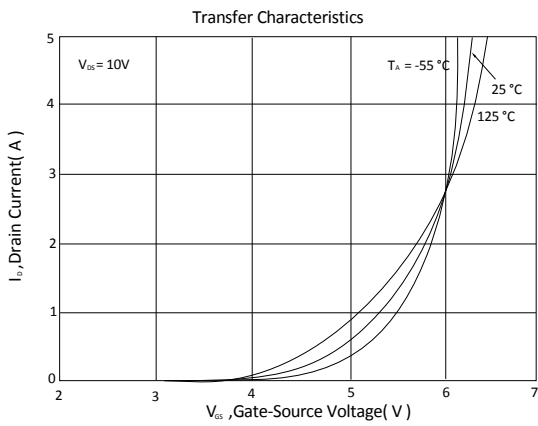
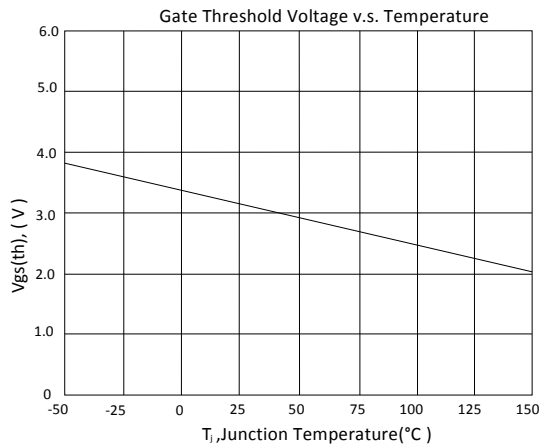
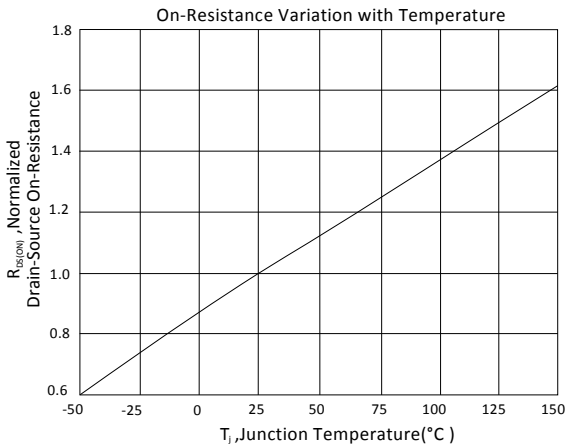
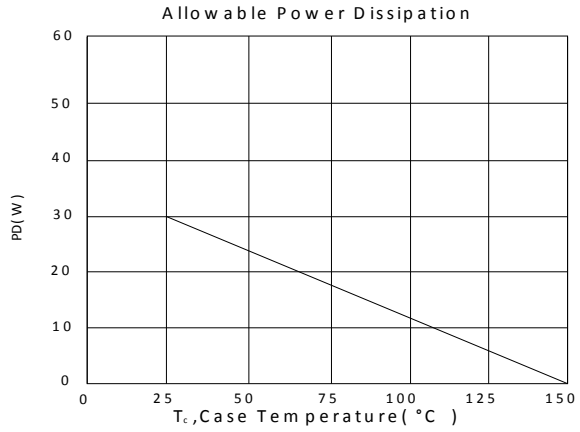
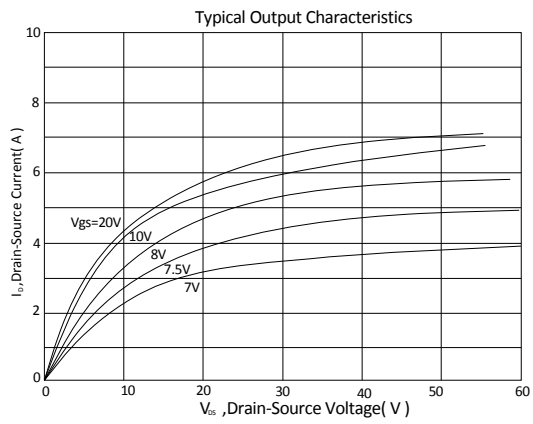


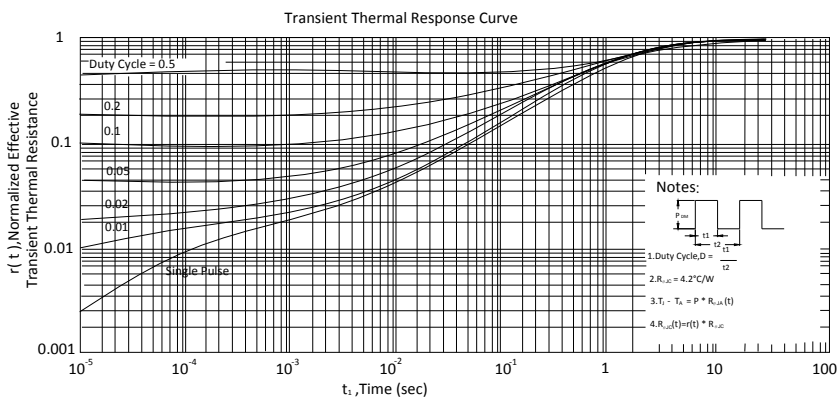
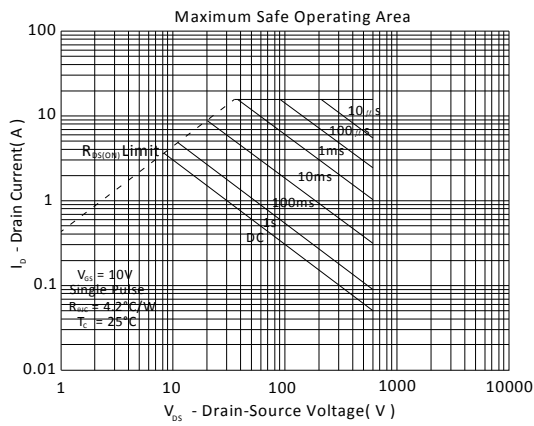
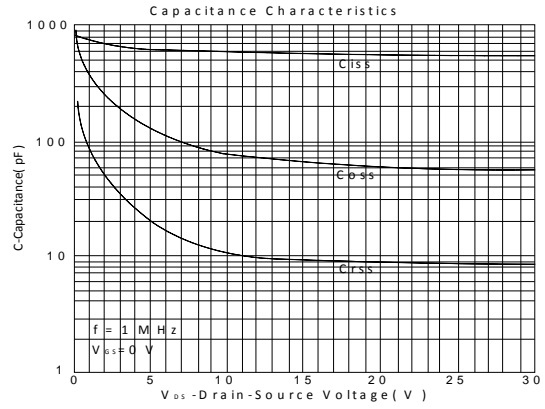
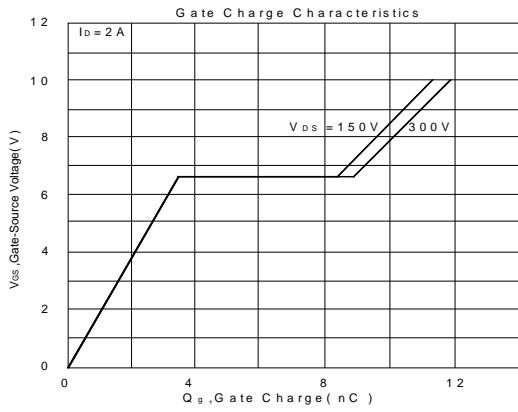
Dimension in mm

Dimension	A	A1	B	B2	C	D	D2	D3	E	E2	H	L	L1	P
Min.	2.10	0.90	0.40	0.60	0.40	5.30	6.70	3.40	6.30	4.80	10.2	0.89	0.90	2.10
Max.	2.50	1.50	0.90	1.15	0.60	6.25	7.30	4.30	6.80	5.50	11.5	1.40	1.80	2.50



TYPICAL CHARACTERISTICS







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Excelliance MOS Corporation

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