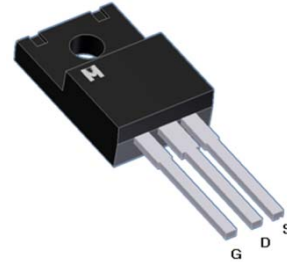


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	600V
$R_{DS(on)}$ (MAX.)	0.75 $\Omega$
$I_D$	12A



UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 30$	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	12	A
	$T_C = 100\text{ }^\circ\text{C}$		6.5	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	48	
Avalanche Current		$I_{AS}$	12	
Avalanche Energy	$L = 3\text{mH}, I_D = 12\text{A}, R_G = 25\text{ }\Omega$	$E_{AS}$	216	mJ
Repetitive Avalanche Energy <sup>2</sup>	$L = 0.5\text{mH}$	$E_{AR}$	36	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	48	W
	$T_C = 100\text{ }^\circ\text{C}$		19	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.6	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		60	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

ELECTRICAL CHARACTERISTICS ( $T_c = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	600			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 30V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600V, V_{GS} = 0V$			10	$\mu A$
		$V_{DS} = 480V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 5A$		0.65	0.75	$\Omega$
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 25V, I_D = 5A$		8		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		1440		pF
Output Capacitance	$C_{oss}$			136		
Reverse Transfer Capacitance	$C_{rss}$			7.5		
Total Gate Charge <sup>1,2</sup>	$Q_g$	$V_{DS} = 300V, V_{GS} = 15V,$ $I_D = 5A$		21		nC
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			4.6		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			6.4		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	$V_{DS} = 300V,$ $I_D = 5A, V_{GS} = 15V, R_{GS} = 10\Omega$		12		nS
Rise Time <sup>1,2</sup>	$t_r$			10		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			26		
Fall Time <sup>1,2</sup>	$t_f$			10		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_c = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				12	A
Pulsed Current <sup>3</sup>	$I_{SM}$				48	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$			1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 5A, di_F/dt = 100A / \mu S$		0.7		$\mu S$
Reverse Recovery Charge	$Q_{rr}$				5.5	

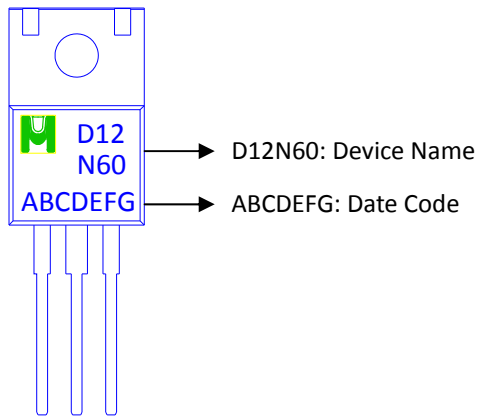
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\text{ }\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

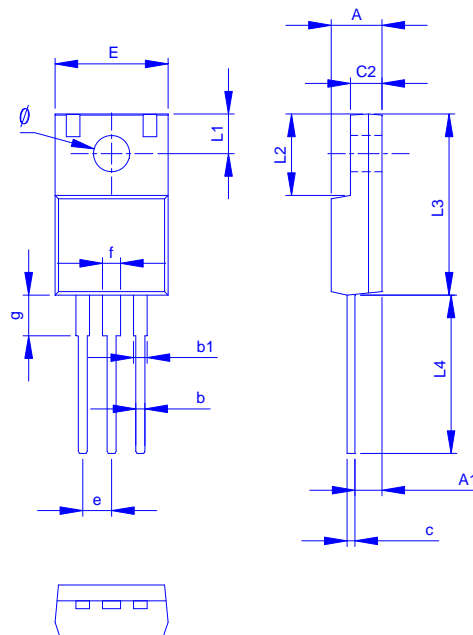
<sup>3</sup>Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMD12N60F for TO-220F



Outline Drawing



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L1	L2	L3	L4	φ	e	f	g
Min.	4.20	1.95	0.50	0.90	0.45	2.34	9.70	2.70	6.48	14.80	12.68	3.00	2.35	1.18	3.13
Max.	4.90	2.96	1.05	1.50	0.80	3.20	10.66	3.80	7.50	16.30	14.50	3.50	2.75	1.90	4.00



TYPICAL CHARACTERISTICS

