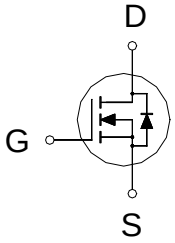
杰力科技股份有限公司
Excelliance MOS Corporation

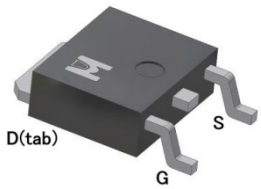
EMD50N15A

N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	150V
$R_{DSON\ (MAX.)}$	50mΩ
I_D	36A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Drain-Source Voltage		V_{DSS}	150	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 °C	I_D	36	A
	T_C = 100 °C		22	
Pulsed Drain Current[1]		I_{DM}	120	
Avalanche Current		I_{AS}	18	
Avalanche Energy	L = 0.2mH, ID=18A, RG=25Ω	E_{AS}	32.4	mJ
Repetitive Avalanche Energy[2]	L = 0.1mH	E_{AR}	16.2	
Power Dissipation	T_C = 25 °C	P_D	104	W
	T_C = 100 °C		41	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.2	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		75	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]75°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.5	2.5	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120V, V_{GS} = 0V			1	μA
		V_{DS} = 100V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	48			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		40	50	mΩ
		V_{GS} = 7V, I_D = 15A		48	60	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A		40		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		4905		pF
Output Capacitance	C_{oss}			238		
Reverse Transfer Capacitance	C_{rss}			200		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		2.0		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 80V, V_{GS} = 10V, I_D = 20A		67.5		nC
Gate-Source Charge[1,2]	Q_{gs}			12.7		
Gate-Drain Charge[1,2]	Q_{gd}			16.6		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 75V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		20		nS
Rise Time[1,2]	t_r			18		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			40		
Fall Time[1,2]	t_f			18		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				36	A
Pulsed Current[3]	I_{SM}				120	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 25A, dI_F/dt = 100A / μS		120		nS
Reverse Recovery Charge	Q_{rr}			380		nC

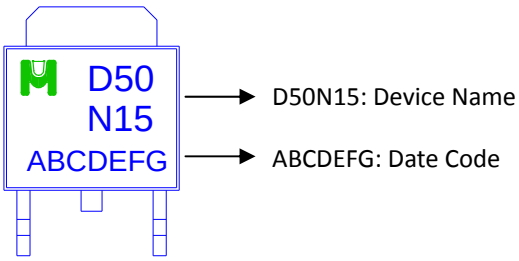
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

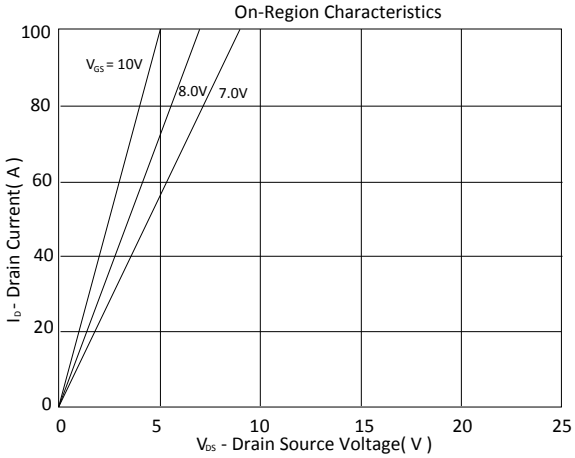
Ordering & Marking Information:

Device Name: EMD50N15A for DPAK (TO-252)

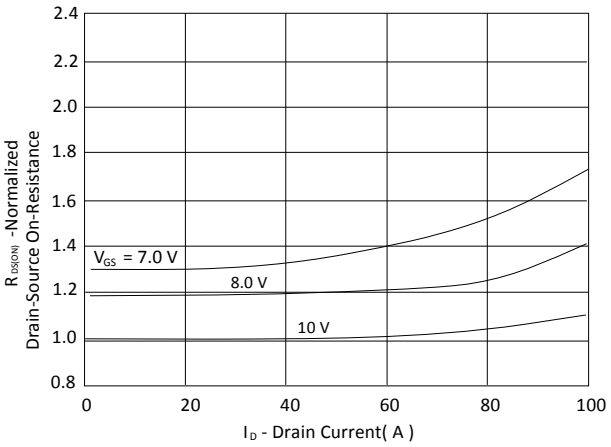


TYPICAL CHARACTERISTICS

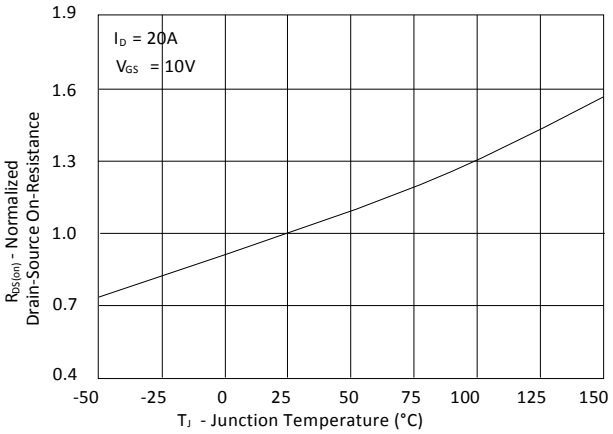
On-Region Characteristics



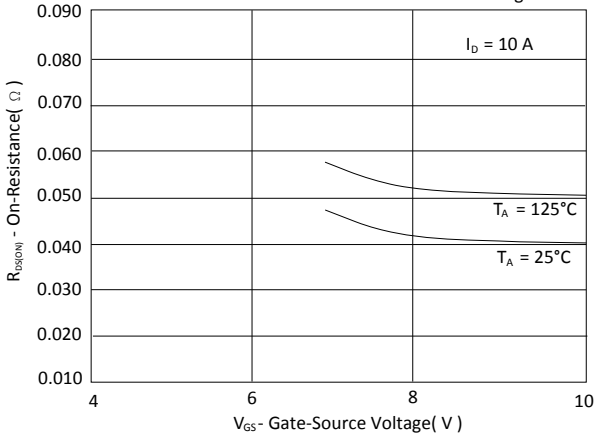
On-Resistance Variation with Drain Current and Gate Voltage



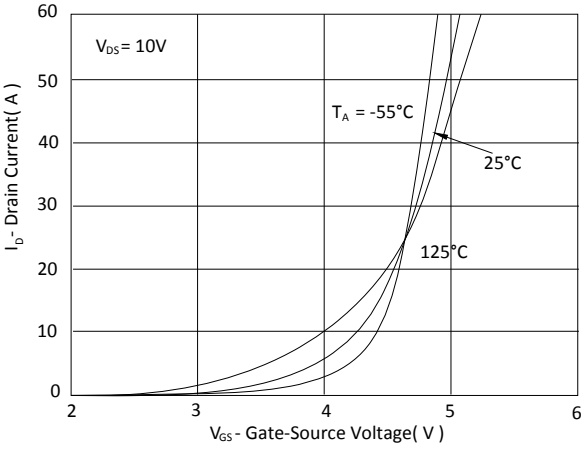
On-Resistance Variation with Temperature



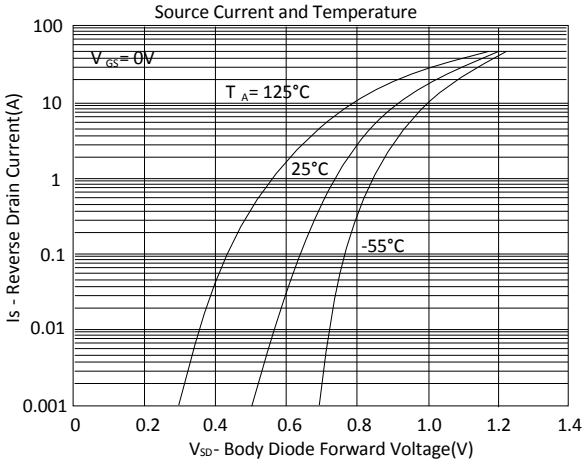
On-Resistance Variation with Gate-Source Voltage

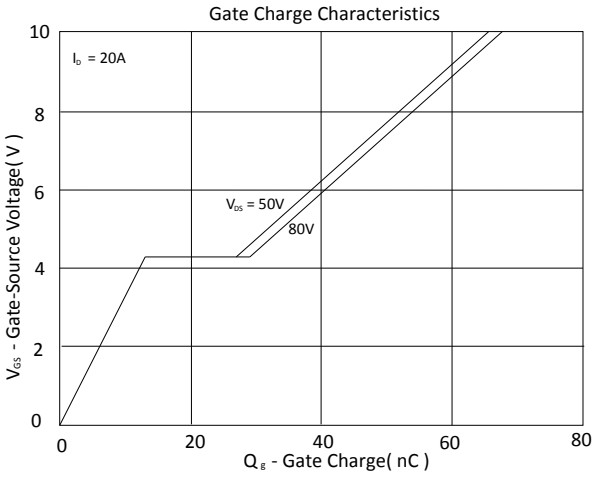


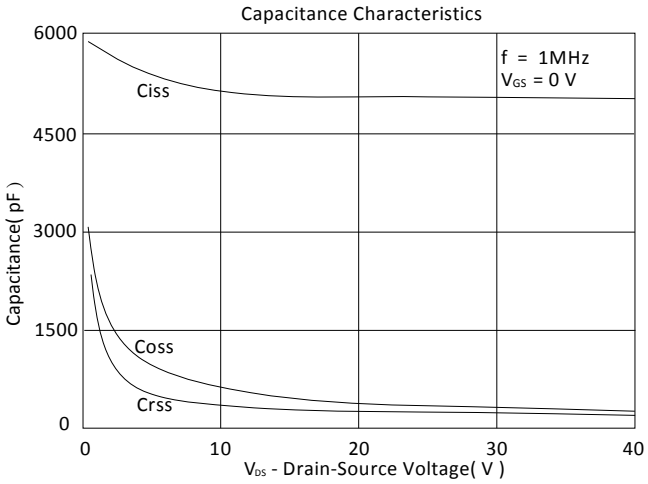
Transfer Characteristics

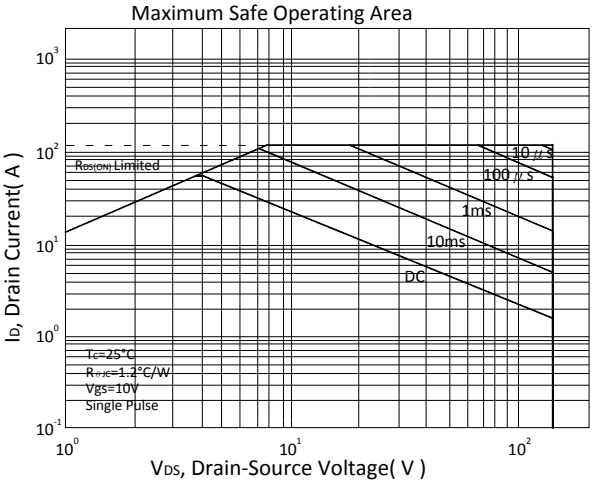


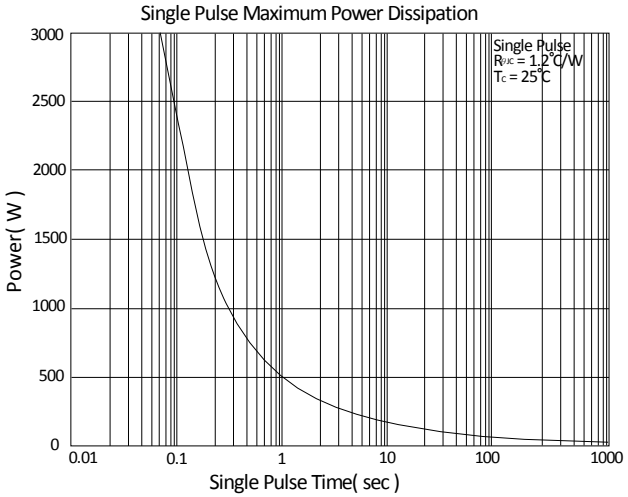
Body Diode Forward Voltage Variation with Source Current and Temperature

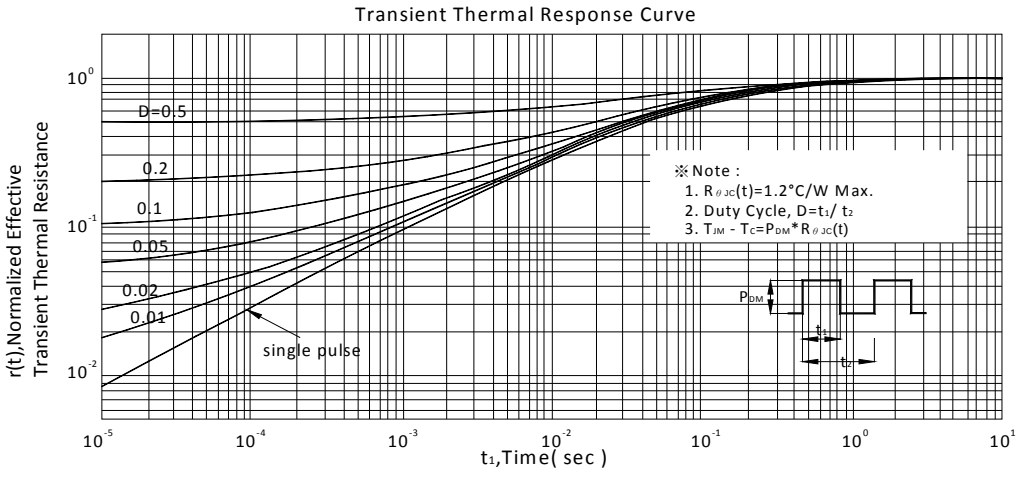



Gate Charge Characteristics
I_D = 20A
V_{DS} = 50V
80V
V_{GS} - Gate-Source Voltage(V)
Q_g - Gate Charge(nC)

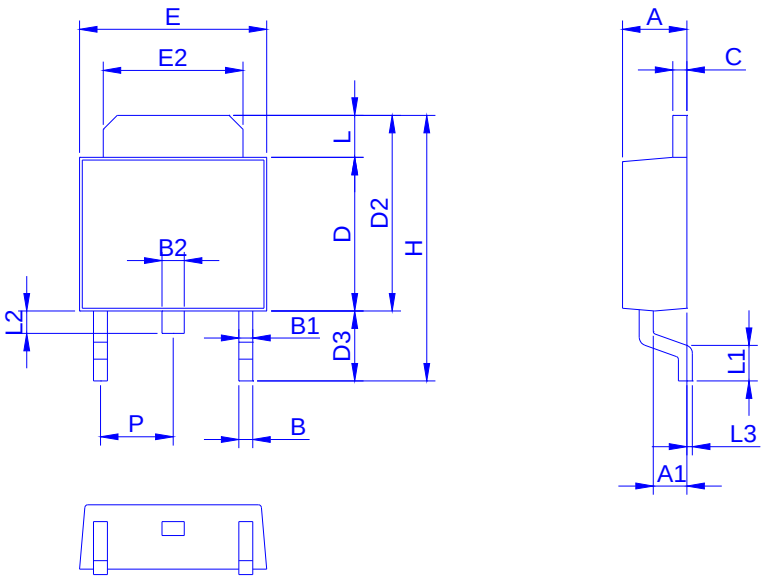

Capacitance Characteristics
f = 1MHz
V_{GS} = 0 V
Ciss
Coss
Crss
Capacitance(pF)
V_{DS} - Drain-Source Voltage(V)


Maximum Safe Operating Area
$R_{DS(ON)}$ Limited
10μs
100μs
1ms
10ms
DC
T_C=25°C
$R_{θJC}$=1.2°C/W
Vgs=10V
Single Pulse
I_D, Drain Current(A)
V_{DS}, Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
$R_{θJC}$ = 1.2°C/W
T_C = 25°C
Power(W)
Single Pulse Time(sec)


Transient Thermal Response Curve
D=0.5
0.2
0.1
0.05
0.02
0.01
single pulse
※Note :
1. $R_{θJC}(t)$=1.2°C/W Max.
2. Duty Cycle, D=t_1/ t_2
3. T_{JM} - T_C=P_{DM}*$R_{θJC}(t)$
P_{DM}
t_1
t_2
r(t),Normalized Effective Transient Thermal Resistance
t_1,Time(sec)

Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint