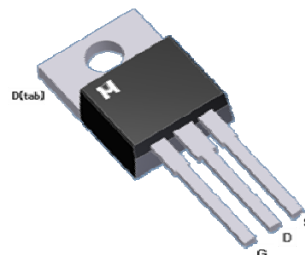
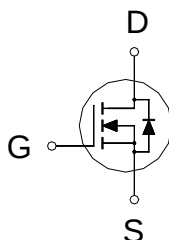


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	150V
$R_{DS(on)} (MAX.)$	60m Ω
I_D	43A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Drain-Source Voltage		V_{DSS}	150	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	43	A
	$T_C = 100\text{ }^{\circ}\text{C}$		26	
Pulsed Drain Current ¹		I_{DM}	120	
Avalanche Current		I_{AS}	18	
Avalanche Energy	$L = 0.2\text{mH}$, $I_{AS}=18\text{A}$, $R_G=25\text{ }\Omega$	E_{AS}	32.4	mJ
Repetitive Avalanche Energy ²	$L = 0.1\text{mH}$	E_{AR}	16.2	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	83	W
	$T_C = 100\text{ }^{\circ}\text{C}$		33	
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.5	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	150			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	3.0	4.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 30V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 120V, V_{GS} = 0V$			1	μA
		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	43			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 20A$		50	60	mΩ
		$V_{GS} = 7V, I_D = 20A$		58	70	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 20A$		25		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$		2903		pF
Output Capacitance	C_{oss}			172		
Reverse Transfer Capacitance	C_{rss}			59		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		2.3		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 80V, V_{GS} = 10V,$ $I_D = 20A$		38.2		nC
Gate-Source Charge ^{1,2}	Q_{gs}			9.8		
Gate-Drain Charge ^{1,2}	Q_{gd}			14.5		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 75V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		15		nS
Rise Time ^{1,2}	t_r			40		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			45		
Fall Time ^{1,2}	t_f			38		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I_S				43	A
Pulsed Current ³	I_{SM}				120	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = 20A, dI_F/dt = 100A / \mu S$		100		nS
Reverse Recovery Charge	Q_{rr}			360		nC

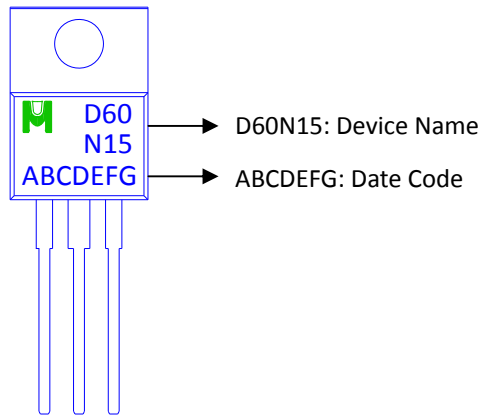
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

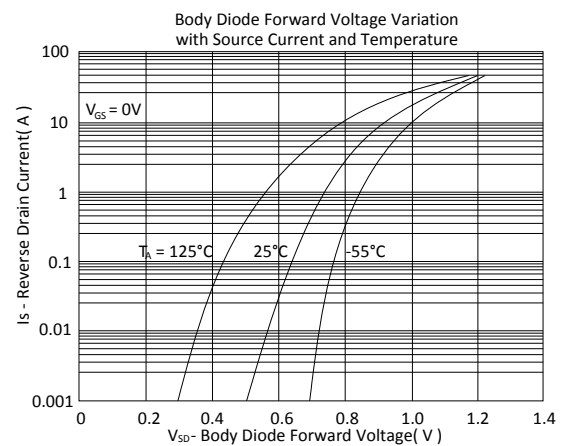
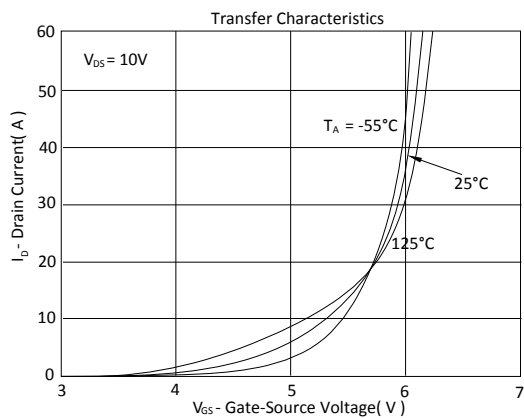
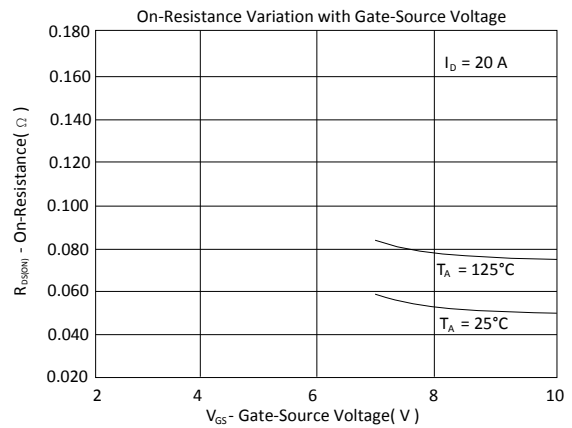
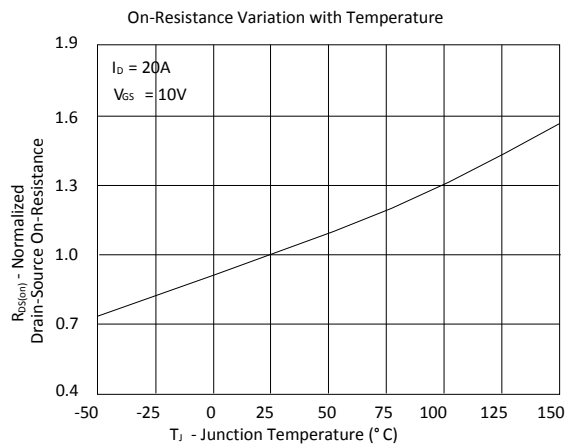
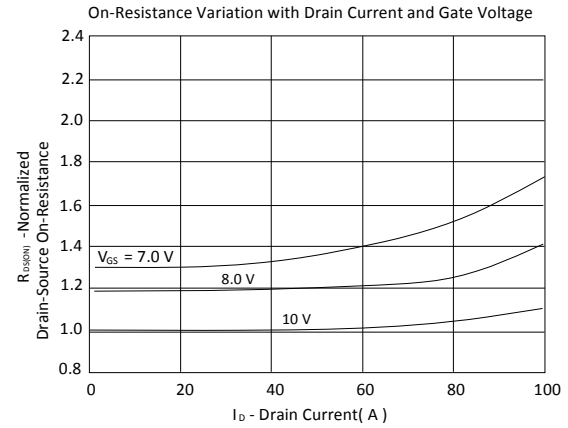
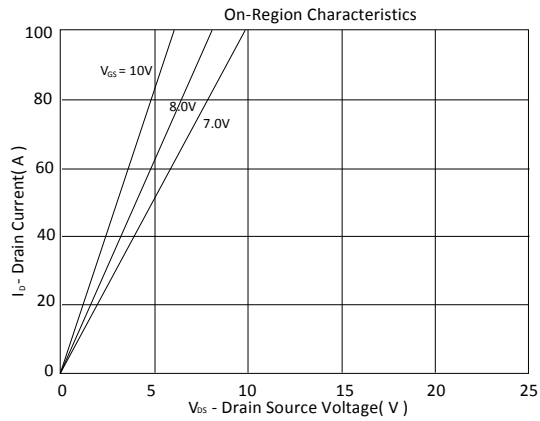
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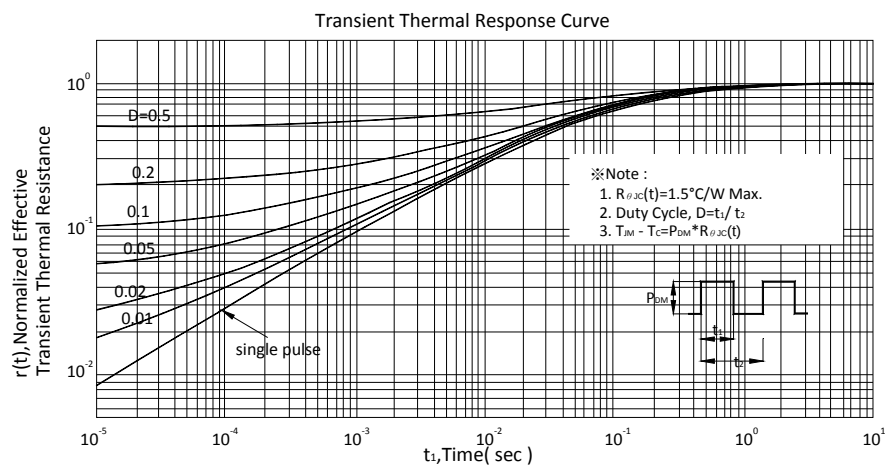
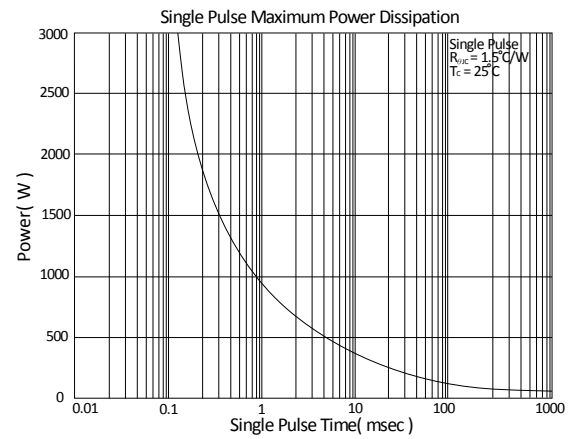
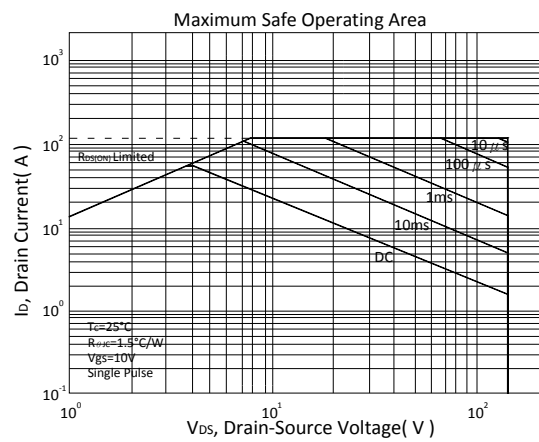
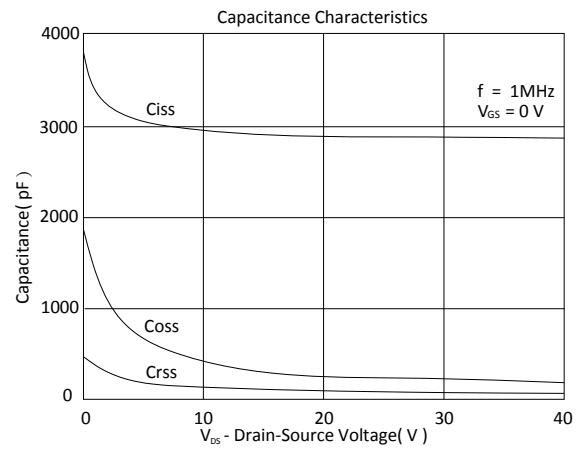
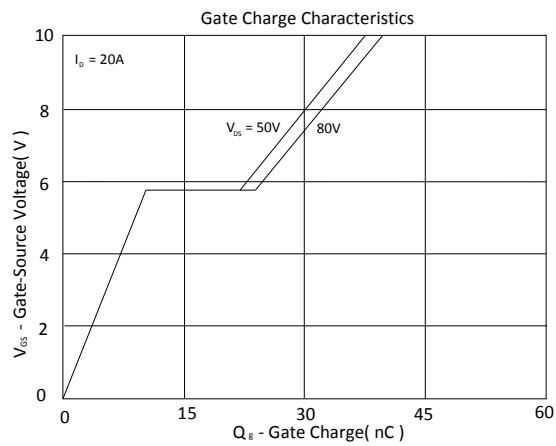
Device Name: EMD60N15E for TO-220



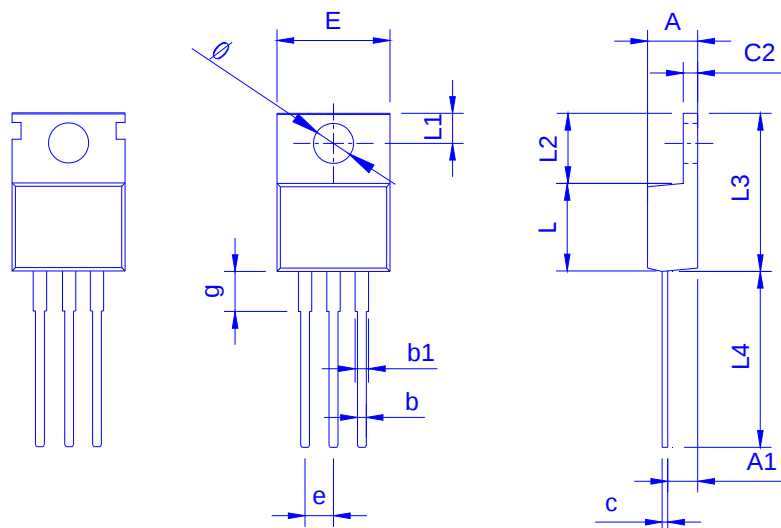


TYPICAL CHARACTERISTICS





Outline Drawing



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L	L1	L2	L3	L4	ø	e	g
Min.	4.07	2.04	0.60	1.15	0.31	1.11	9.90	8.30	2.50	6.00	14.30	12.70	3.40	2.04	2.85
Typ.	4.44	2.40	0.80	1.27	-	1.27	10.16	-	2.74	6.30	15.00	13.40	3.84	2.54	3.71
Max.	4.82	3.00	1.00	1.75	0.65	1.41	11.50	9.75	3.25	6.80	16.90	14.50	4.00	3.04	4.10