



杰力科技股份有限公司
Excelliance MOS Corporation

EMF20B02V

P-Channel Logic Level Enhancement Mode Field Effect Transistor

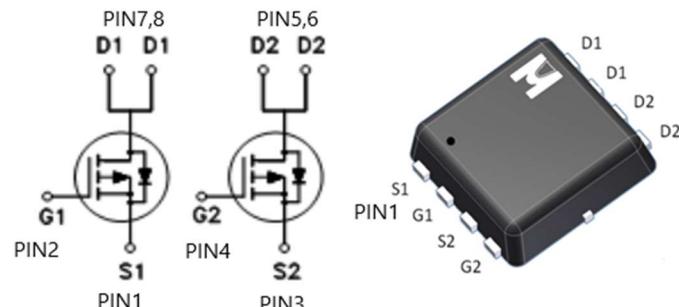
Product Summary:

BV_{DSS}	-20V
$R_{DS(on)}$ (MAX.)	20m Ω
I_D	-8.5A

P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±12	V
Continuous Drain Current	T _A = 25 °C	I _D	-8.5	A
	T _A = 70 °C		-6	
Pulsed Drain Current ¹		I _{DM}	-34	
Power Dissipation	T _A = 25 °C	P _D	2	W
	T _A = 70 °C		1.28	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-20			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.4	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 12\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$			-1	μA
		$V_{DS} = -12\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$			-10	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = -5\text{V}, V_{GS} = -4.5\text{V}$	-8.5			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = -4.5\text{V}, I_D = -8.5\text{A}$		15	20	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -4.5\text{A}$		19	25	
		$V_{GS} = -1.8\text{V}, I_D = -2.5\text{A}$		26	40	
Forward Transconductance ¹	g_f	$V_{DS} = -5\text{V}, I_D = -8.5\text{A}$		22		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = -10\text{V}, f = 1\text{MHz}$		3050		pF
Output Capacitance	C_{oss}			460		
Reverse Transfer Capacitance	C_{rss}			410		
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=-4.5\text{V})$	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V}, I_D = -8.5\text{A}$		27		nC
	$Q_g(V_{GS}=-2.5\text{V})$			16.5		
Gate-Source Charge ^{1,2}	Q_{gs}			2.2		
Gate-Drain Charge ^{1,2}	Q_{gd}			6.8		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$			20		nS
Rise Time ^{1,2}	t_r			50		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			90		
Fall Time ^{1,2}	t_f			60		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_s				-2.3	A
Pulsed Current ³	I_{SM}				-9.2	
Forward Voltage ¹	V_{SD}	$I_F = I_s, V_{GS} = 0\text{V}$			-1.2	V

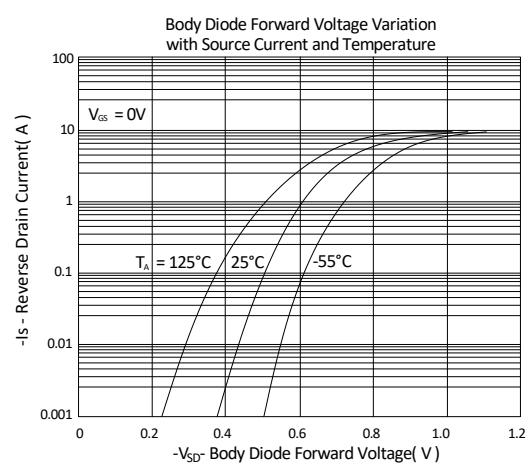
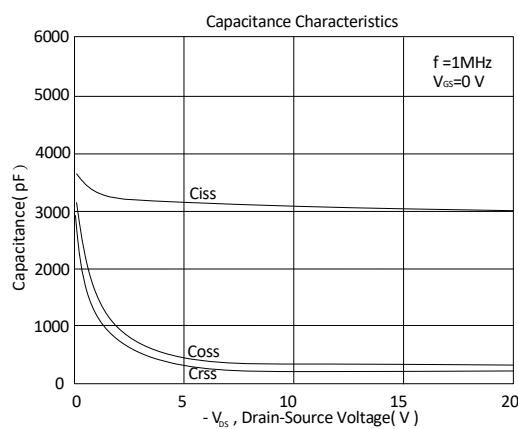
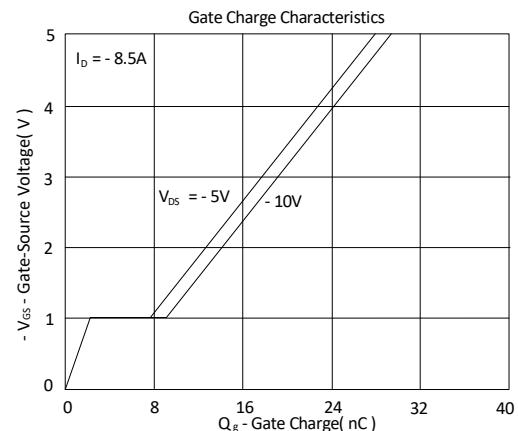
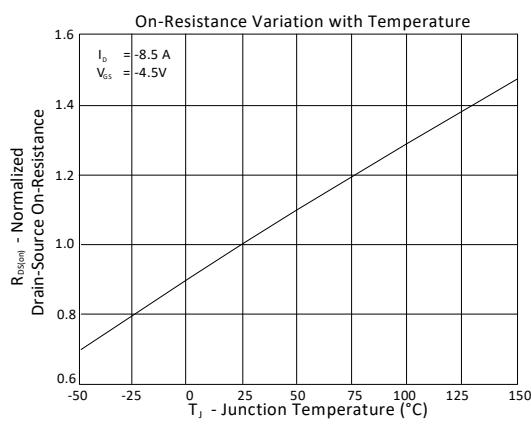
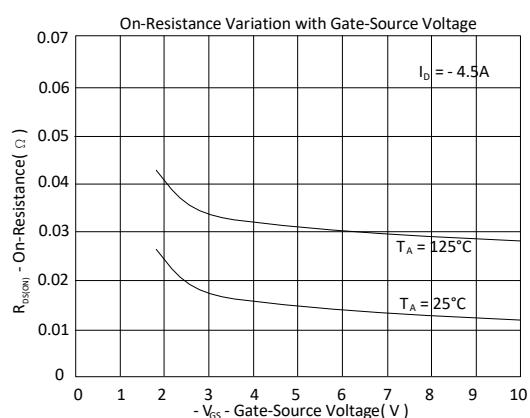
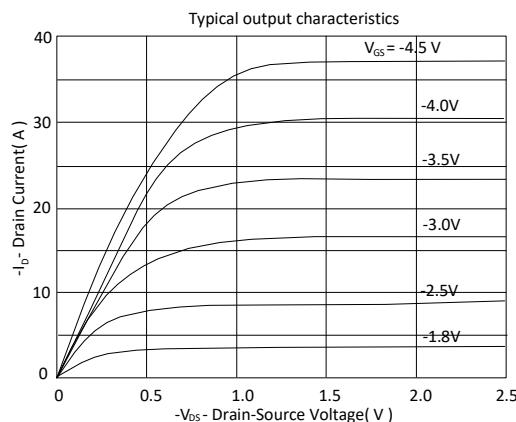
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

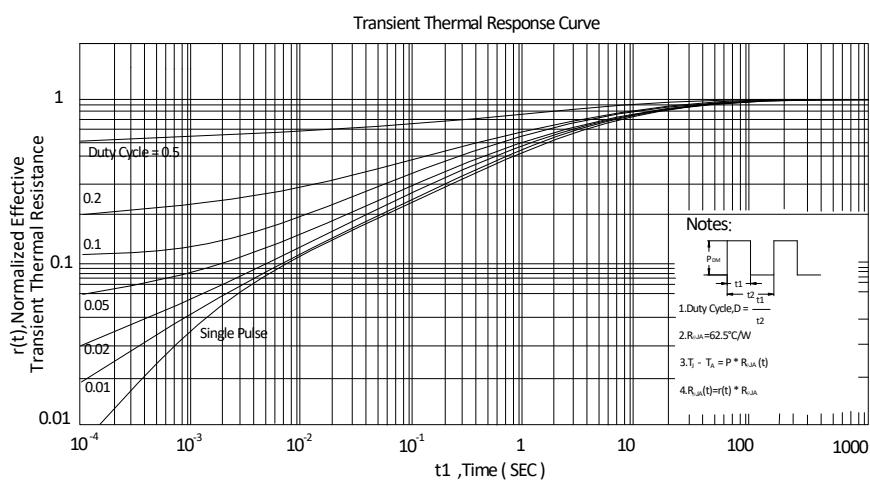
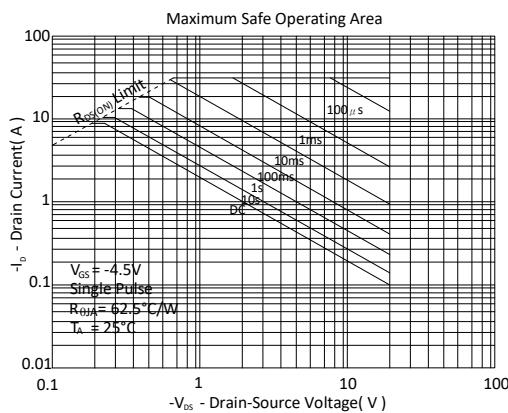
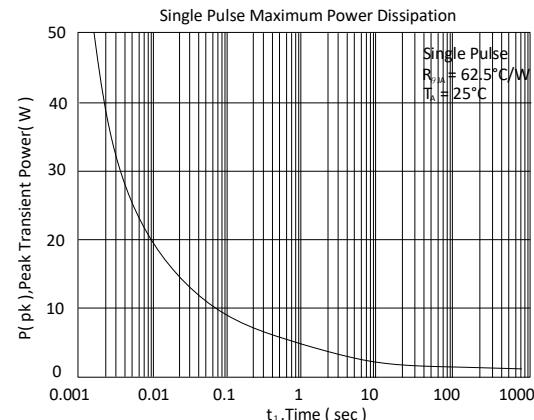
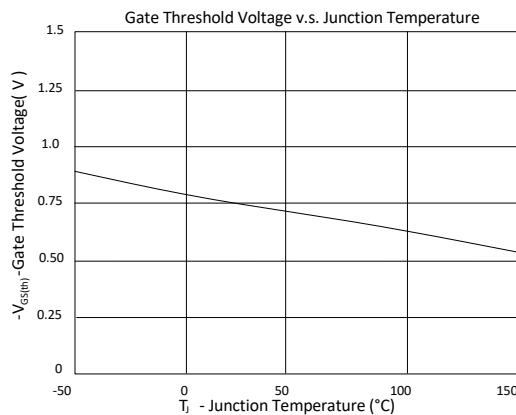
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

EMC will review datasheet by quarter, and update new version.

TYPICAL CHARACTERISTICS





Ordering & Marking Information:

Device Name: EMF20B02V for EDFN3X3



→ EMF20B02V : Device Name

→ ABCDEFG: Date Code

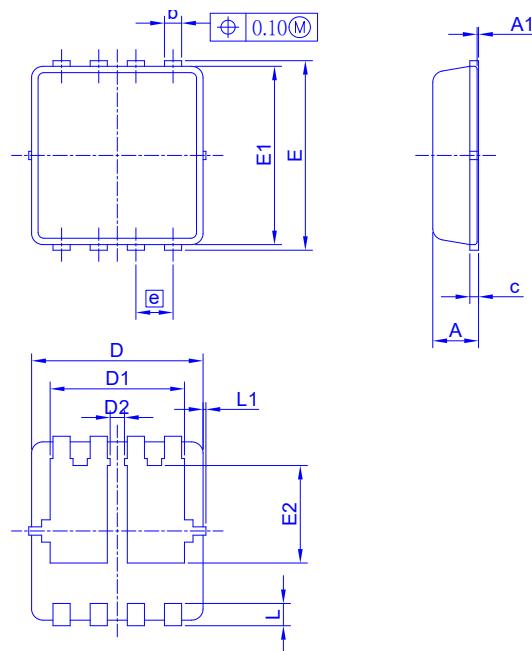
→ A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

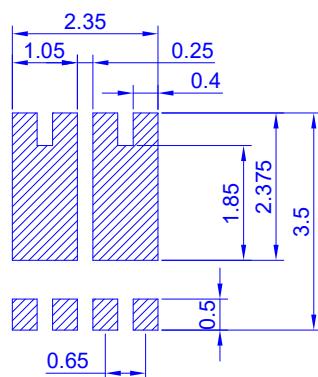
Outline Drawing



Dimension in mm

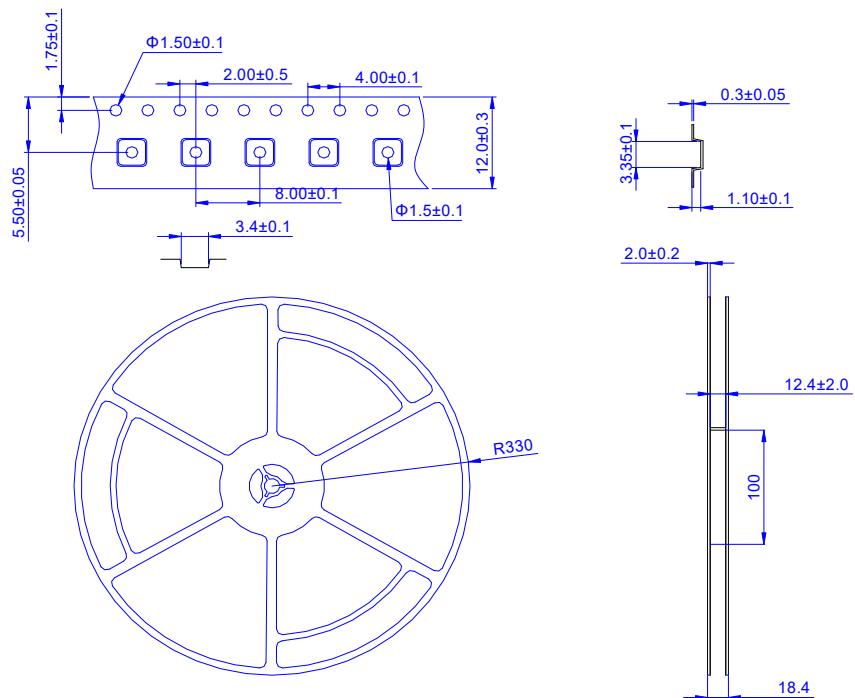
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	L	L1	θ1
Min.	0.65	0	0.20	0.10	2.90	2.15	0.28	3.10	2.90	1.53	0.55	0.30	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.47	0.38	3.20	3.00	1.81	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.75	-	3.50	3.30	1.98	0.75	0.50	0.150	14°

Recommended minimum pads





Tape&Reel Information: 5000pcs/Reel



產品別	EDFN3X3
Reel 尺寸	13"
編帶方式	FEED DIRECTION
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	1 : 1
內盒滿箱數	5K
內/外箱比	10 : 1
外箱滿箱數	50K