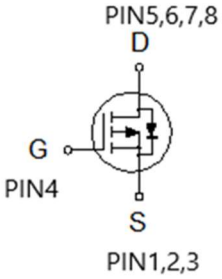
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-12V
$R_{DSON\ (MAX.)}$	20mΩ
I_D	-18A



P-Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_C = 25 °C	I_D	-18	A
	T_A = 25 °C		-9	
	T_C = 100 °C		-12	
Pulsed Drain Current[1]		I_{DM}	-72	
Power Dissipation	T_C = 25 °C	P_D	21	W
	T_C = 100 °C		8.3	
Power Dissipation	T_A = 25 °C	P_D	2.5	W
	T_A = 70 °C		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]50°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-12			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.4	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -12V, V_{GS} = 0V			-1	μA
		V_{DS} = -10V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -4.5V	-18			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -9A		15	20	mΩ
		V_{GS} = -2.5V, I_D = -5A		19	25	
		V_{GS} = -1.8V, I_D = -3A		26	40	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -9A		22		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -6V, f = 1MHz		3100		pF
Output Capacitance	C_{oss}			460		
Reverse Transfer Capacitance	C_{rss}			413		
Total Gate Charge[1,2]	Q_g(V_{GS}=-4.5V)	V_{DS} = -6V, V_{GS} = -4.5V, I_D = -9A		25.5		nC
	Q_g(V_{GS}=-2.5V)			15		
Gate-Source Charge[1,2]	Q_{gs}			2.2		
Gate-Drain Charge[1,2]	Q_{gd}			5.7		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -6V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω		20		nS
Rise Time[1,2]	t_r			50		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			95		
Fall Time[1,2]	t_f			60		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-18	A
Pulsed Current[3]	I_{SM}				-72	
Forward Voltage[1]	V_{SD}	I_F = -9A, V_{GS} = 0V			-1.2	V

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

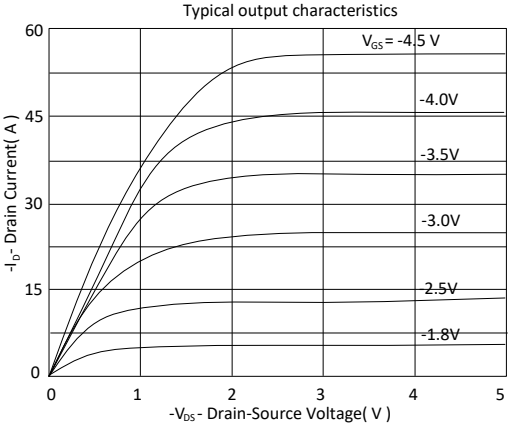
[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

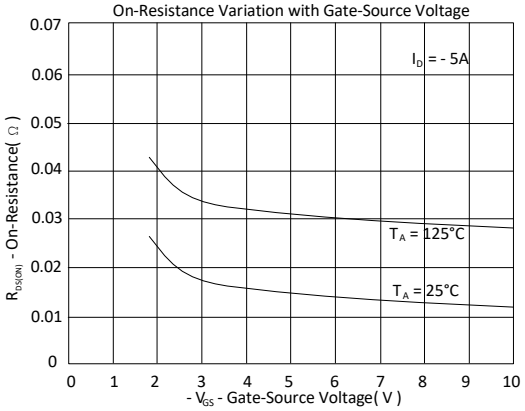
EMC will review datasheet by quarter, and update new version.

TYPICAL CHARACTERISTICS

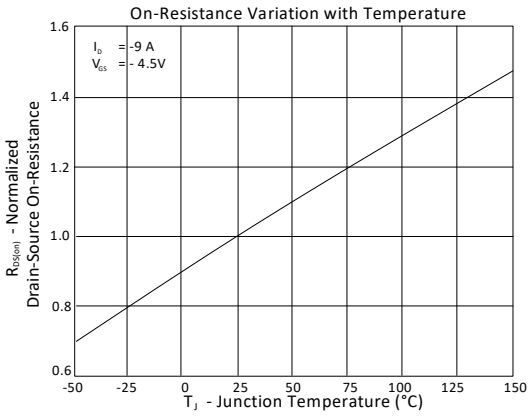
Typical output characteristics



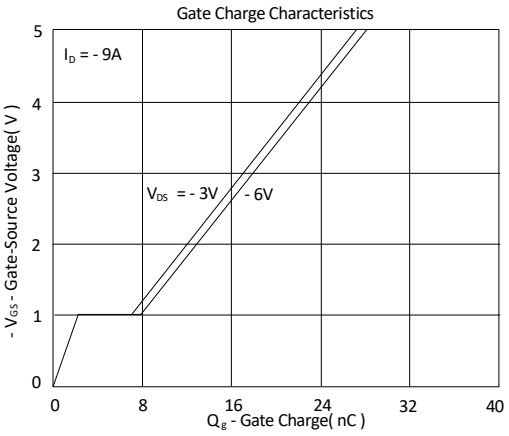
On-Resistance Variation with Gate-Source Voltage



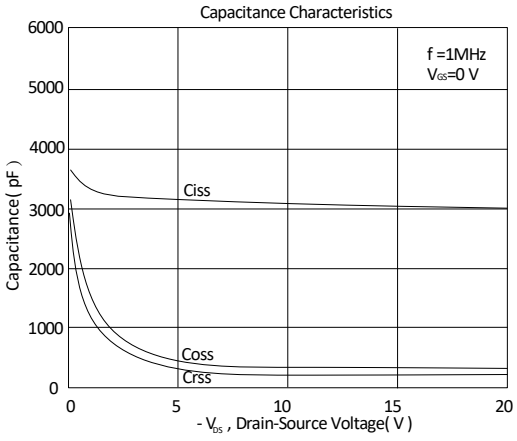
On-Resistance Variation with Temperature



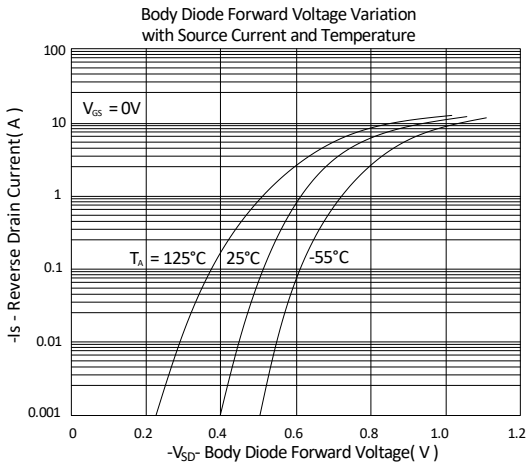
Gate Charge Characteristics



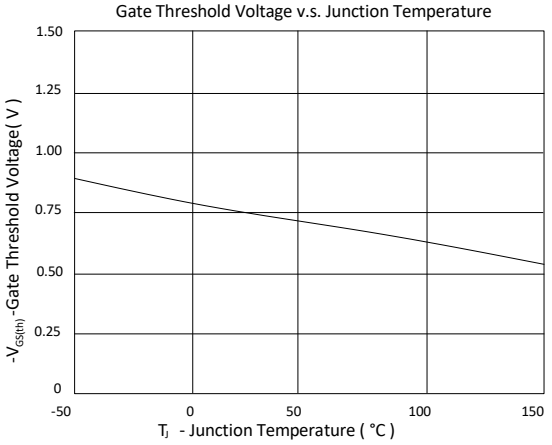
Capacitance Characteristics



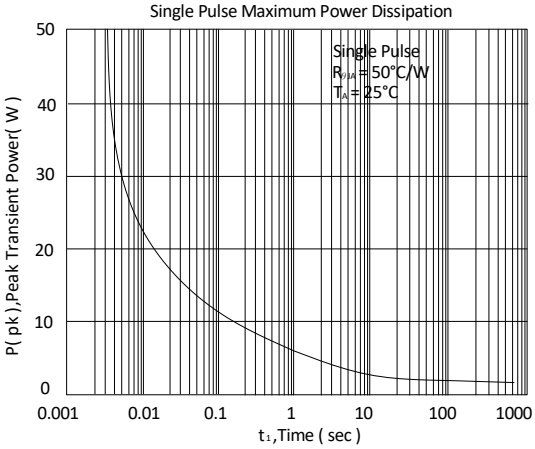
Body Diode Forward Voltage Variation
with Source Current and Temperature



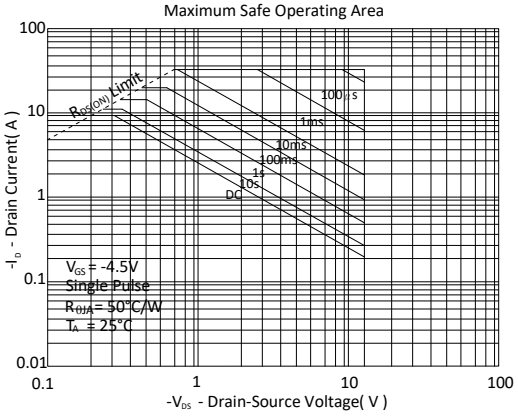
Gate Threshold Voltage v.s. Junction Temperature



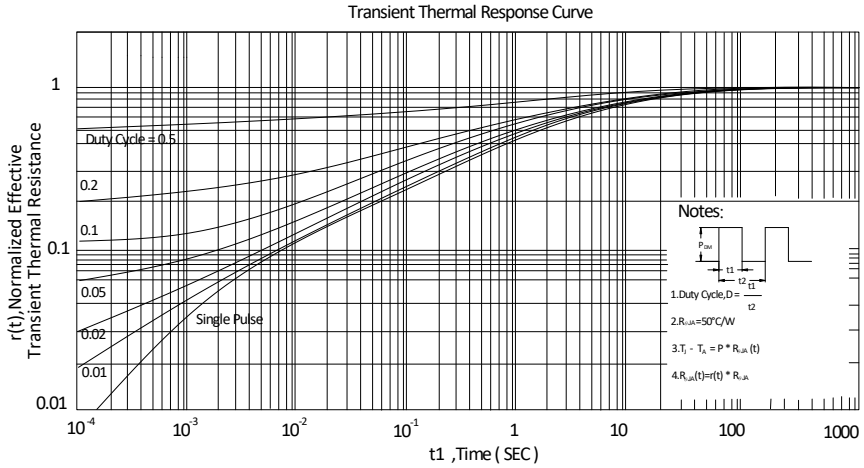
Single Pulse Maximum Power Dissipation



Maximum Safe Operating Area

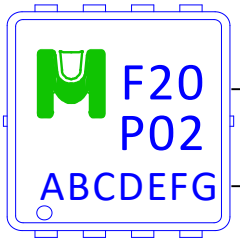


Transient Thermal Response Curve



Ordering & Marking Information:

Device Name: EMF20P02V for EDFN3X3



F20P02: Device Name

ABCDEFG: Date Code

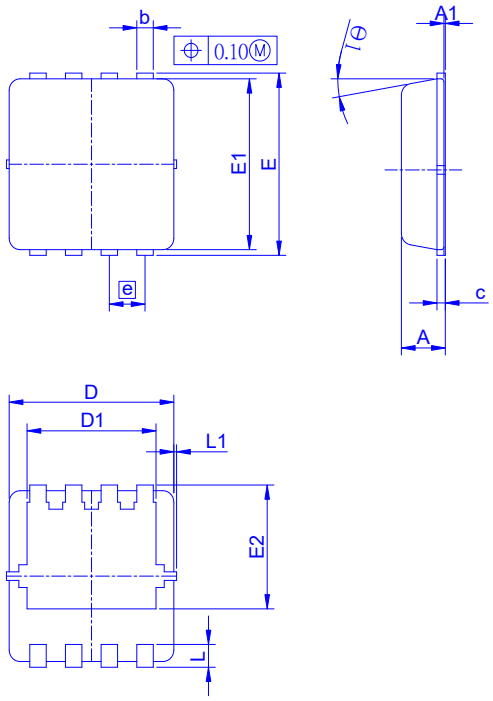
A: Assembly House

B: Year(A:2008 B:2009 C:2010….)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

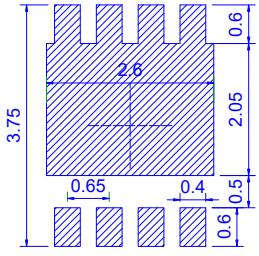
Outline Drawing



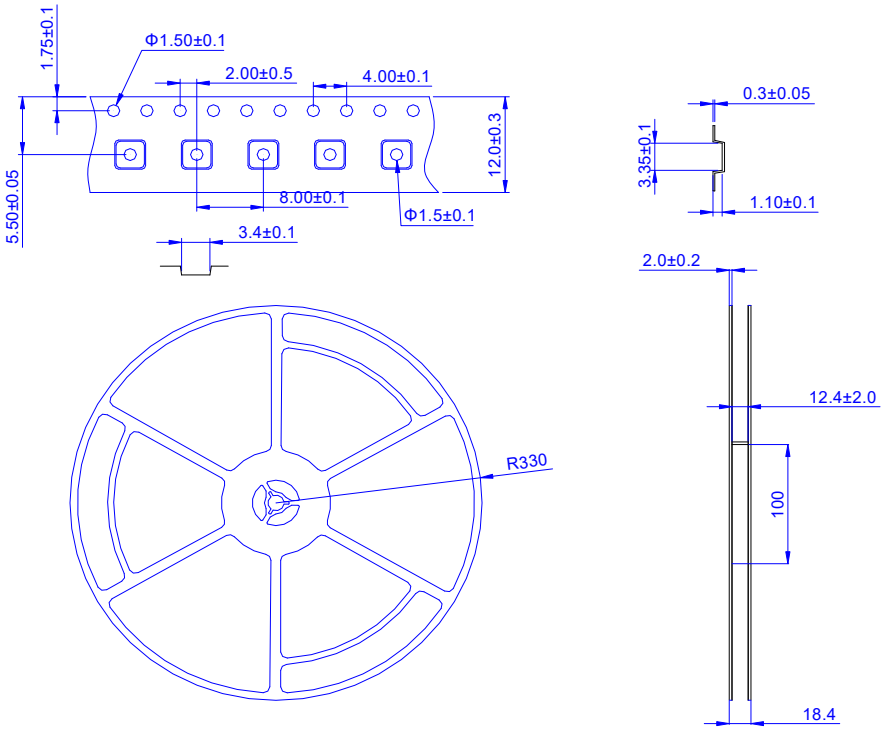
Dimension in mm

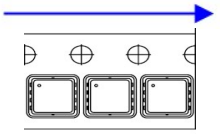
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ1
Min.	0.65	0	0.20	0.10	2.90	2.15	3.10	2.90	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.45	3.20	3.00	1.97	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.74	3.50	3.30	2.59	0.75	0.60	0.150	14°

Recommended minimum pads



Tape&Reel Information: 5000pcs/Reel



產品別	EDFN3X3
Reel 尺寸	13”
編帶方式	FEED DIRECTION 
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	1 : 1
內盒滿箱數	5K
內/外箱比	10 : 1
外箱滿箱數	50K