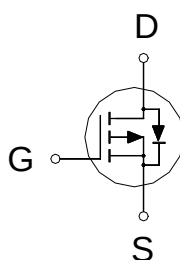


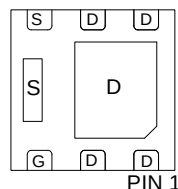
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-12V
$R_{DS(on)} (MAX.)$	20m Ω
I_D	-9.5A



Bottom View



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 8	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	-9.5	A
	$T_A = 70^\circ\text{C}$		-7.0	
Pulsed Drain Current ¹		I_{DM}	-38	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.08	W
	$T_A = 70^\circ\text{C}$		1.33	
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		12	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		60	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³60 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-12			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.4	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 8V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -10V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -4.5V$	-9.5			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -6A$		15	20	mΩ
		$V_{GS} = -2.5V, I_D = -5A$		19	25	
		$V_{GS} = -1.8V, I_D = -3A$		26	40	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -6A$		20		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		3100		pF
Output Capacitance	C_{oss}			460		
Reverse Transfer Capacitance	C_{rss}			413		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -5A$		25.5		nC
Gate-Source Charge ^{1,2}	Q_{gs}			2.2		
Gate-Drain Charge ^{1,2}	Q_{gd}			5.7		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6\Omega$		20		nS
Rise Time ^{1,2}	t_r			50		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			95		
Fall Time ^{1,2}	t_f			60		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I_S				-3	A
Pulsed Current ³	I_{SM}				-12	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			-1.2	V

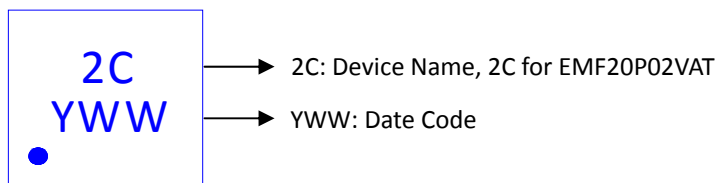
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

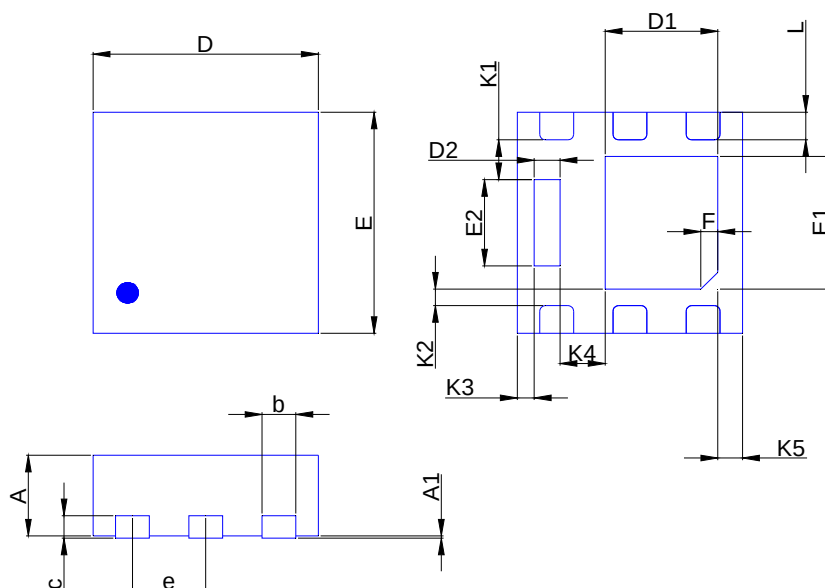
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMF20P02VAT for EDFN 2 x 2



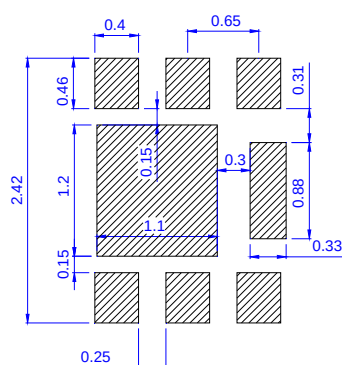
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.50	0.00	0.25		1.9	1.0	0.13	1.9	1.1	0.65				0.306	0.10	0.2	0.10	0.27	0.17
Typ.		0.02	0.30	0.1	2.0	1.1	0.25	2.0	1.2	0.75	0.65	0.15	45°	0.356	0.15	0.25	0.15		0.22
Max.	0.65	0.05	0.35		2.1	1.2	0.35	2.1	1.3	0.88				0.406	0.20	0.3	0.20		0.27

Recommended minimum pads





TYPICAL CHARACTERISTICS

