

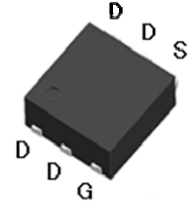
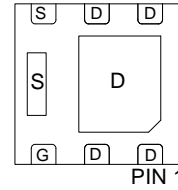
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	-20V
$R_{DS(on) (MAX.)}$	44m $\Omega$
$I_D$	-4.7A



Bottom View



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	-4.7	A
	$T_A = 70\text{ }^\circ\text{C}$		-3.5	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	-18.8	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	2.08	W
	$T_A = 70\text{ }^\circ\text{C}$		1.33	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		12	$^\circ\text{C} / \text{W}$
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$		60	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

<sup>3</sup>60 $^\circ\text{C} / \text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-20			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-0.4	-0.75	-1.2	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±12V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V			-1	μA
		V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			-10	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = -5V, V <sub>GS</sub> = -4.5V	-4.7			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.7A		35	44	mΩ
		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -3.5A		55	70	
		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -1.5A		65	90	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -4.7A		14		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -10V, f = 1MHz		679		pF
Output Capacitance	C <sub>oss</sub>			124		
Reverse Transfer Capacitance	C <sub>rss</sub>			106		
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -10V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.7A		12.8		nC
Gate-Source Charge <sup>1,2</sup>	Q <sub>gs</sub>			2.2		
Gate-Drain Charge <sup>1,2</sup>	Q <sub>gd</sub>			4.1		
Turn-On Delay Time <sup>1,2</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> = -10V, I <sub>D</sub> = -1A, V <sub>GS</sub> = -4.5V, R <sub>GS</sub> = 6Ω		12		nS
Rise Time <sup>1,2</sup>	t <sub>r</sub>			25		
Turn-Off Delay Time <sup>1,2</sup>	t <sub>d(off)</sub>			35		
Fall Time <sup>1,2</sup>	t <sub>f</sub>			25		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				-3	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				-12	
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			-1.2	V

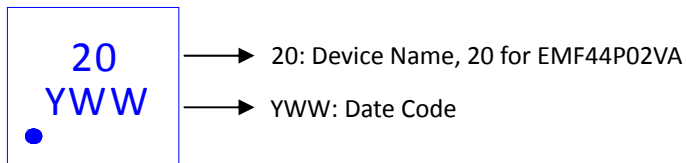
<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

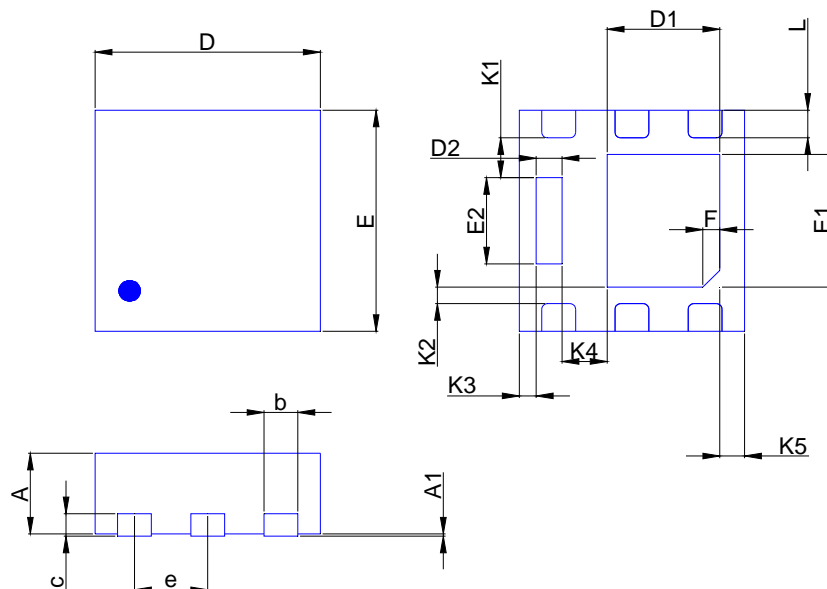
<sup>3</sup>Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMF44P02VA for EDFN 2 x 2



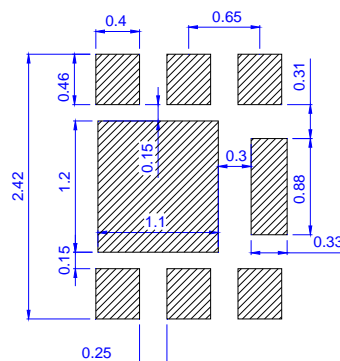
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.70	0.00	0.25		1.9	0.9	0.13	1.9	1.1	0.68				0.306	0.10	0.2	0.10	0.35	0.17
Typ.	0.75	0.02	0.30	0.203	2.0	1.0	0.23	2.0	1.2	0.78	0.65	0.15	45°	0.356	0.15	0.25	0.15	0.40	0.22
Max.	0.80	0.05	0.35		2.1	1.1	0.33	2.1	1.3	0.88				0.406	0.20	0.3	0.20	0.45	0.27

Recommended minimum pads





TYPICAL CHARACTERISTICS

