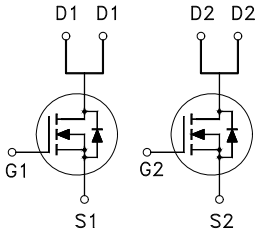
杰力科技股份有限公司
Excelliance MOS Corporation

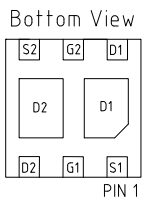
EMF50A02VA

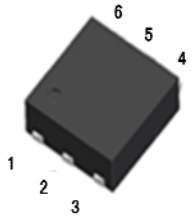
Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	20V
$R_{DSON\ (MAX.)}$	45mΩ
I_D	4.8A







Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	4.8	A
	T_A = 70 °C		3.8	
Pulsed Drain Current[1]		I_{DM}	19.2	
Power Dissipation	T_A = 25 °C	P_D	1.9	W
	T_A = 70 °C		1.2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		15	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		65	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]65°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

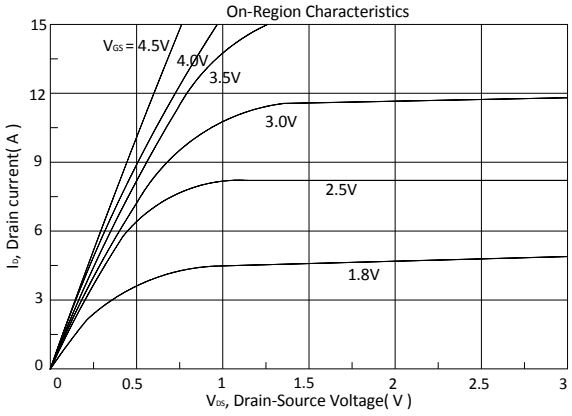
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.4	0.75	1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	μA
		V_{DS} = 16V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	4.8			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 3.5A		36	45	mΩ
		V_{GS} = 2.5V, I_D = 2A		43	60	
		V_{GS} = 1.8V, I_D = 1A		58	85	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 3.5A		5		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		355		pF
Output Capacitance	C_{oss}			56		
Reverse Transfer Capacitance	C_{rss}			40		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		3.2		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 10V, V_{GS} = 4.5V, I_D = 3.5A		4.6		nC
Gate-Source Charge[1,2]	Q_{gs}			0.66		
Gate-Drain Charge[1,2]	Q_{gd}			1.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6Ω		8		nS
Rise Time[1,2]	t_r			10		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			20		
Fall Time[1,2]	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				4.8	A
Pulsed Current[3]	I_{SM}				19.2	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V

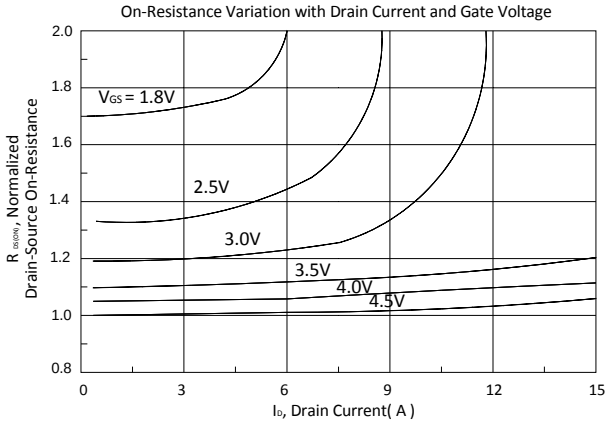
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

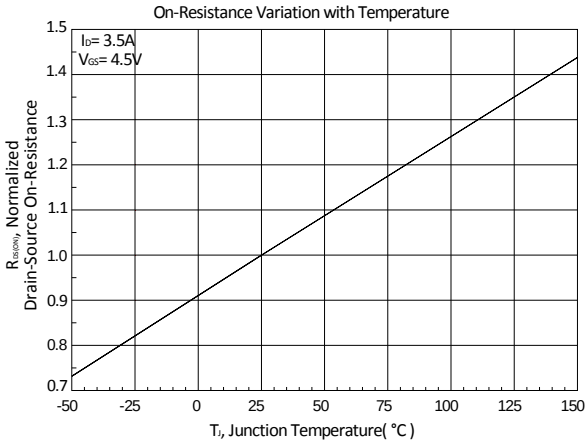
[2]Independent of operating temperature.

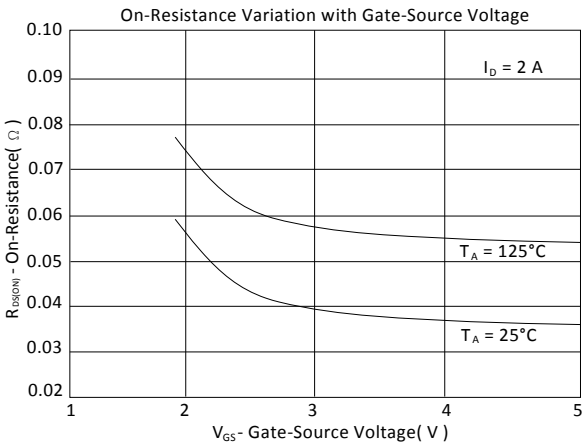
[3]Pulse width limited by maximum junction temperature.

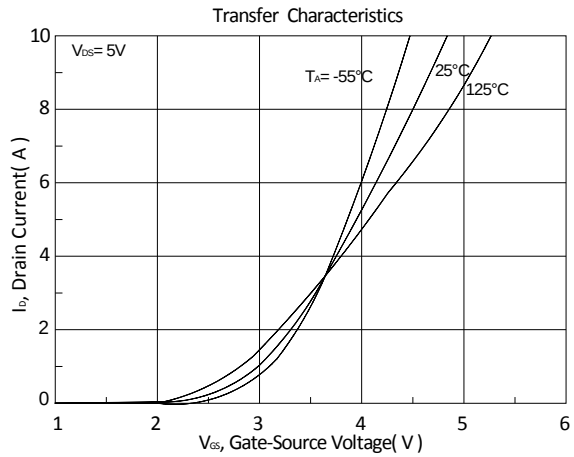
TYPICAL CHARACTERISTICS

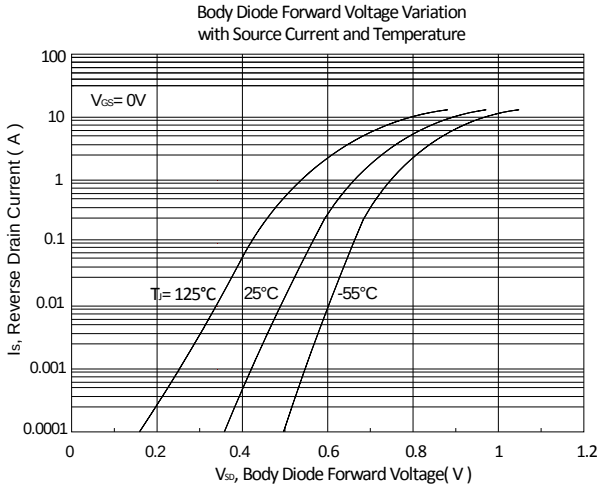


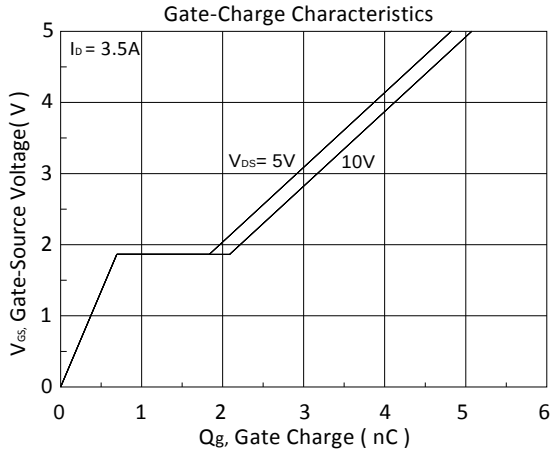


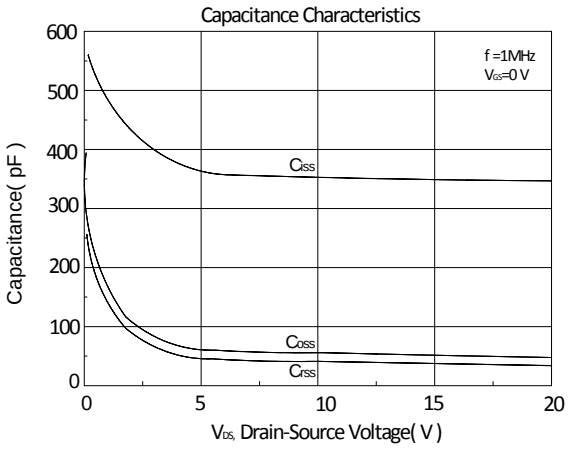


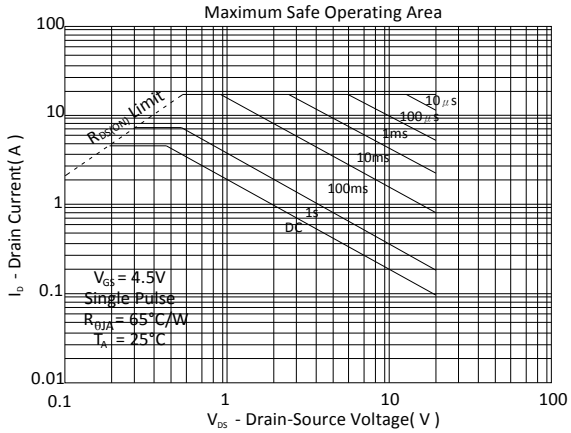


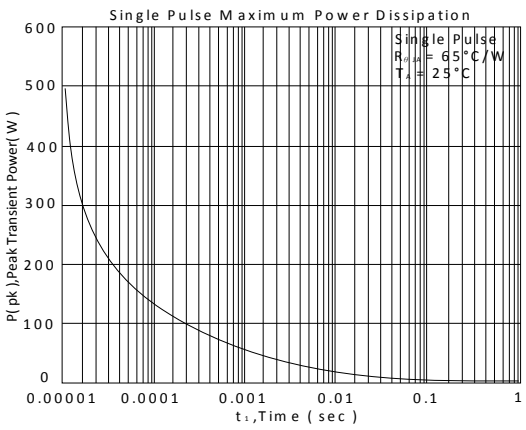


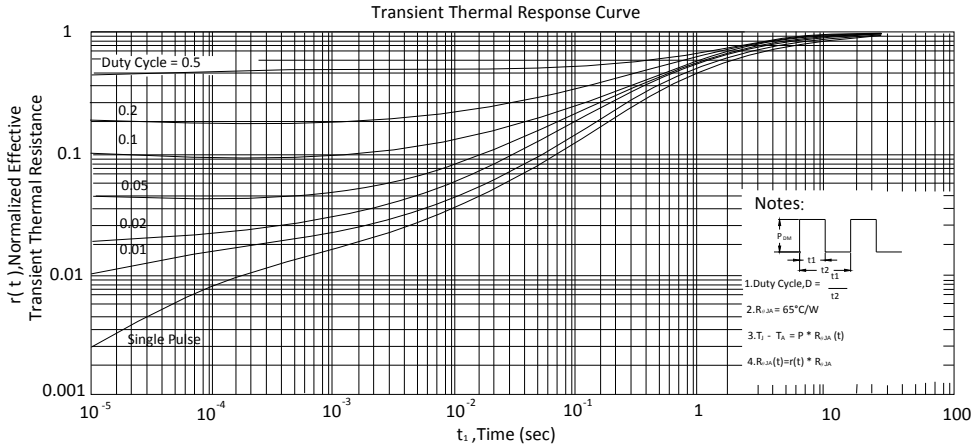



Gate-Charge Characteristics
ID = 3.5A
VDS= 5V
10V
VGS, Gate-Source Voltage(V)
Qg, Gate Charge (nC)


Capacitance Characteristics
f =1MHz
VGS=0 V
Ciss
Coss
Crss
Capacitance(pF)
VDS, Drain-Source Voltage(V)

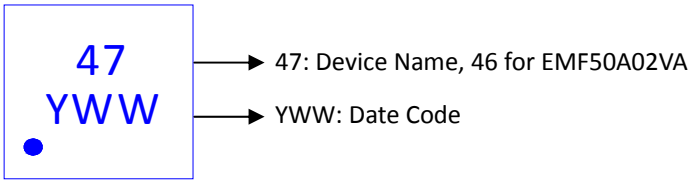

Maximum Safe Operating Area
RDS(ON) Limit
10 μs
100 μs
1ms
10ms
100ms
1s
DC
VGS = 4.5V
Single Pulse
RθJA = 65°C/W
TA = 25°C
ID - Drain Current(A)
VDS - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
RθJA = 65°C/W
TA = 25°C
P(pk),Peak Transient Power(W)
t1 ,Time (sec)

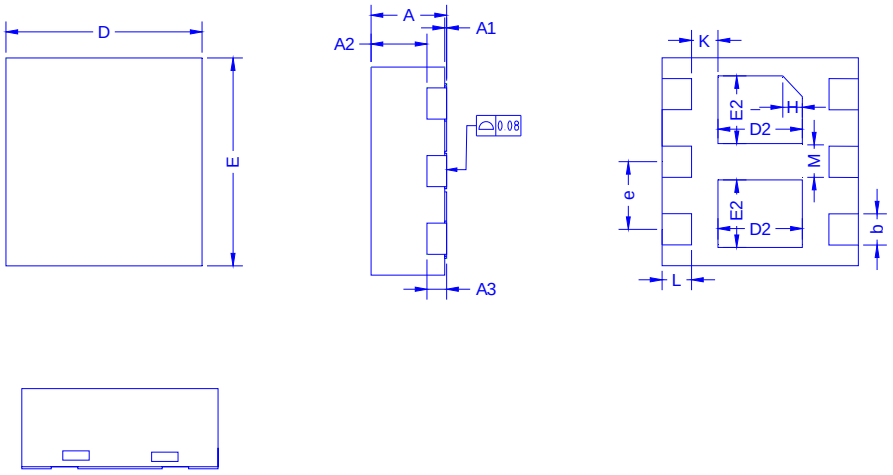

Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.RθJA = 65°C/W
3.TJ - TA = P * RθJA (t)
4.RθJA(t)=r(t) * RθJA
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (sec)

Ordering & Marking Information:

Device Name: EMF50A02VA for EDFN 2 x 2



Outline Drawing



Dimension in mm

Dimension	A	A1	A2	A3	b	D	E	D2	E2	e	H	K	L	M
Min.	0.70	0.00	0.50	0.20 REF	0.25	1.90	1.90	0.76	0.55	0.55	0.20 REF	0.17	0.25	0.25
Max.	0.80	0.05	0.60		0.35	2.10	2.10	0.96	0.75	0.75		0.37	0.35	0.45

Recommended minimum pads