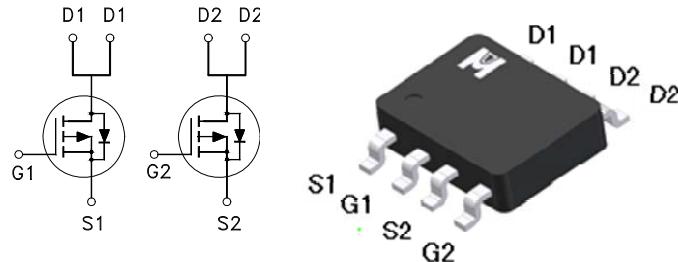


Dual P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	-20V
R _{DSON} (MAX.)	100mΩ
I _D	-3A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNIT
Gate-Source Voltage	V _{GS}	±12	V
Continuous Drain Current	I _D	-3	A
		-2.4	
Pulsed Drain Current ¹	I _{DM}	-16	
Power Dissipation	P _D	2	W
		1.2	
Operating Junction & Storage Temperature Range	T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	25	62.5	°C / W
Junction-to-Ambient ³	R _{θJA}			

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³62.5°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, Unless Otherwise Noted)

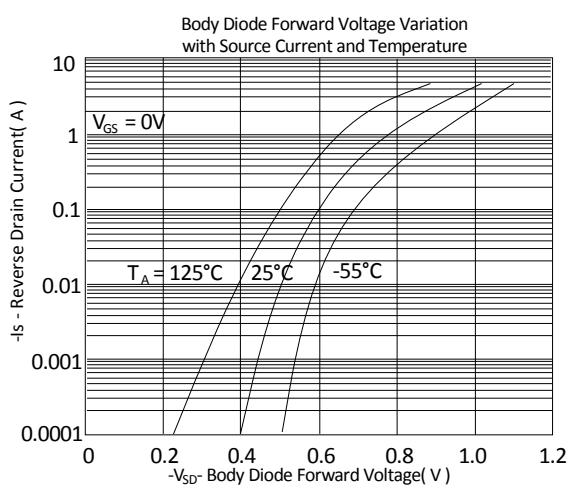
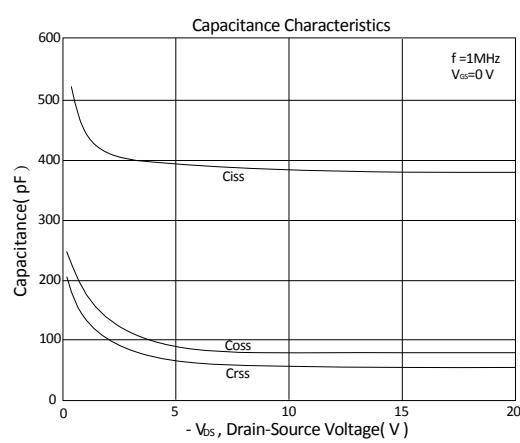
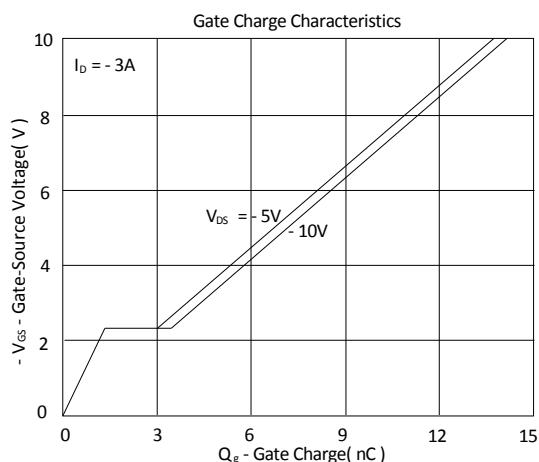
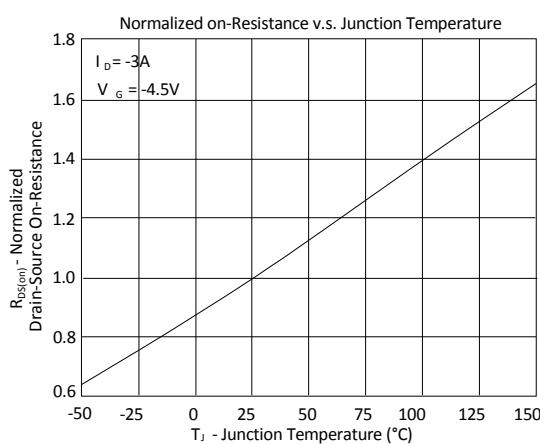
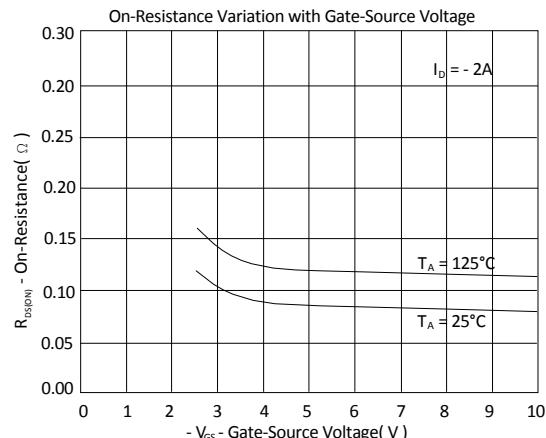
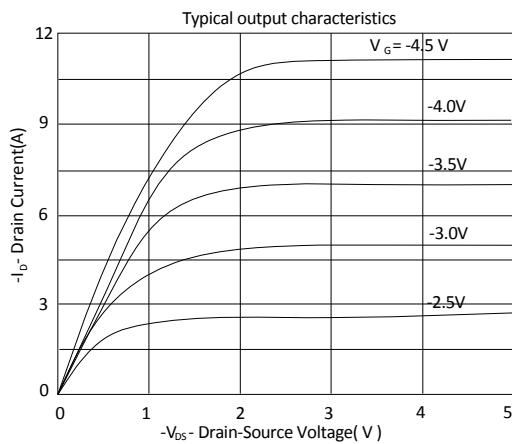
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-20			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.3	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			-10	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = -5V, V_{GS} = -4.5V$	-3			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = -4.5V, I_D = -3A$		85	100	$\text{m}\Omega$
		$V_{GS} = -2.5V, I_D = -2.5A$		120	150	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -3A$		4.5		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -10V, f = 1\text{MHz}$		382		pF
Output Capacitance	C_{oss}			70		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -3A$		7.2		nC
Gate-Source Charge ^{1,2}	Q_{gs}			1.2		
Gate-Drain Charge ^{1,2}	Q_{gd}			2.3		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6\Omega$		10		nS
Rise Time ^{1,2}	t_r			20		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			15		
Fall Time ^{1,2}	t_f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S				-2.3	A
Pulsed Current ³	I_{SM}				-9.2	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V

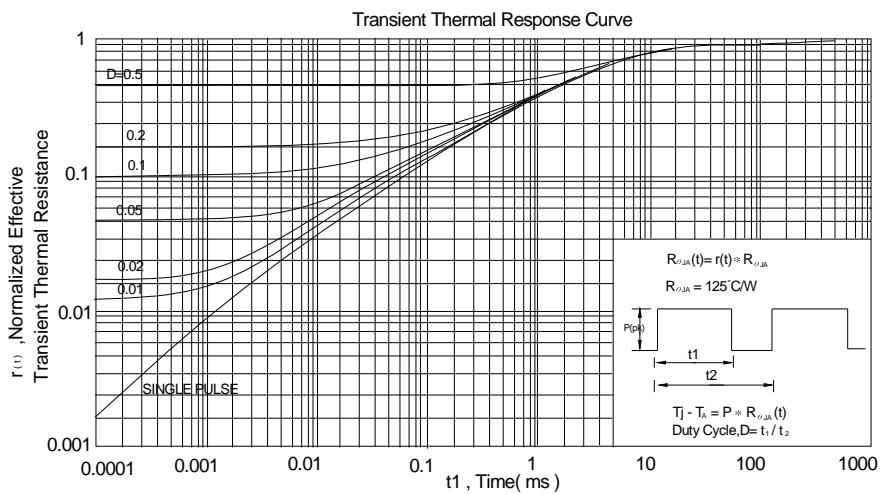
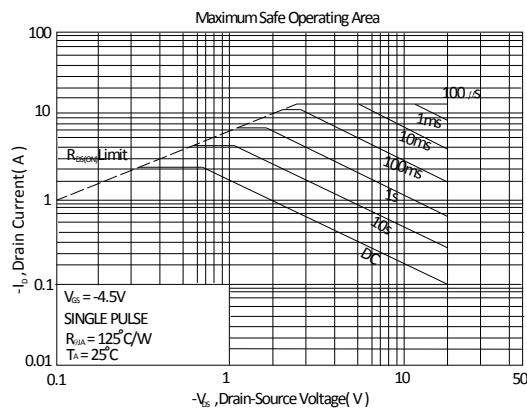
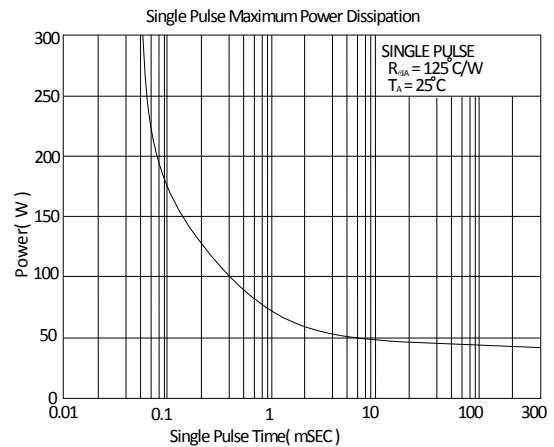
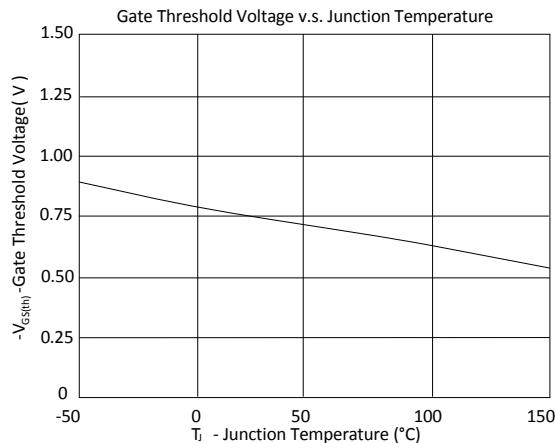
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

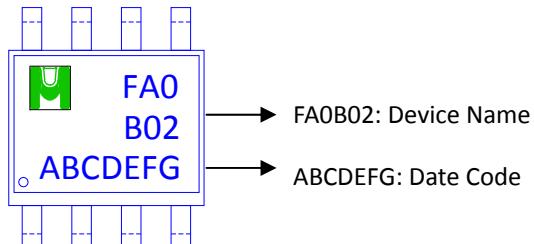
TYPICAL CHARACTERISTICS



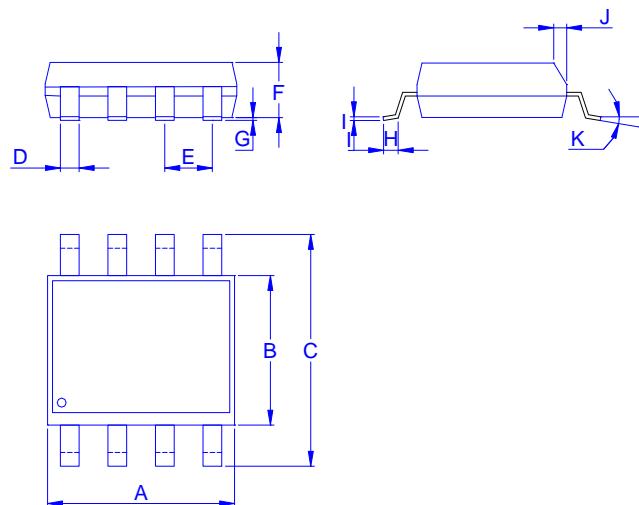


Ordering & Marking Information:

Device Name: EMFA0B02G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°