# EMIF04-EAR02M8

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## 4-line IPAD™ EMI filter and ESD protection for headset

## Features

- Lead-free package
- High attenuation: -30 dB at 900 MHz
- Low cut-off frequencies: 60 MHz for speaker lines
- High current capability: 50 mA per line
- Very low PCB space consumption: 1.5 mm x 1.7 mm
- Very thin package: 0.6 mm maximum
- High efficiency in ESD suppression IEC6 1000-4-2 level 4
- High reliability offered by monolithic integration

### Complies with following standards:

- IEC 61000-4-2 level 4 input pins
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

## Applications

- Mobile phones

## Description

The EMIF04-EAR02M8 chip is a highly integrated device designed to suppress EMI/RFI noise for headset mobile phone. The new LC architecture on the speaker lines provides a high attenuation value maintaining a very low serial resistance.

The 8-lead micro-QFN package offers the possibility to integrate the whole function in a very small PCB space.

Additionally, this filter includes ESD protection circuitry, which prevents damage to the protected device when subjected to ESD surges up 30 kV.

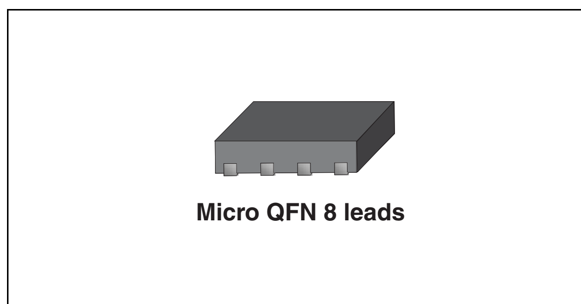



Figure 1. Pin configuration (bottom side)

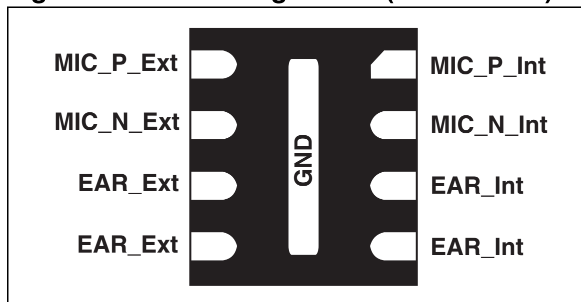
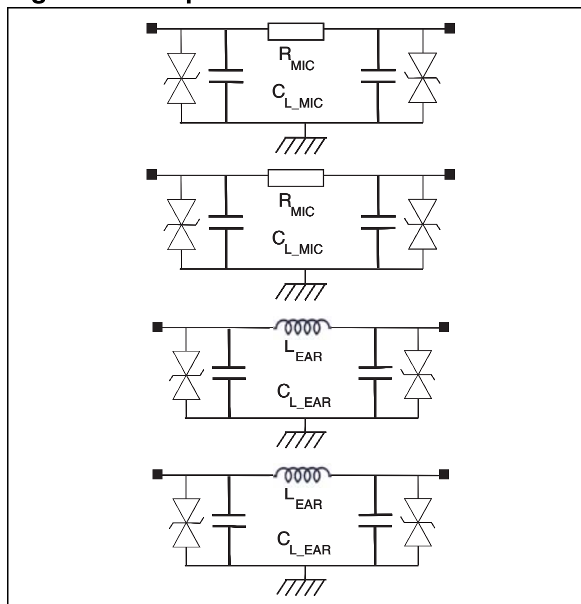



Figure 2. Equivalent circuit

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# 1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb}$ = 25 °C)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{PP}$ | ESD IEC 61000-4-2<br>air discharge<br>contact discharge | <br>30<br>30 | kV |
| $I_{EAR}$ | Maximum rms current per channel | 50 | mA |
| $T_j$ | Operating junction temperature | -30 to 125 | °C |
| $T_{stg}$ | Storage temperature range | -55 to +150 | °C |

Figure 3. Electrical symbols and parameters

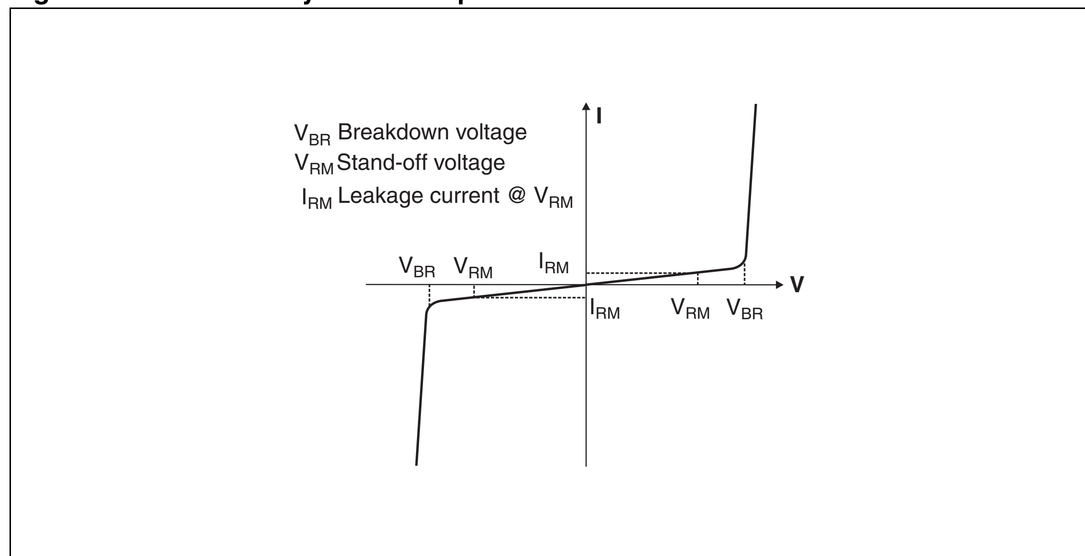


Table 2. Electrical characteristics ($T_{amb}$ = 25 °C)

| Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{BR}$ | $I_R$ = 1 mA | 7 | | | V |
| $I_{RM}$ | $V_{RM}$ = 3 V | | | 100 | nA |
| $L_{EAR}$ | | | 1.5 | | nH |
| $R_L$ | Parasitic resistance of inductor $L_{EAR}$ | | 0.30 | 0.6 | Ω |
| $R_{MIC}$ | | 54 | 68 | 82 | Ω |
| $C_{L_EAR}$ | $V_R$ = 0 V DC, 1 MHz | 84 | 105 | 126 | pF |
| $C_{L_MIC}$ | $V_R$ = 0 V DC, 1 MHz | 60 | 76 | 92 | pF |
| $F_{c_EAR}$ | Cut-off frequency earphone line:<br>$Z_{SOURCE} = Z_{LOAD}$ = 50 Ω | | 60 | | MHz |
| $F_{c_MIC}$ | Cut-off frequency microphone line:<br>$Z_{SOURCE} = Z_{LOAD}$ = 50 Ω | | 70 | | MHz |



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**Figure 4. S21 attenuation measurement**

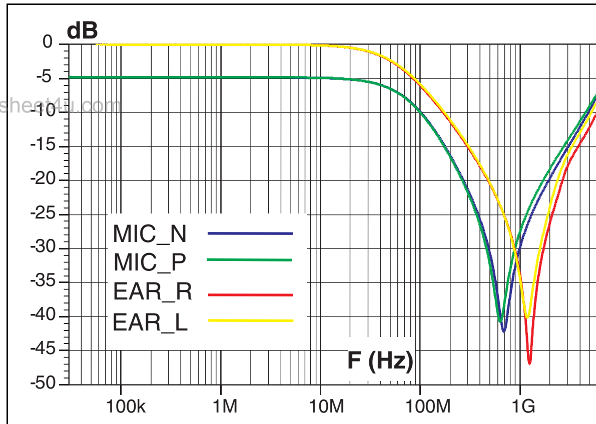


**Figure 5. Analog cross talk measurements**

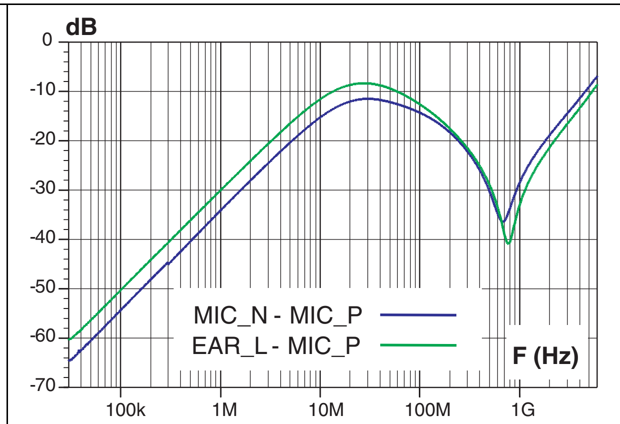


**Figure 6. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one MIC input ($V_{in}$) and on one MIC output**

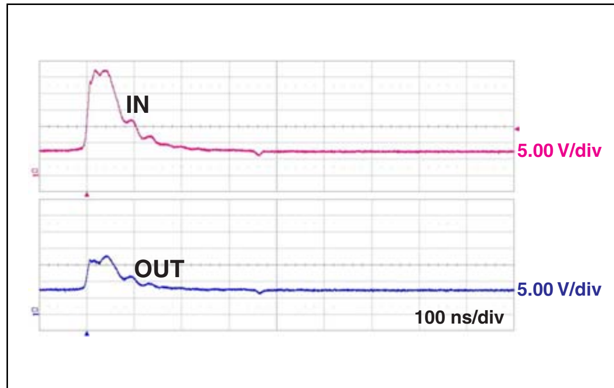


**Figure 7. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one MIC input ($V_{in}$) and on one MIC output**

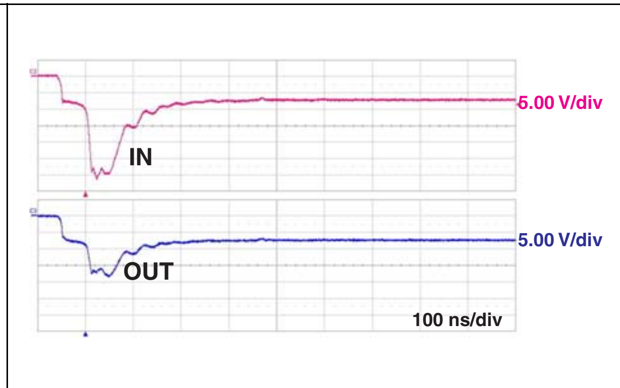


**Figure 8. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one EAR input ($V_{in}$) and on one EAR output**

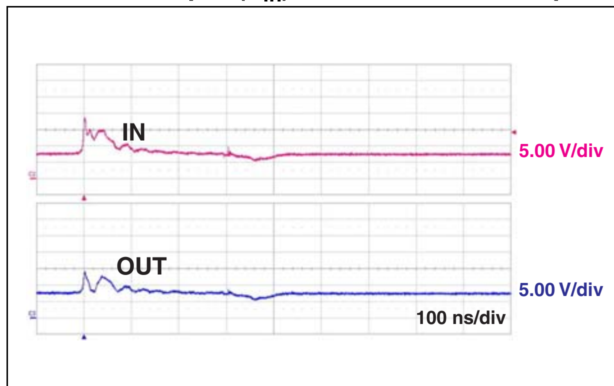


**Figure 9. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one EAR input ($V_{in}$) and on one EAR output**

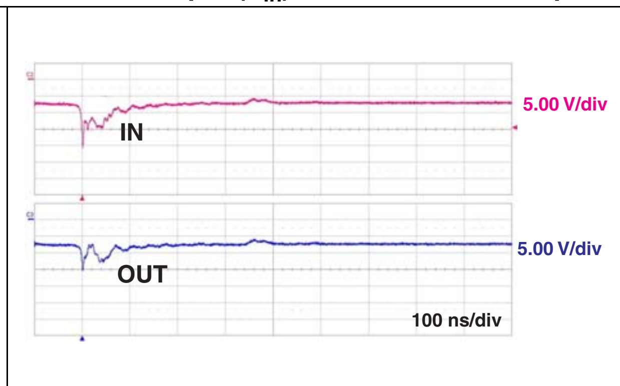




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**Figure 10. Relative line capacitance variation versus applied voltage**

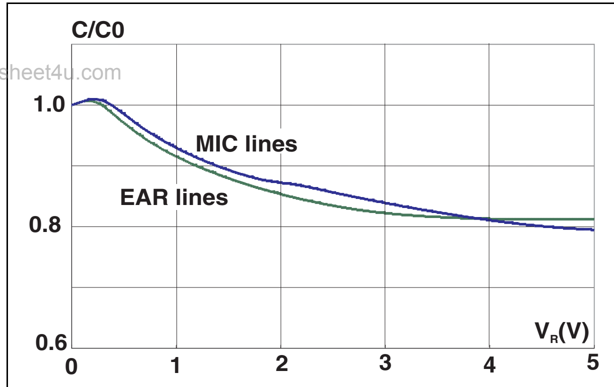



**Figure 11. Total harmonic distortion with noise: MIC lines, R = 10 kΩ**

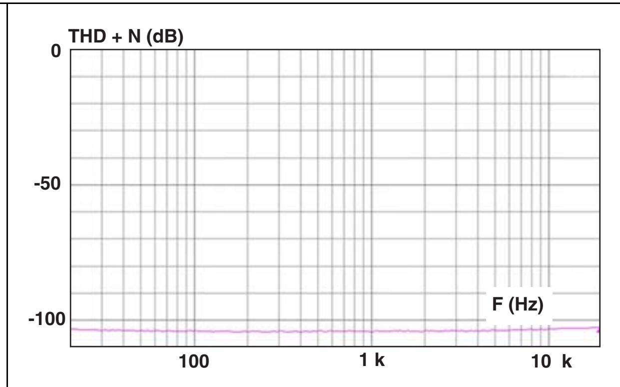



**Figure 12. Total harmonic distortion with noise: MIC lines, R = 32 Ω**

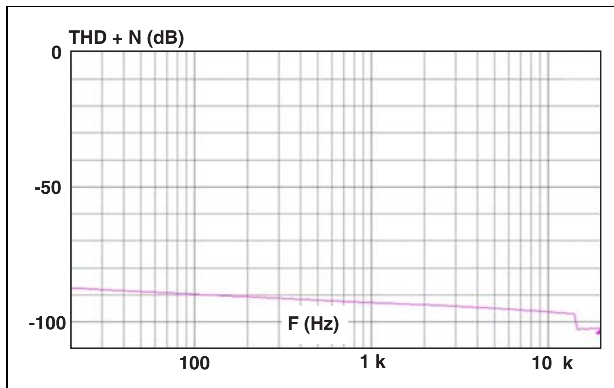



**Figure 13. Total harmonic distortion with noise: EAR lines, R = 32 Ω**

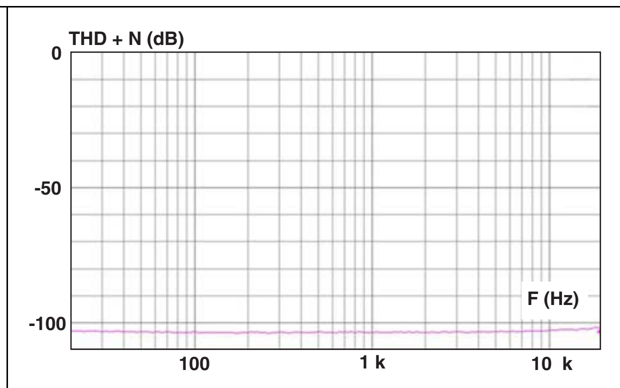
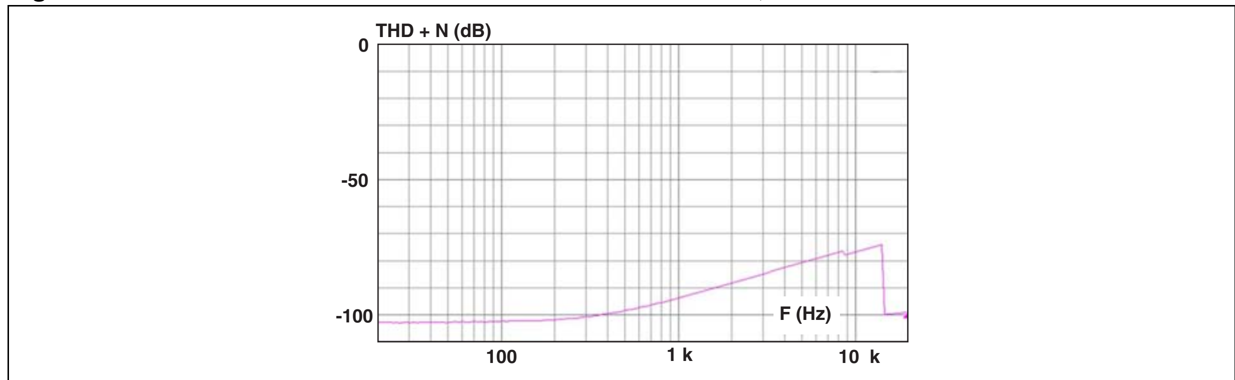



**Figure 14. Total harmonic distortion with noise: EAR lines, R = 8 Ω**



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# 2 Application information

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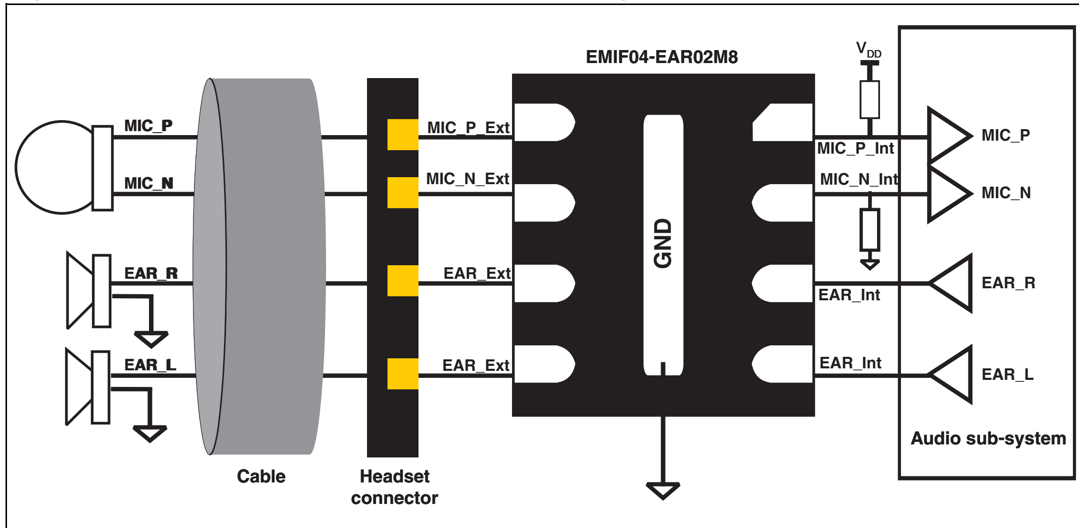
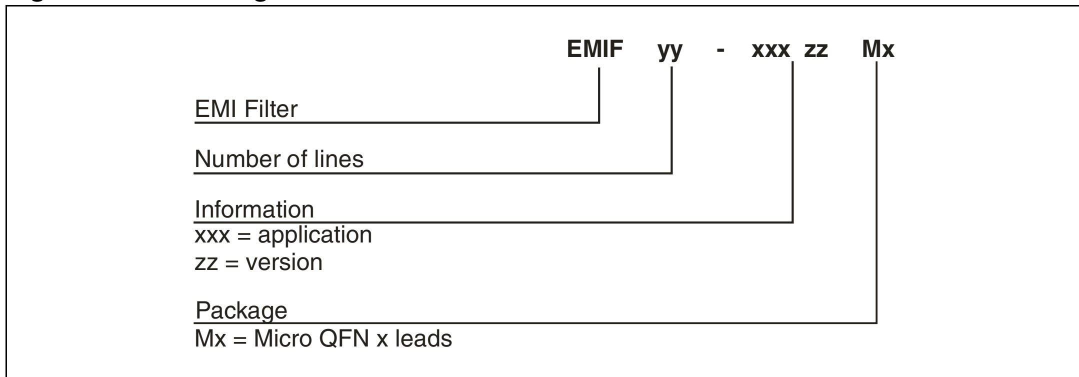
**Figure 15. Example of application scheme using EMIF04-EAR02M8**




# 3 Ordering information scheme

**Figure 16. Ordering information scheme**



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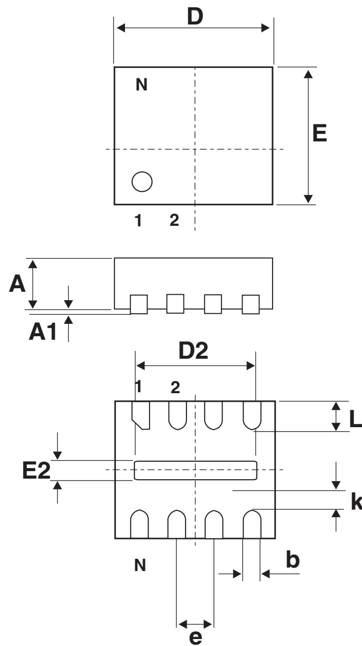
# 4 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

**Table 3. Micro QFN dimensions**




| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.15 | 0.18 | 0.25 | 0.006 | 0.007 | 0.001 |
| D | 1.65 | 1.70 | 1.75 | | 0.067 | |
| D2 | 1.15 | 1.3 | 1.4 | 0.045 | 0.051 | 0.055 |
| E | 1.45 | 1.50 | 1.55 | | 0.059 | |
| E2 | 0.05 | 0.20 | 0.30 | 0.002 | 0.008 | 0.012 |
| e | | 0.40 | | | 0.016 | |
| k | 0.20 | | | 0.008 | | |
| L | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |

**Figure 17. Footprint**

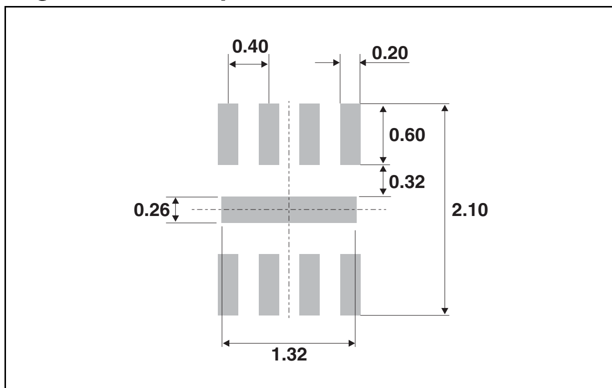



**Figure 18. Marking**

Dot: Pin1 identification
XX = Marking

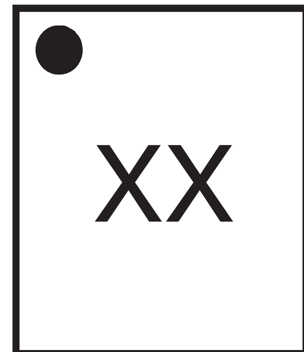





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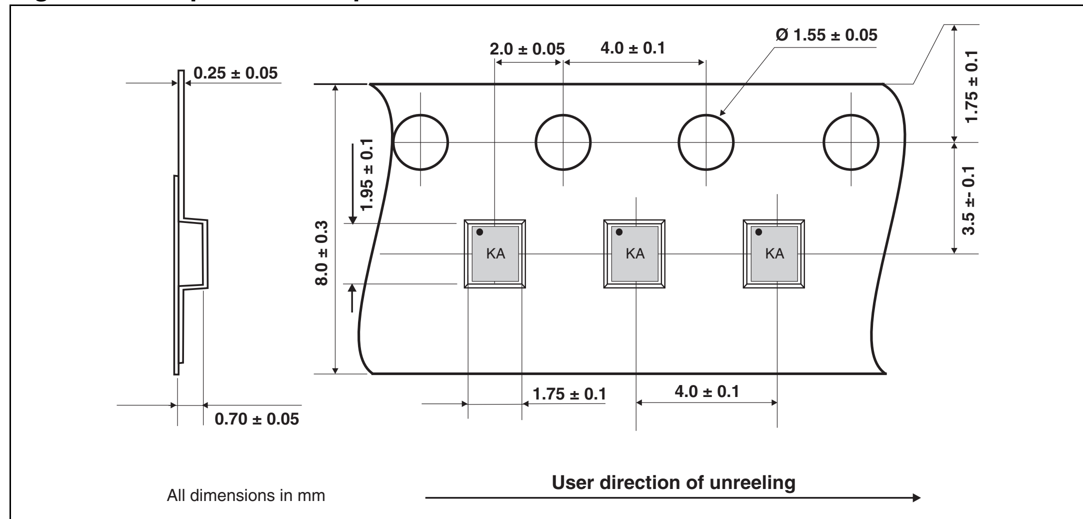
**Figure 19. Tape and reel specification**




Note: *Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.*



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# 5 Recommendation on PCB assembly

## 5.1 Stencil opening design

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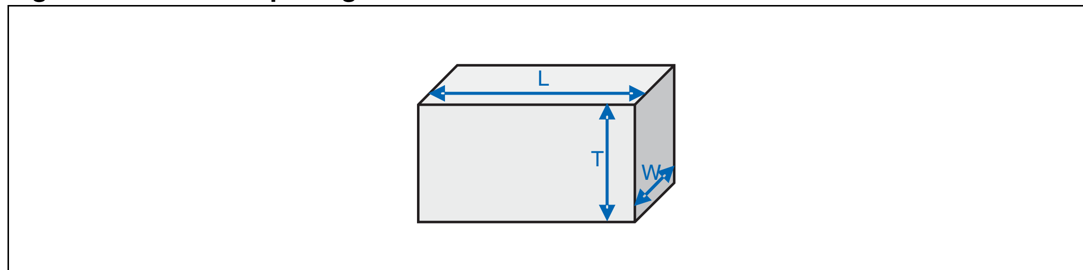
1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

**Figure 20. Stencil opening dimensions**




   b) General design rule

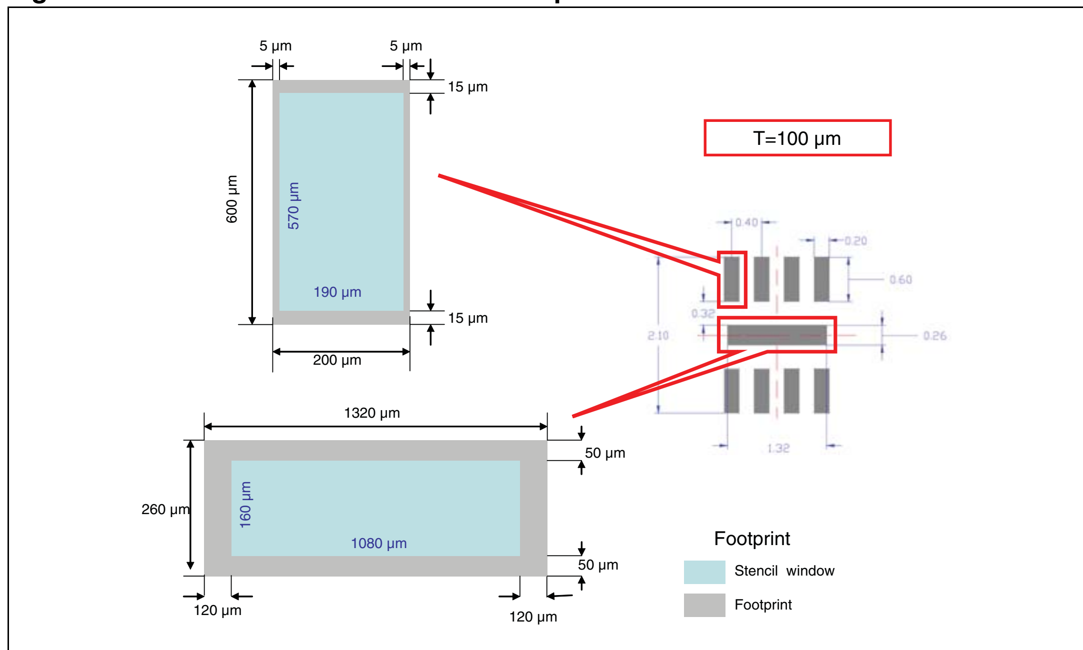
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c) Stencil opening for leads: Opening to footprint ratio is 90%.

**Figure 21. Recommended stencil window position**



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## 5.2 Solder paste

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1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

## 5.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 5.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.



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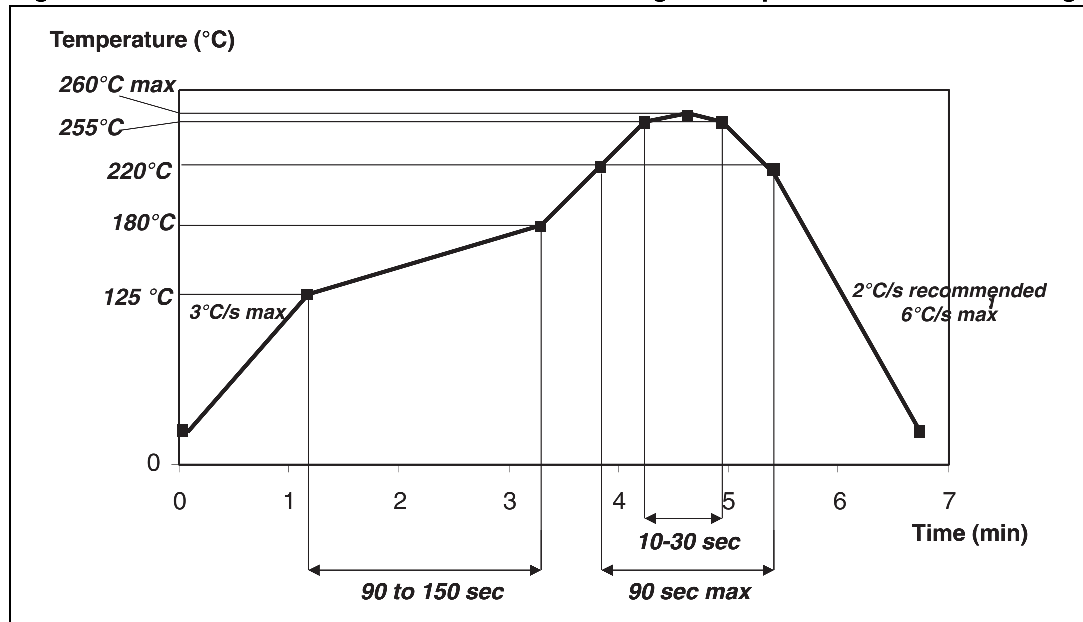
## 5.5 Reflow profile

**Figure 22. ST ECOPACK® recommended soldering reflow profile for PCB mounting**




*Note: Minimize air convection currents in the reflow oven to avoid component movement.*



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# 6 Ordering information

Table 4. Ordering information

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| EMIF04-EAR02M8 | KA(1) | Micro QFN | 3.8 mg | 3000 | Tape and reel |

1. The marking can be rotated by 90° to differentiate assembly location

# 7 Revision history

Table 5. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 24-Mar-2009 | 1 | Initial release |



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