EMIF10-1K010F1

10 LINES EMI FILTER AND ESD PROTECTION

IPAD™

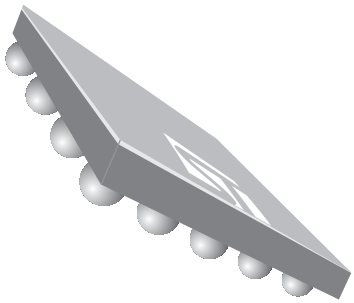
MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required :

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

The EMIF10-1K010F1 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 flip chip packaging means the package size is equal to the die size.
This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

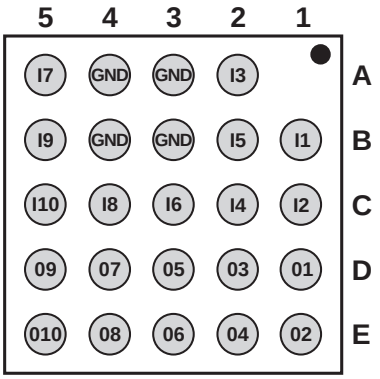


Flip Chip package

BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 2.57mm x 2.57mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

PIN CONFIGURATION (ball side)



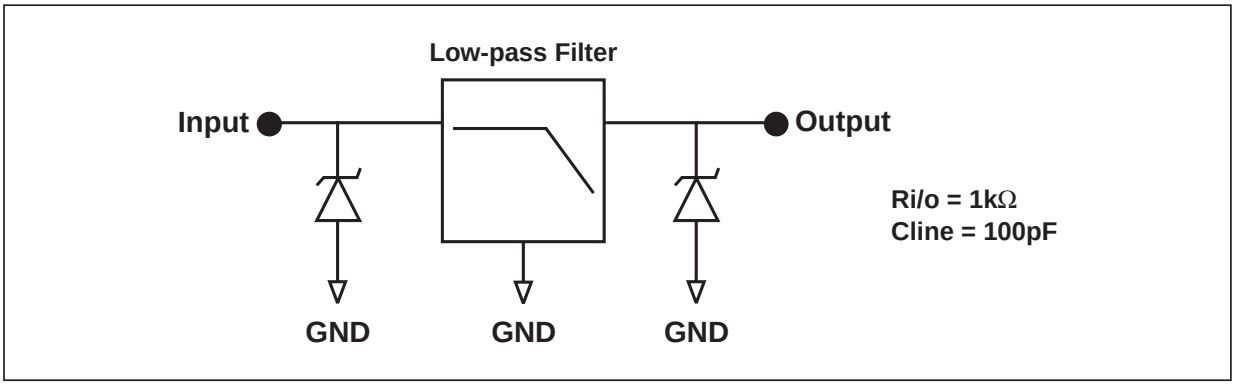
COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

Level 4	15kV	(air discharge)
	8 kV	(contact discharge)

MIL STD 883E - Method 3015-6 Class 3

BASIC CELL CONFIGURATION



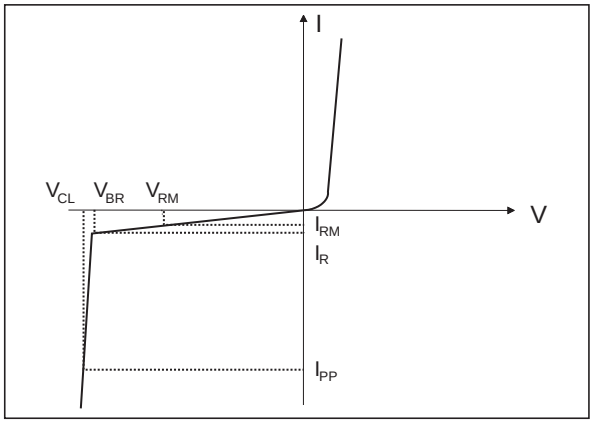
TM : IPAD is a trademark of STMicroelectronics.

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C)

Symbol	Parameter and test conditions	Value	Unit
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{in}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1mA	6	8	10	V
I_{RM}	V_{RM} = 3V per line			500	nA
$R_{I/O}$		900	1000	1100	Ω
C_{line}	At 0V bias	80	100	120	pF

Fig. 1: S21(dB) attenuation measurement and Aplac simulation.

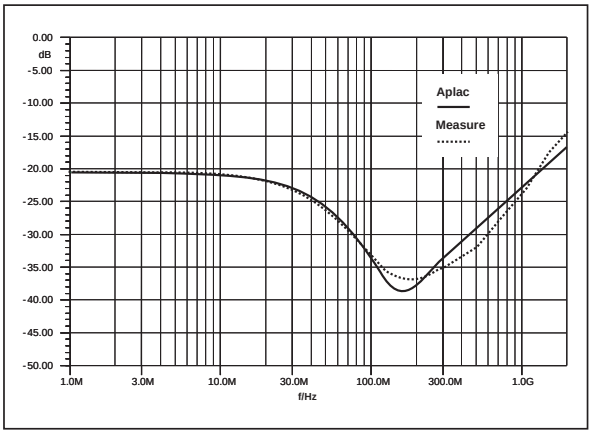


Fig. 2: Analog crosstalk measurements.

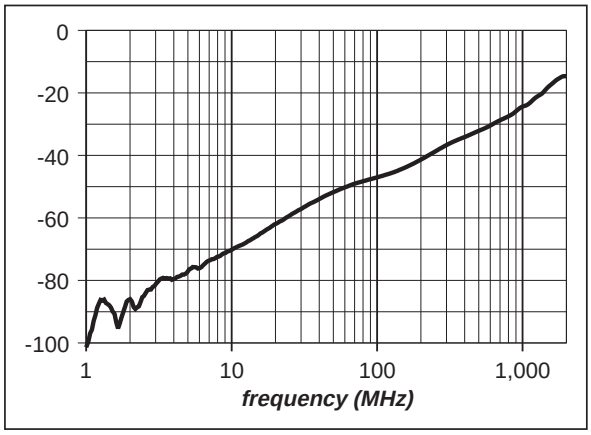


Fig. 3: Digital crosstalk measurement.

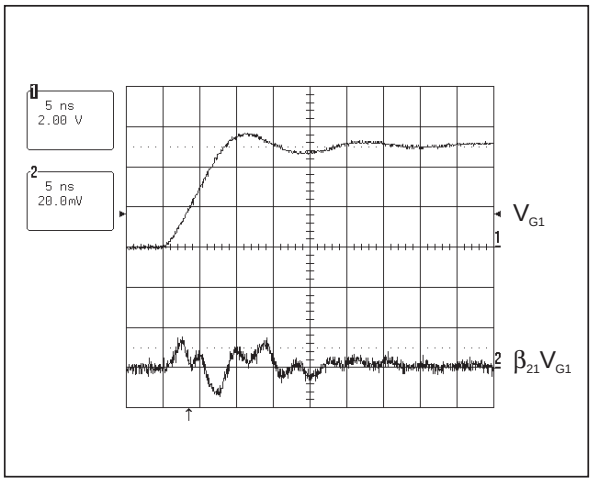


Fig. 4: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout).

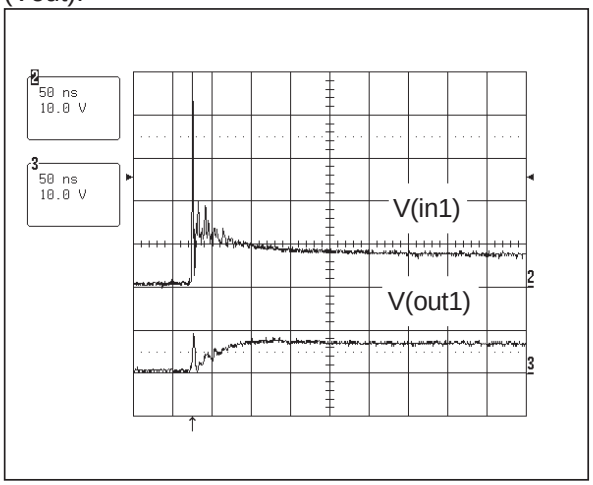


Fig. 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout).

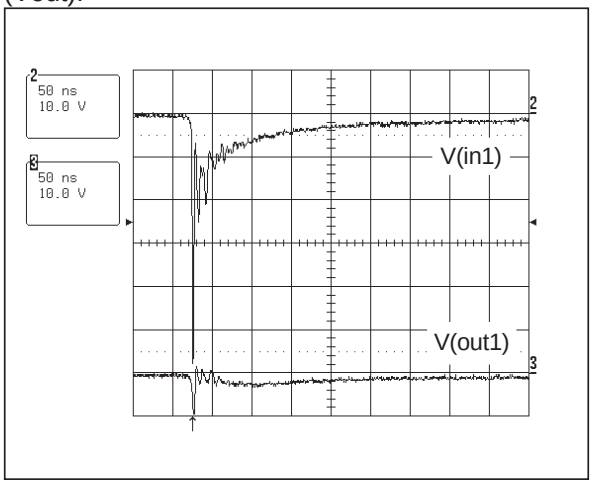


Fig. 6: Line capacitance versus applied voltage.

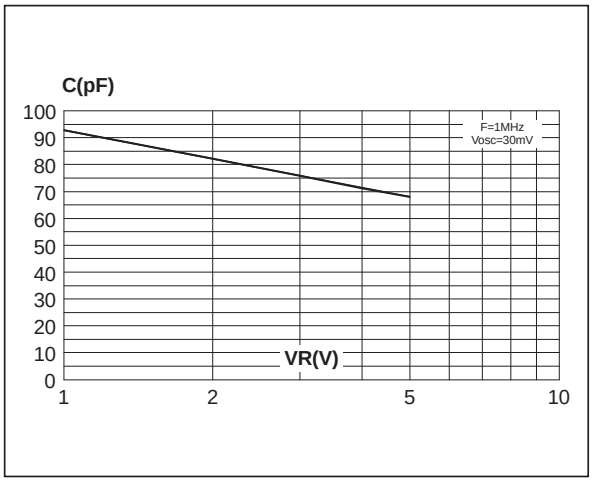


Fig. 7: Aplac model single line structure.

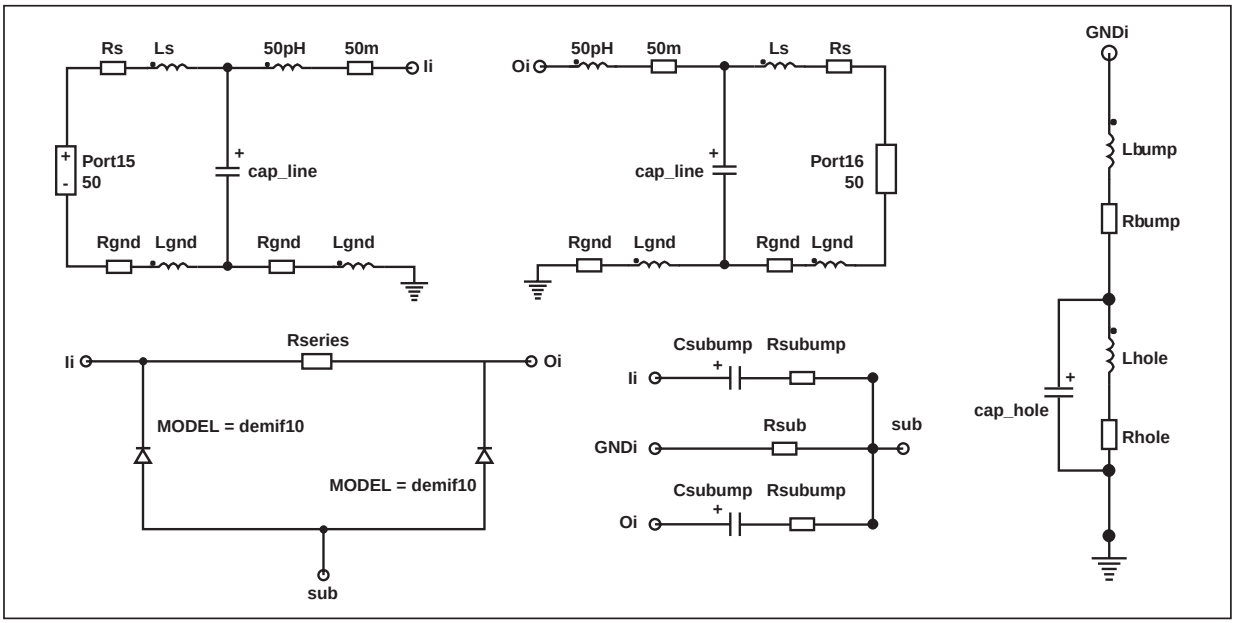
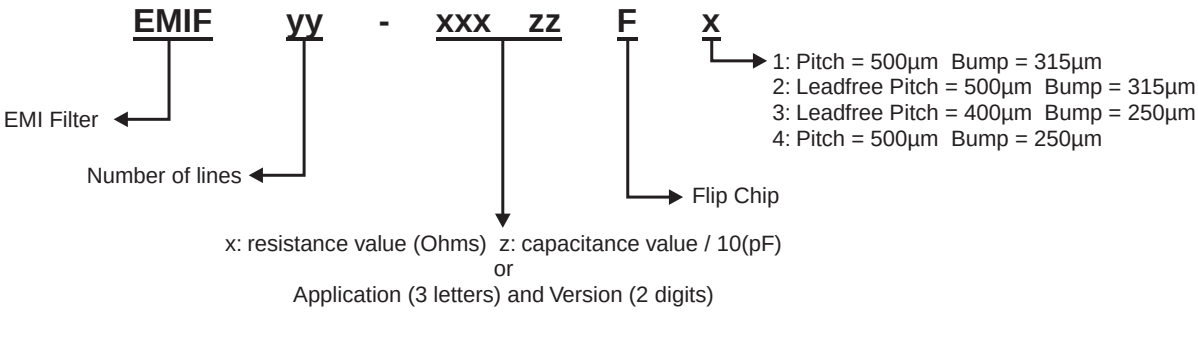


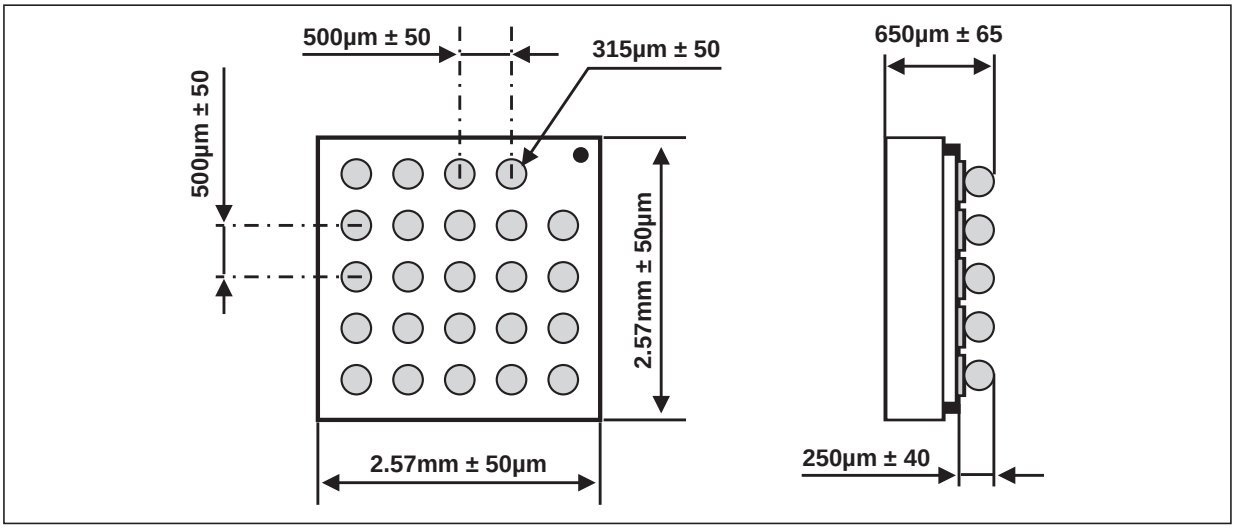
Fig. 8: Aplac model parameters.

aplacvar	Cz	57pF	Model demif10
aplacvar	Rseries	960	BV = 7
aplacvar	cap_line	0.8pF	IBV = 1m
aplacvar	Ls	0.6nH	CJO = Cz
aplacvar	Rbump	50m	M = 0.3333
aplacvar	Lbump	50pH	Rs = 1
aplacvar	Rs	0.15	VJ = 0.6
aplacvar	Csubump	15pF	TT = 100n
aplacvar	Rsubump	0.15	
aplacvar	Rsub	0.1	
aplacvar	lhole	1.2nH opt	
aplacvar	Rhole	0.15	
aplacvar	cap_hole	0.15pF	
aplacvar	Rgnd	0.25	
aplacvar	lgnd	0.4nH	

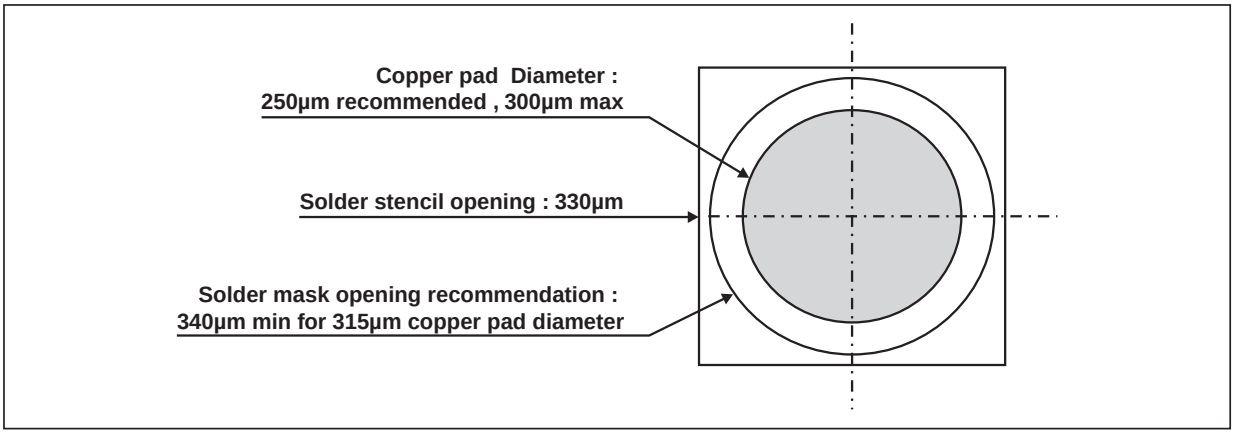
ORDER CODE



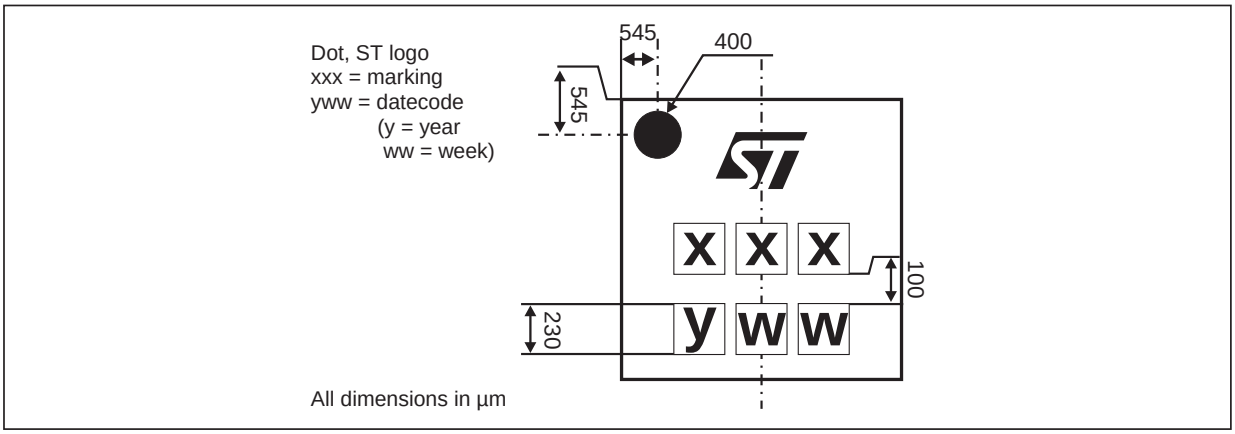
PACKAGE MECHANICAL DATA
FLIP CHIP



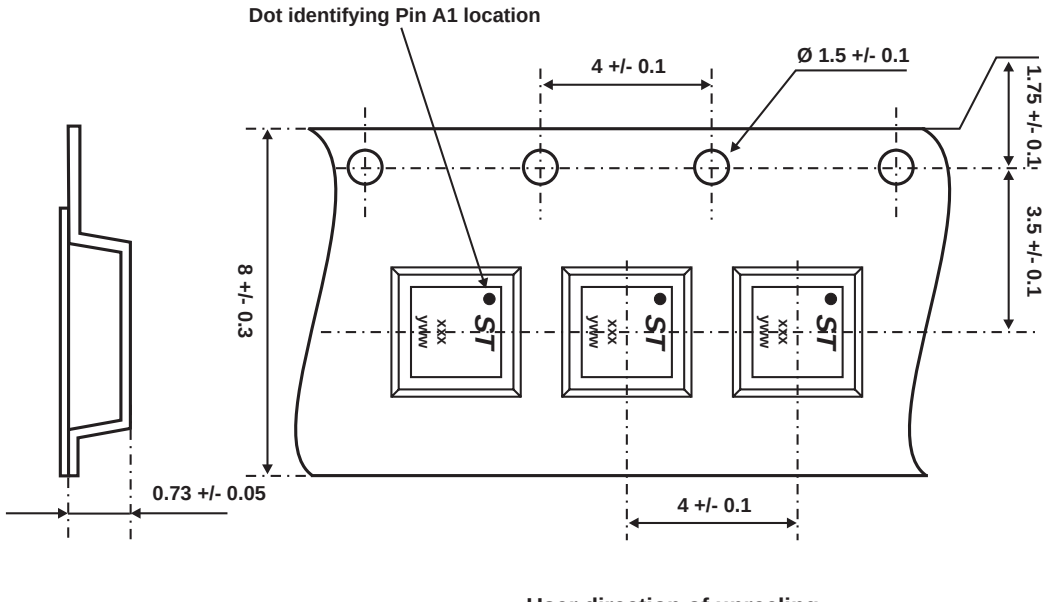
FOOT PRINT RECOMMENDATIONS



MARKING



PACKING



OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-1K010F1	FDT	Flip Chip	9.2 mg	5000	Tape & reel (7”)

Note: More information are available in the application notes:
- AN1235: "Flip-Chip: Package description and recommandations for use"
- AN1751: "EMI Filters: Recommendations and measurements"