EMIF10-1K010F2

EMI FILTER INCLUDING ESD PROTECTION

IPAD™

MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

The EMIF10-1K010F2 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 flip chip packaging means the package size is equal to the die size. This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15kV.

BENEFITS

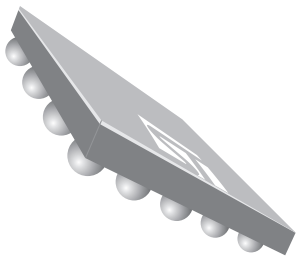
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming: 2.57 mm x 2.57 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

Level 4 15kV (air discharge)
8kV (contact discharge)

MIL STD 883E -Method 3015-6 Class 3



Flip-Chip (24 Bumps)

Table 1: Order Code

Part Number	Marking
EMIF10-1K010F2	FD

Figure 1: Pin Configuration (ball side)

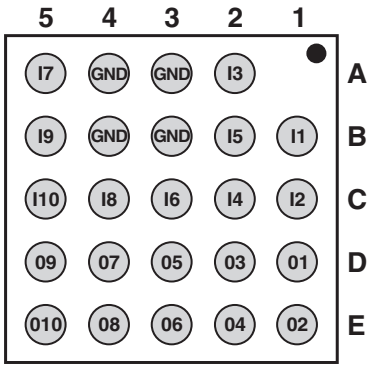


Figure 2: Basic Cell Configuration

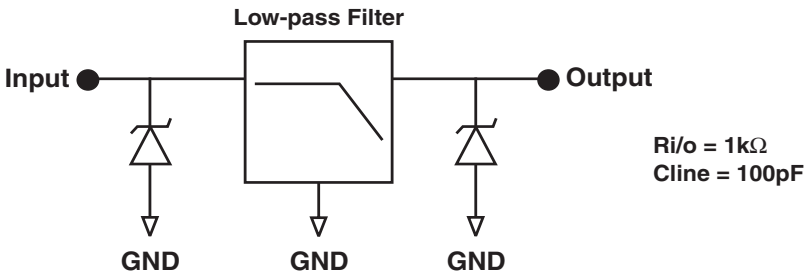


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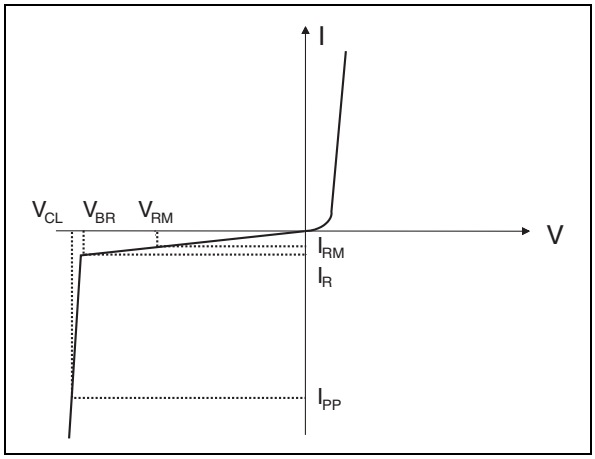
Table 2: Absolute Maximum Ratings (T_{amb} = 25°C)

Symbol	Parameter and test conditions	Value	Unit
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 3: Electrical Characteristics (T_{amb} = 25°C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{in}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3V per line			500	nA
$R_{I/O}$		900	1000	1100	Ω
R_{line}	At 0V bias	80	100	120	pF

Figure 3: S21 (dB) attenuation measurement and Aplac simulation

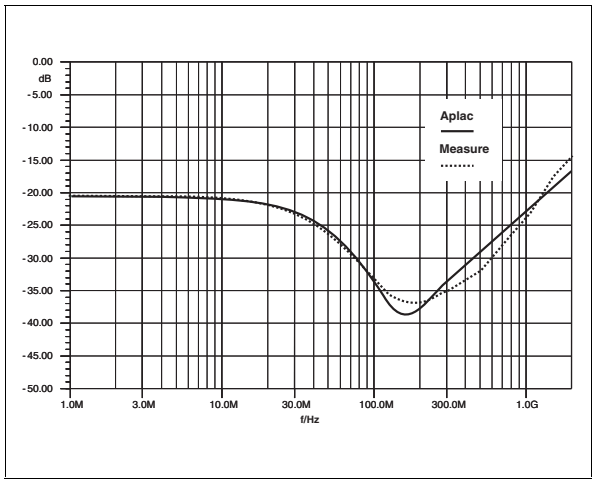


Figure 4: Analog crosstalk measurements

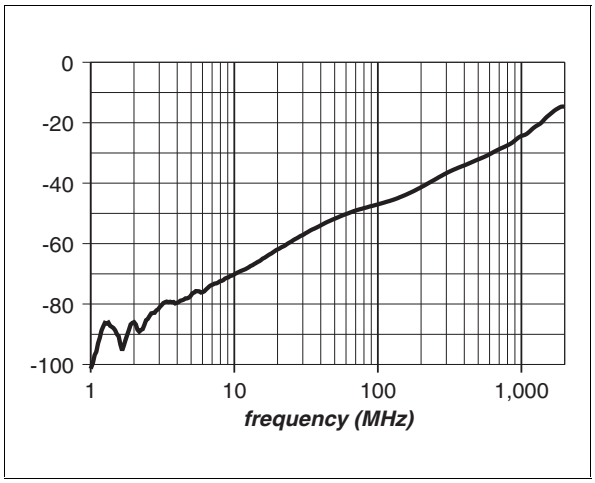


Figure 5: Digital crosstalk measurement

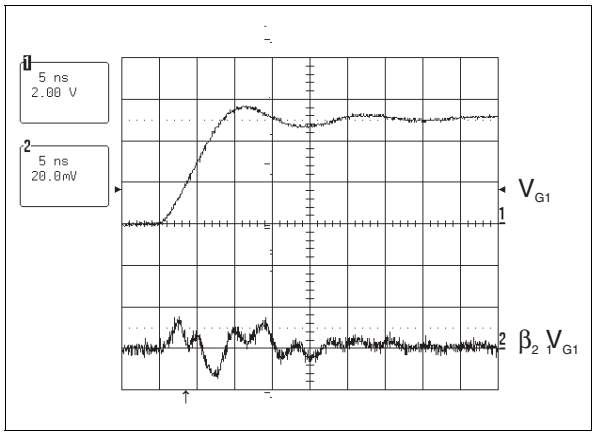


Figure 6: ESD response to IEC61000-4-2 (+15kV air disc.harge) on one input V(in) and on one output (Vout)

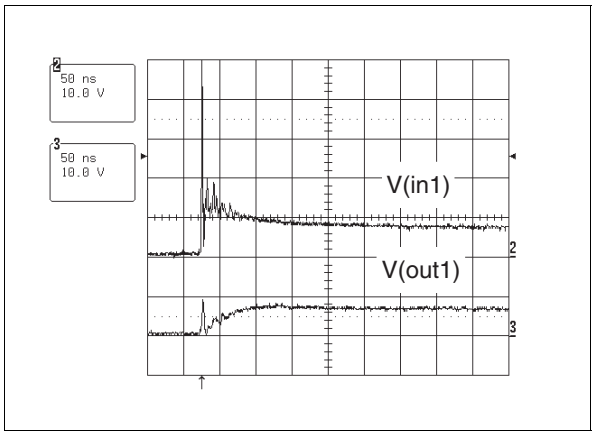


Figure 7: ESD response to IEC61000-4-2 (-15kV air discharge) on one input V(in) and on one output (Vout)

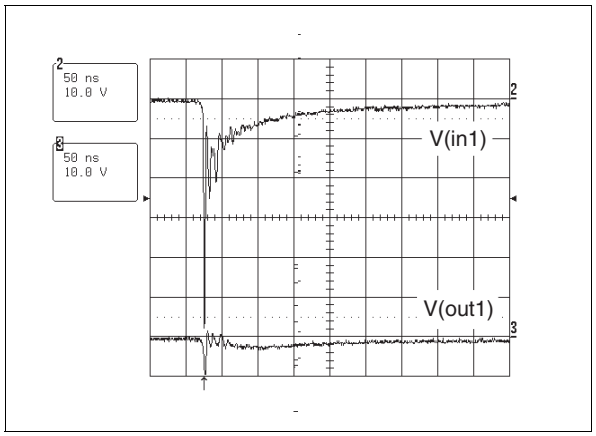


Figure 8: Line capacitance versus applied voltage

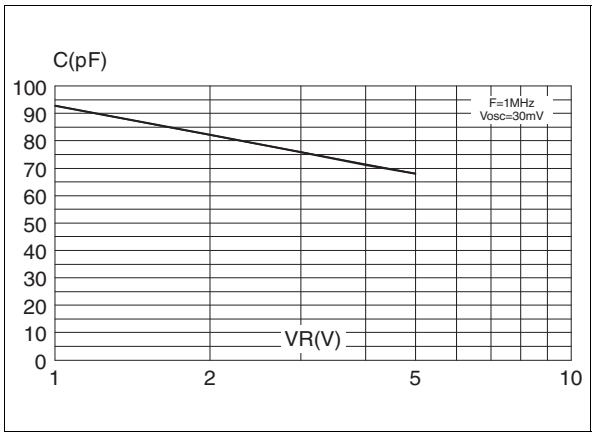


Figure 9: Aplac model single line structure

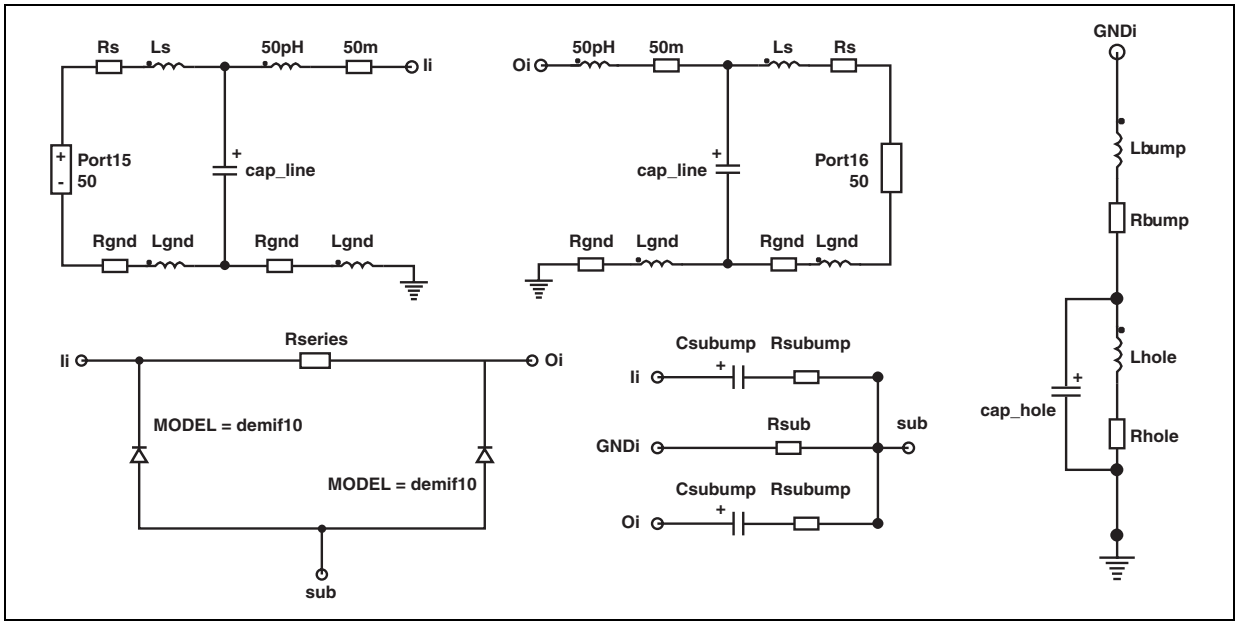


Figure 10: Aplac model parameters

Cz	57pF	Model demif10
Rseries	960	BV = 7
cap_line	0.8pF	IBV = 1m
Ls	0.6nH	CJO = Cz
Rbump	50m	M = 0.3333
Lbump	50pH	Rs = 1
Rs	0.15	VJ = 0.6
Csubump	15pF	TT = 100n
Rsubump	0.15	
Rsub	0.1	
lhole	1.2nH opt	
Rhole	0.15	
cap_hole	0.15pF	
Rgnd	0.25	
lgnd	0.4nH	

Figure 11: Ordering Information Scheme

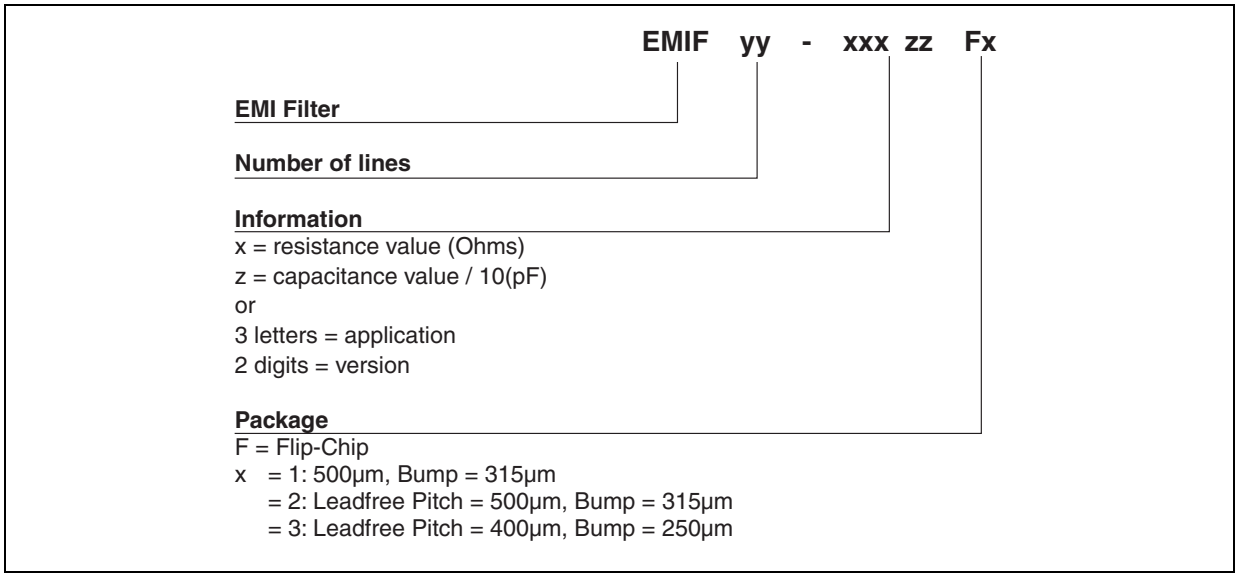


Figure 12: FLIP-CHIP Package Mechanical Data

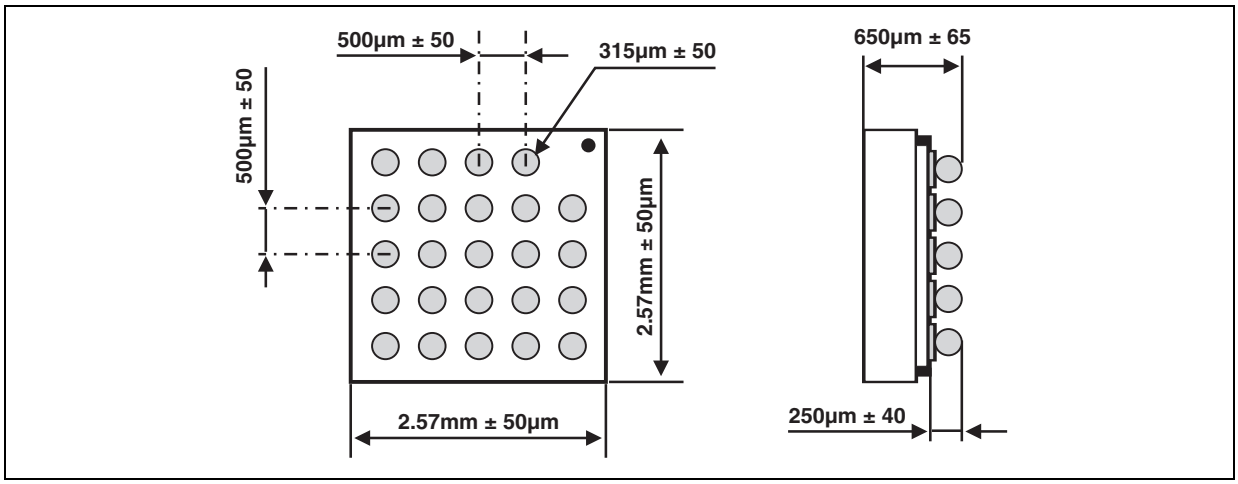


Figure 13: Foot print recommendations

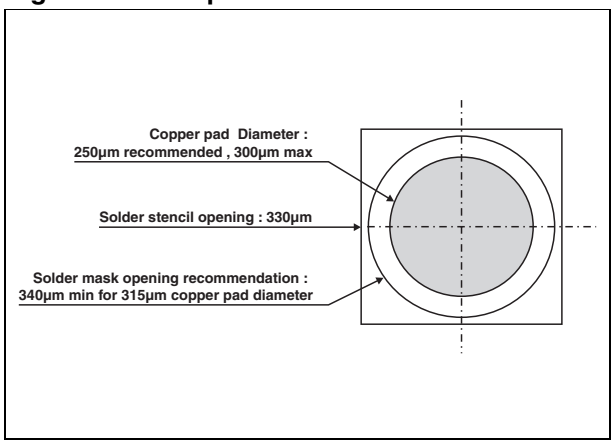


Figure 14: Marking

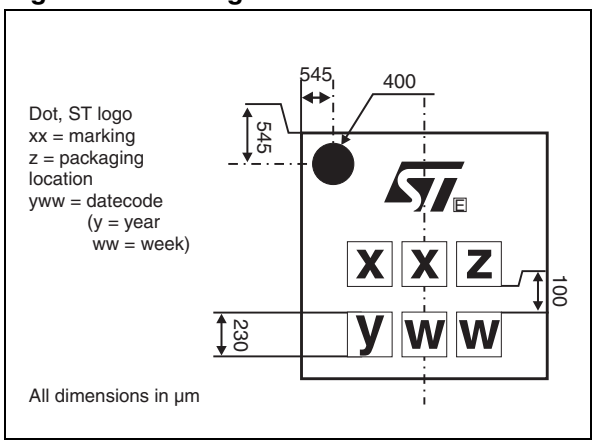


Figure 15: FLIP-CHIP Tape and Reel Specification

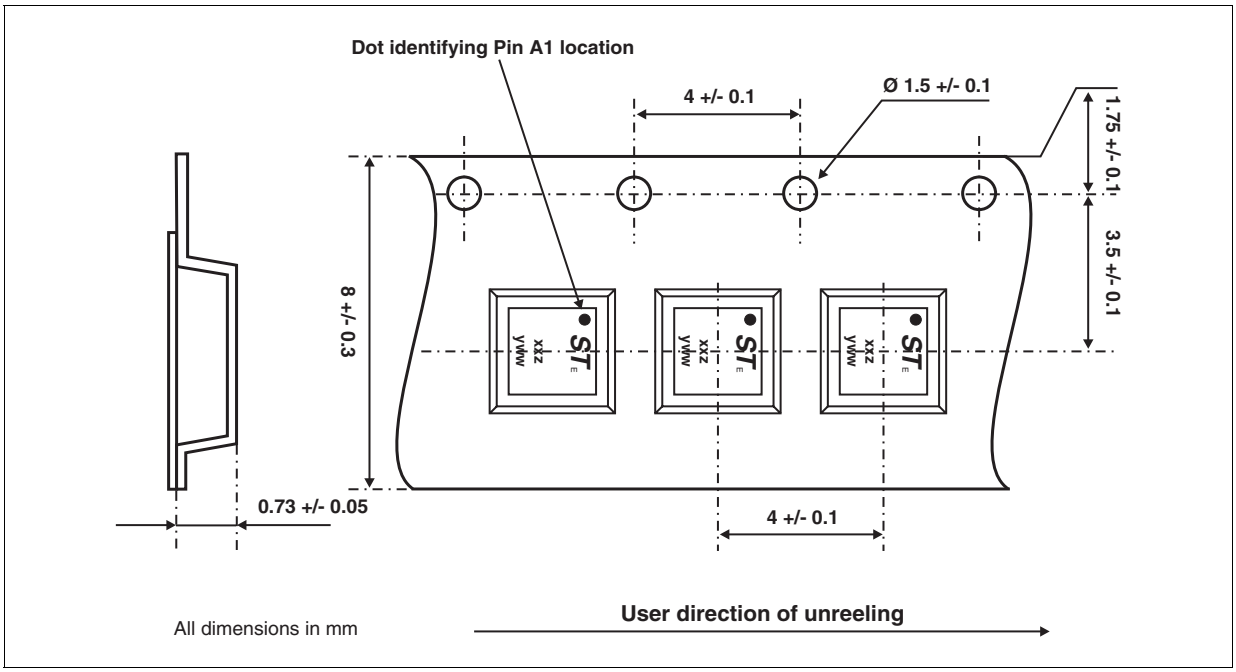


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF010-1K010F2	FD	Flip-Chip	9.2 mg	5000	Tape & reel 7”

Note: More informations are available in the application notes:
AN1235: “Flip-Chip: Package description and recommendations for use”
AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
12-Oct-2004	1	First issue