



EMIF10-COM01

IPAD.™

EMI FILTER INCLUDING ESD PROTECTION

MAIN APPLICATIONS

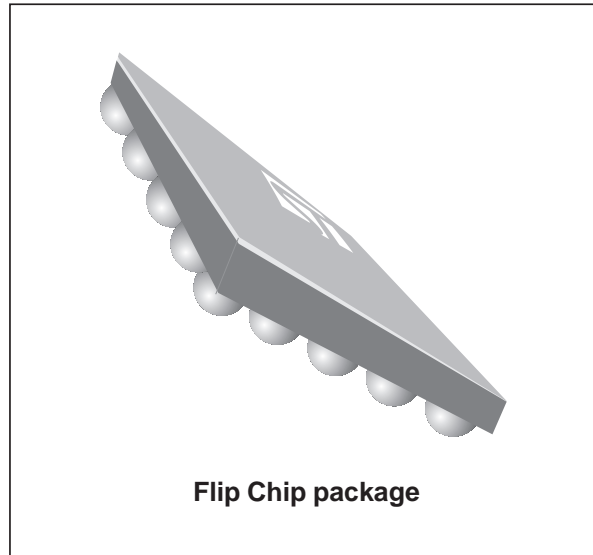
Where EMI filtering in ESD sensitive equipment is required:

- Computers and printers
- Communication systems
- Mobile phones

DESCRIPTION

The EMIF10-COM01 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 flip-chip packaging means the package size is equal to the die size. That's why EMIF10-COM01 is a very small device.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to



Flip Chip package

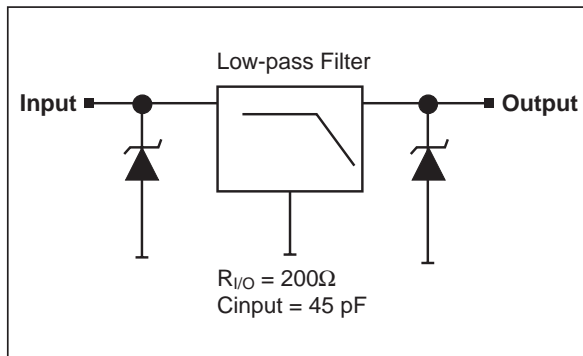
BENEFITS

- EMI symmetrical (I/O) low-pass filter
- Very low PCB space consuming:
2.64 x 2.64 mm²
- Very thin package: 0.63 mm
- High efficiency in ESD suppression on both input & output PINS (IEC61000-4-2 level 4).
- High reliability offered by monolithic integration

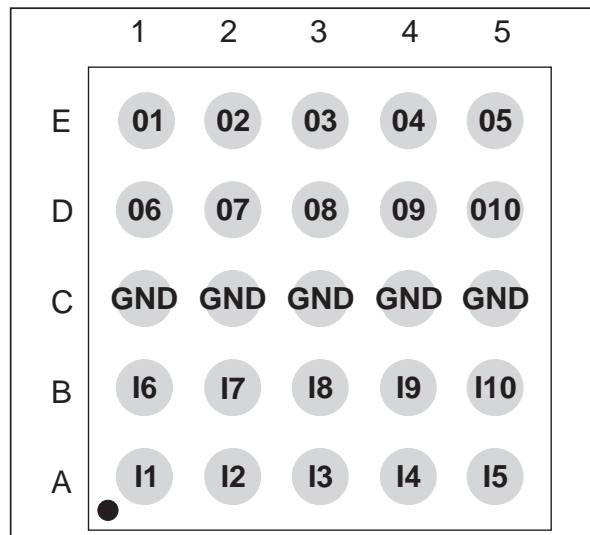
COMPLIES WITH FOLLOWING STANDARD:

IEC61000-4-2 level 4 15 KV (air discharge)
8 kV (contact discharge)

BASIC CELL CONFIGURATION



PIN CONFIGURATION (Ball Side)



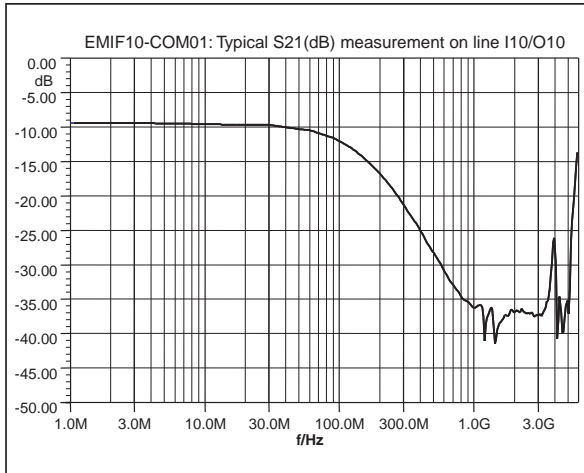
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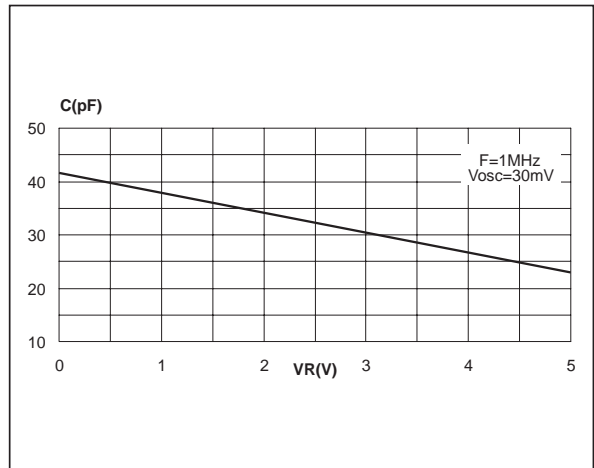
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Filtering Behavior

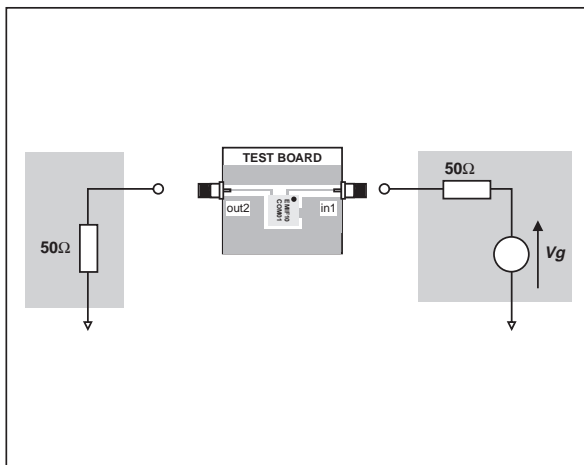


Note: Spikes at high frequencies are induced by the PCB layout

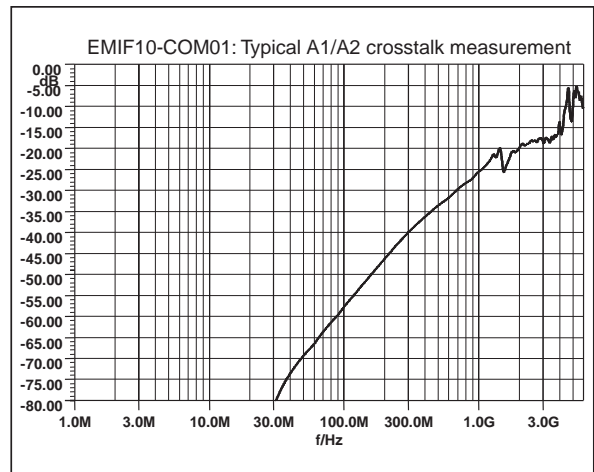
Capacitance versus reverse applied voltage



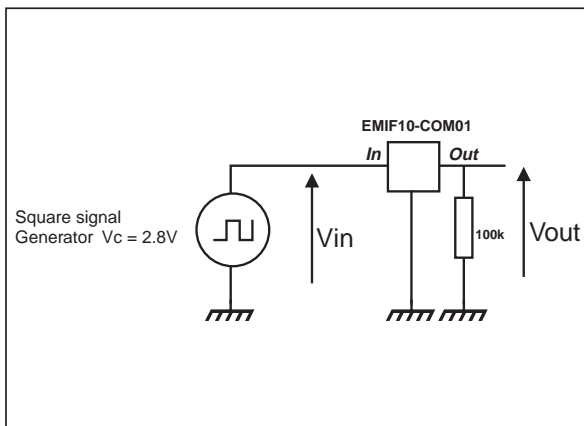
Analog Crosstalk: Measurements



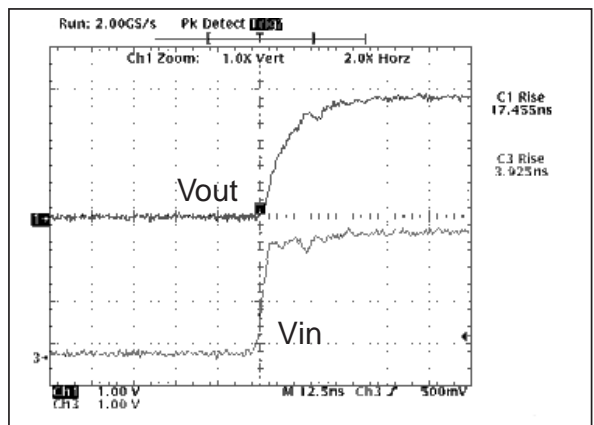
Crosstalk Behavior



Rise Time: Measurement



Rise Time

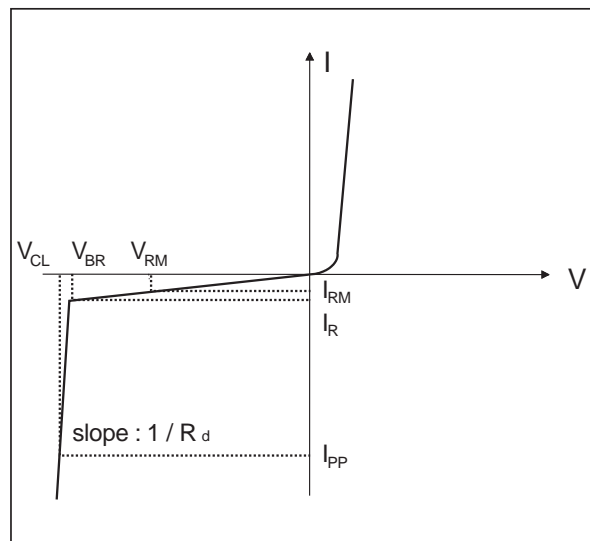


ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharg	15 8	kV
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	-40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$)

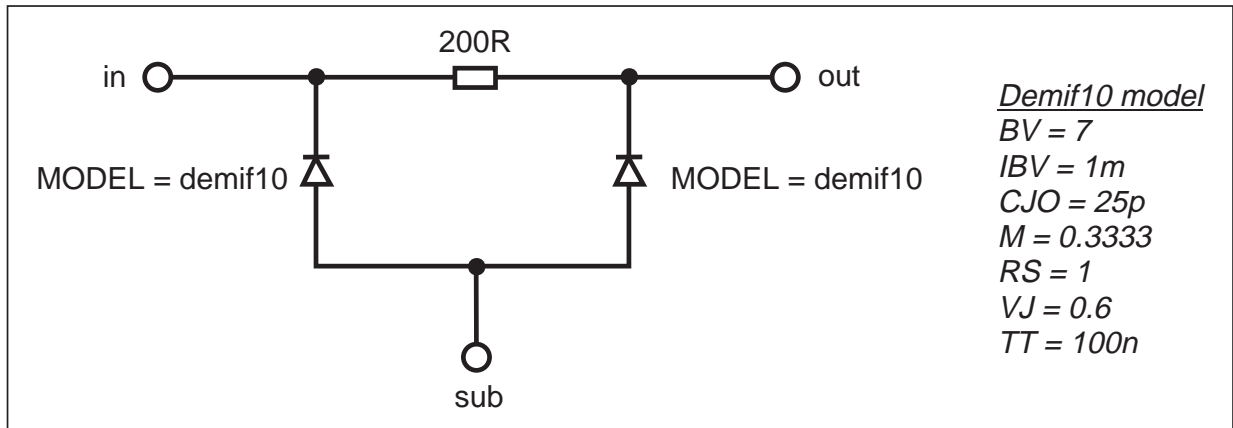
Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{in}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	$I_R = 1\text{mA}$	6	8	10	V
I_{RM}	$V_{RM} = 3\text{V}$ per line			500	nA
R_d	$I_{PP} = 10\text{A}$, $t_p = 2.5\mu\text{s}$ (see note 1)		1		Ω
$R_{I/O}$		180	200	220	Ω
C_{in}	At 0V bias		45	50	pF
t_{LH}	$V_{out} = 2.8\text{V}$ $R_{load} = 100\text{k}\Omega$			25	ns

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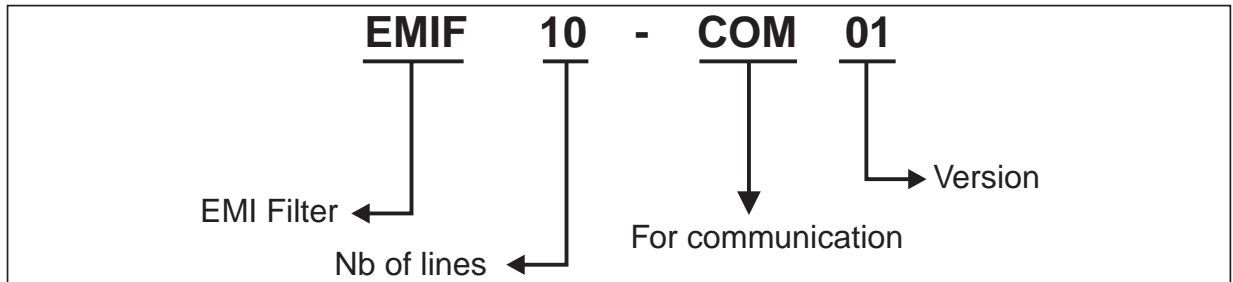
APLAC MODEL



PCB grounding recommendations

In order to ensure a good efficiency in terms of ESD protection and filtering behavior, we recommend to implement microvias (100 µm dia.) between the GND bumps and the GND layer. GND bumps can be connected together in PCB layer 1, and in addition, if possible, use through hole vias (200 µm dia.) in both sides of filter to improve contact to GND (layer). This layout will minimize the distance to the ground and thus parasitic inductances. In addition, we recommend to have GND plane wherever possible.

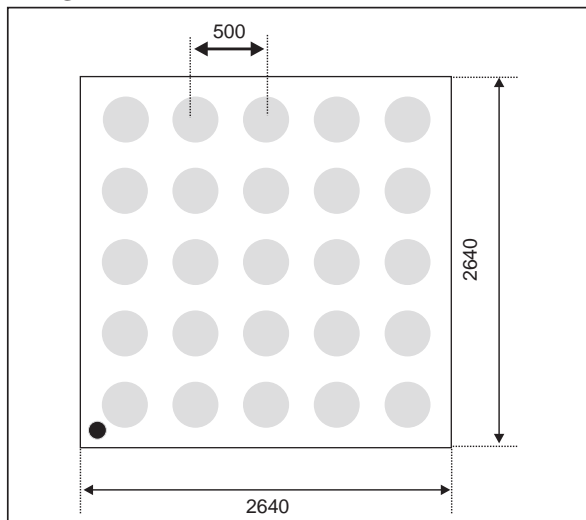
ORDERING CODE



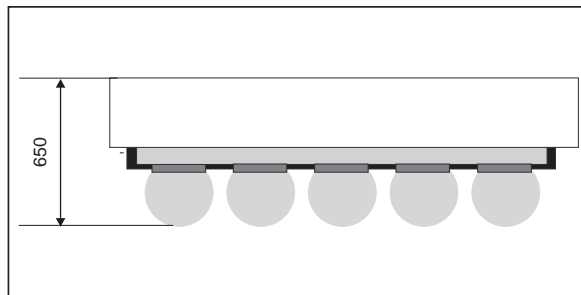
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PACKAGE MECHANICAL DATA

DIE SIZE

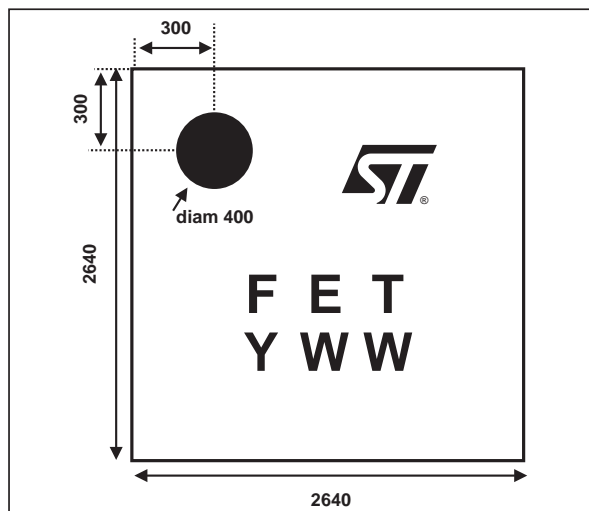


All dimensions in μm



- Die size: $(2640 \pm 50) \times (2640 \pm 50)$
- Die height (including bumps): 650 ± 65
- Bump diameter: 315 ± 50
- Pitch: 500 ± 50
- Weight: 9.3mg

MARKING



- Y W W: Date code

PACKING:

EMIF10-COM01 is delivered in Tape & Reel (7 inches reel); one Tape & Reel contains 5000 dice.

Note: More packing information are available in the application note AN1235: "Flip-Chip package description and recommendations for use"

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