1.5MHz 1A, Synchronous Step-Down Regulator

General Description

EML3020 is a high efficiency step down DC/DC converter with input over voltage protection function. It features an extremely low quiescent current, which is suitable for reducing standby power consumption, especially for portable applications.

The device can accept input voltage from 2.5V to 5.5V and deliver up to 1A output current. High 1.5MHz switching frequency allows the use of small surface mount inductors and capacitors to reduce overall PCB board space. Furthermore, the built-in synchronous switch improves efficiency and eliminates external Schottky diode. EML3020 uses different modulation algorithms for various loading conditions: (1) Pulse Width Modulation (PWM) for low output voltage ripple and fixed frequency noise, (2) Power Saving Modulation (PSM) for improving light load efficiency, and (3) Low Dropout (LDO) Mode for providing 100% duty cycle operation during heavy loading. Adopting low reference voltage design reduces regulated output to 0.6V.

Features

- Achieve 97% efficiency (V_{OUT}=3.3V)
- Input voltage : 2.5V to 5.5V
- Output current up to 1A
- Reference voltage: 0.6V
- Quiescent current 18μ A with no load
- Internal switching frequency: 1.5MHz
- No Schottky diode needed
- Low dropout operation: 100% duty cycle
- Shutdown current < 1μ A
- Excellent line and load transient response
- Over-temperature protection

Applications

- Blue-Tooth devices
- Cellular and Smart Phones
- Personal Multi-media Player (PMP)
- Wireless networking
- Digital Still Cameras
- Portable applications

Typical Application

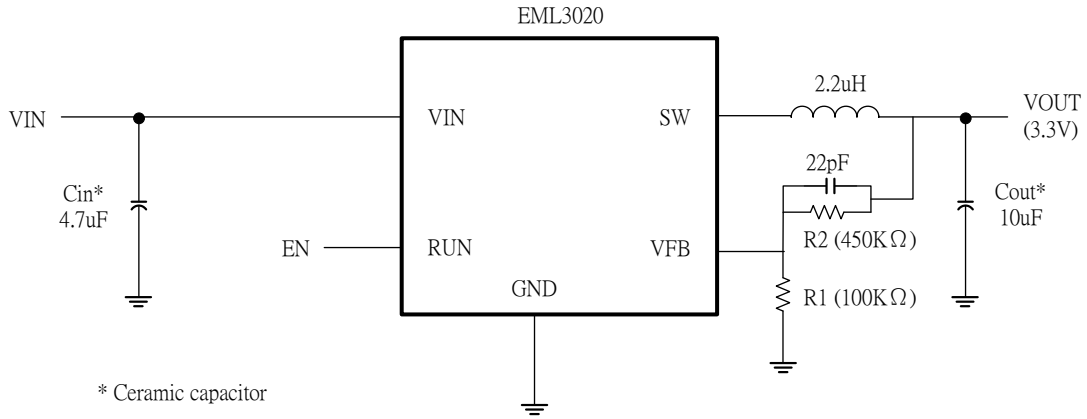
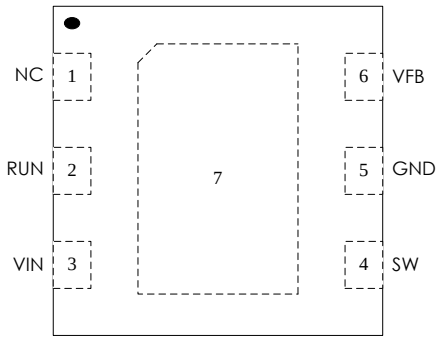


Fig. 1

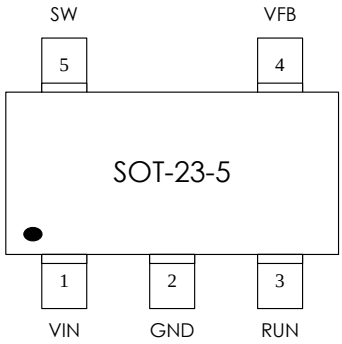
Package Configuration



TDFN-6 (2x2mm)

EML3020-XXFE06NRR

XX	Output Voltage
FE06	TDFN-6 (2x2mm) Package
NRR	RoHS & Halogen free package Commercial Grade Temperature Rating: -40 to 85°C Package in Tape & Reel

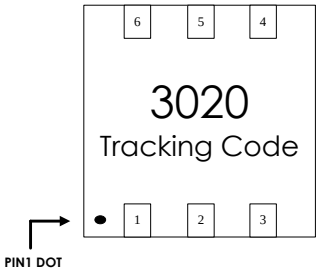
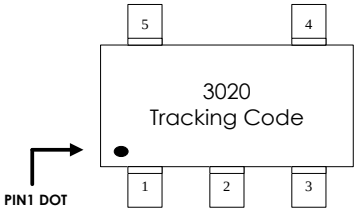


SOT-23-5

EML3020-XXVF05NRR

XX	Output Voltage
VF05	SOT-23-5 Package
NRR	RoHS & Halogen free package Commercial Grade Temperature Rating: -40 to 85°C Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
TDFN-6	Adjustable	EML3020-00FE06NRR		Tape & Reel 3K units
	1.2	EML3020-12FE06NRR		
	3.3	EML3020-33FE06NRR		
SOT-23-5	Adjustable	EML3020-00VF05NRR		Tape & Reel 3K units
	1.2	EML3020-12VF05NRR		
	1.8	EML3020-18VF05NRR		

Pin Functions

Pin Name	TDFN-6	SOT-23-5	Function
NC	**1**	**None**	N.C.
RUN	**2**	**3**	Enable Pin. Minimum 1.2V to enable the device. Maximum 0.4V to shut down the device.
VIN	**3**	**1**	Power Input Pin. Must be closely decoupled to GND pin with a 4.7μF or greater ceramic capacitor.
SW	**4**	**5**	Switch Pin. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
GND	**5**	**2**	Ground Pin.
VFB **(Adjustable)**	**6**	**4**	Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.
VOUT **(Fixed voltage)**			Output Voltage Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.
Exposed pad	**7**	**None**	Connect to GND.

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage ---------- – 0.3V to 6.6V
RUN, VFB Voltages ---------- – 0.3V to V_{IN}
SW Voltage ---------- – 0.3V to (V_{IN} + 0.3V)
Lead Temperature (Soldering, 10 sec)---------- 260°C

Operating Temperature Range ---------- –40°C to 85°C
Junction Temperature (Notes 1, 2) ---------- 150°C
Storage Temperature Range ---------- – 65°C to 150°C
ESD Susceptibility HBM ---------- 2KV
MM ---------- 200V

Thermal data

Package	Thermal resistance	Parameter	Value
TDFN-6 (2x2 mm)	θ JA (Note 3)	Junction-to-ambient	74.7°C/W
	θ JT (Note 4)	Junction-to-top package	24°C/W
SOT-23-5	θ JA (Note 3)	Junction-to-ambient	134.5°C/W
	θ JT (Note 4)	Junction-to-top package	81°C/W

Electrical Characteristics

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} =5.0V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IN}	Input Voltage Range		●	2.5		5.5	V
V_{FB}	Regulated Feedback Voltage		●	0.588	0.600	0.612	V
I_{VFB}	Feedback Current					1	μA
V_{OUT}%	Output Voltage Accuracy	I_{OUT}=100mA, Vin<3.0V		-3		+3	%
		I_{OUT}=100mA, Vin=3.0V to 5.5V	●	-3		+3	%
Δ V_{OUT}	Output Voltage Line Regulation	Vin<3.0V				0.7	%/V
		Vin=3.0V to 5.5V				0.6	%/V
I_{PK}	Peak Inductor Current	V_{FB} = 0.5V or V_{OUT} = 90%,		1.5	2.3		A
I_q	PFM Quiescent Current	V_{FB} = 0.65V or V_{OUT} = 108%			18		μA
	Shutdown	V_{RUN} = 0V, V_{IN} = 4.2V			0.1	1	μA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V or V_{OUT} = 100%		1.2	1.5	1.8	MHz
	Short-Circuit Oscillator Frequency	V_{FB} = 0V or V_{OUT} = 0V			750		kHz
R_{PFET}	$R_{DS(ON)}$ of PMOS	I_{SW} = 100mA			0.24		Ω
R_{NFET}	$R_{DS(ON)}$ of NMOS	I_{SW} = –100mA			0.24		Ω
V_{UVLO}	VIN UVLO Threshold				1.8		V
	VIN UVLO Hysteresis				50		mV
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V				1	μA
V_{RUN}	Enable Threshold		●	1.2			V
	Shutdown Threshold		●			0.4	V
I_{RUN}	RUN Leakage Current					1	μA
T_{SD}	Thermal Shutdown				170		℃
	Thermal Shutdown Hysteresis				30		℃

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D) * \theta_{JA}$.

Note 2: This IC has a built-in over-temperature protection to avoid damage from overloaded conditions.

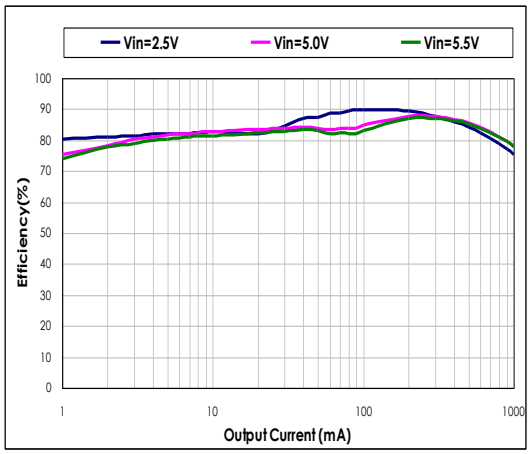
Note 3: θ_{JA} is measured in the natural convection at T_A=25℃ on a highly effective thermal conductivity test board (2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.

Note 4: θ_{JT} represents the heat resistance between the chip and the package top surface.

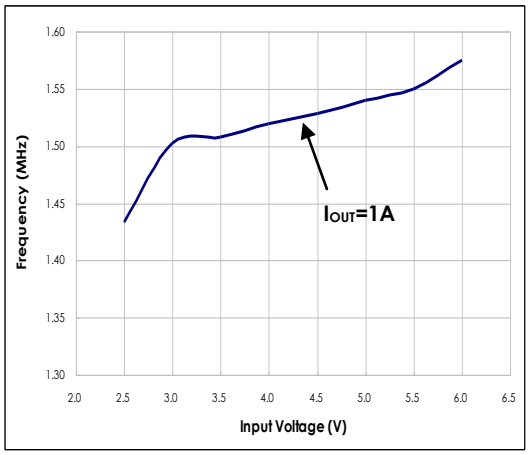
Typical Performance Characteristics

V_{IN}=5.0V, V_{OUT}=1.2V, C_{IN}=4.7uF, C_{OUT}=10uF, L=2.2uH, T_A=25℃, unless otherwise specified

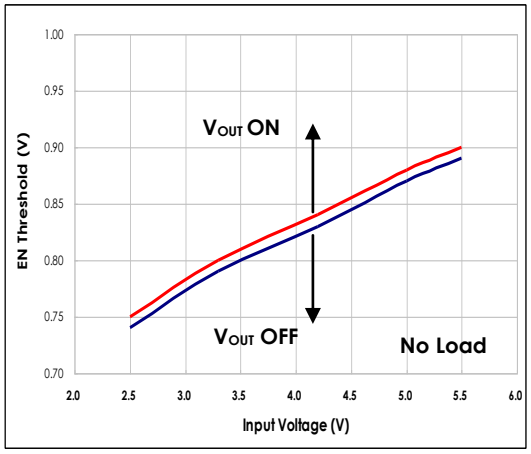
Efficiency vs. Output Current (V_{OUT}=1.2V)



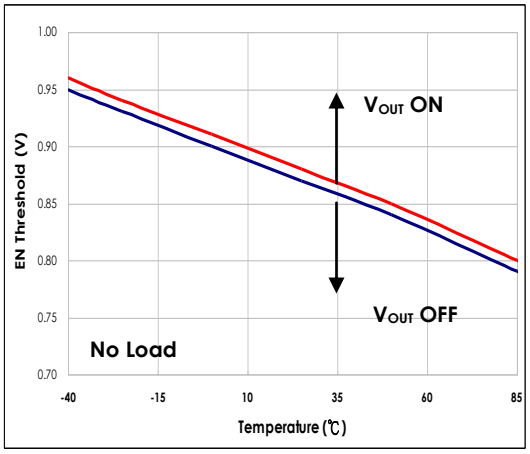
Oscillator Frequency vs. Input Voltage



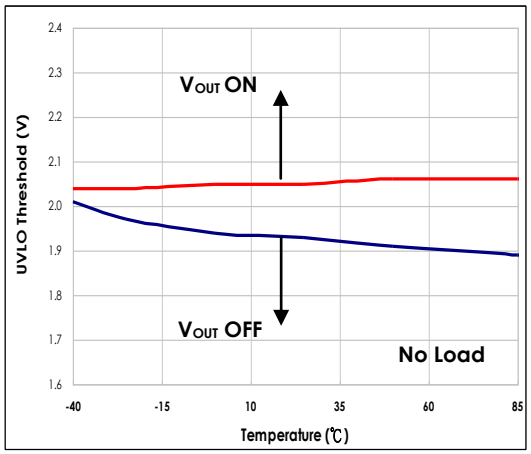
Run Pin Threshold vs. Input Voltage



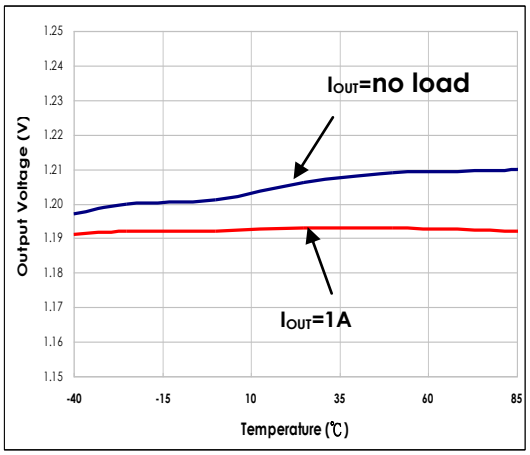
Run Pin Threshold vs. Temperature



UVLO Threshold vs. Temperature



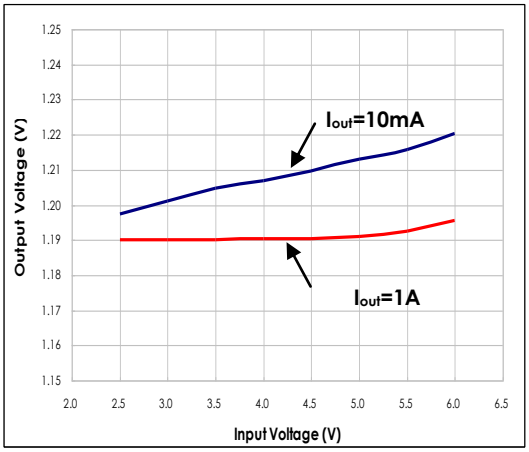
Output Voltage vs. Temperature



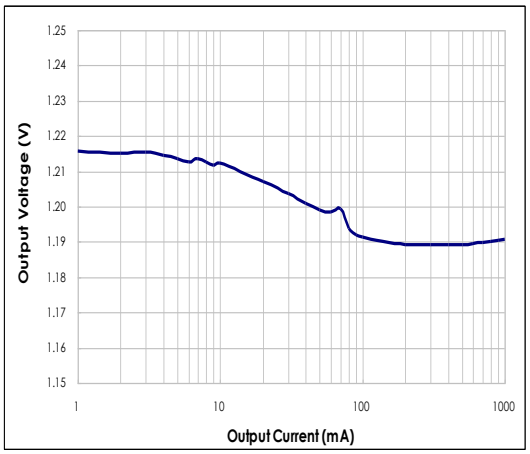
Typical Performance Characteristics

V_{IN}=5.0V, V_{OUT}=1.2V, C_{IN}=4.7uF, C_{OUT}=10uF, L=2.2uH, T_A=25℃, unless otherwise specified

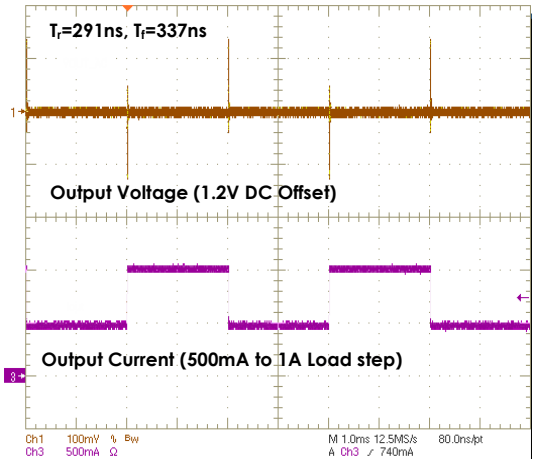
Line Regulation



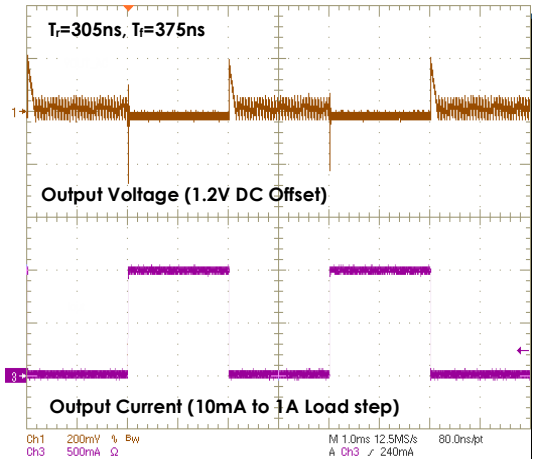
Load Regulation



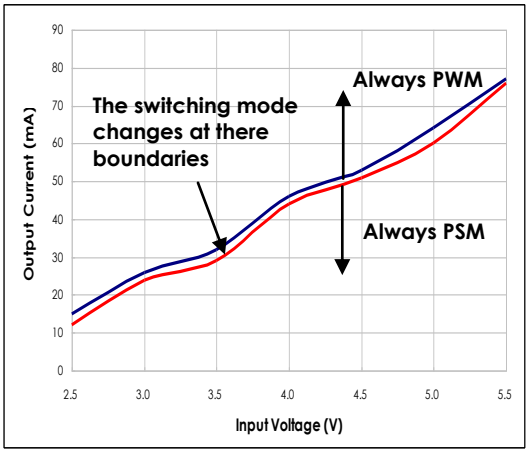
Load Transient Response



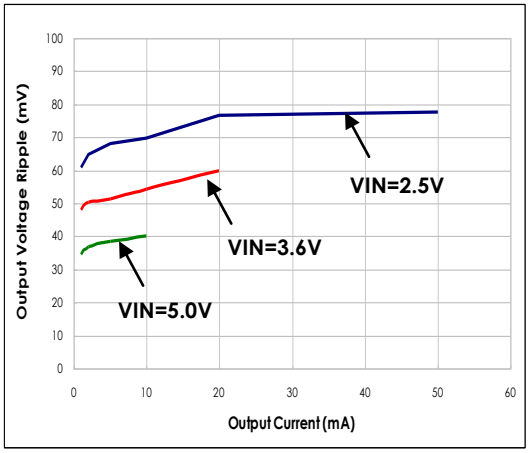
Load Transient Response



PSM/PWM Boundaries



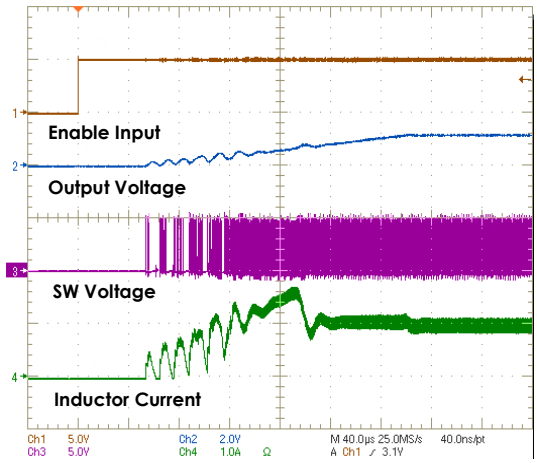
Output Voltage Ripple



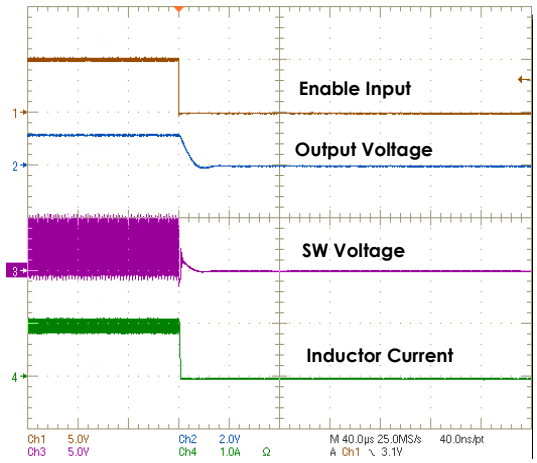
Typical Performance Characteristics

V_{IN}=5.0V, V_{OUT}=1.2V, C_{IN}=4.7uF, C_{OUT}=10uF, L=2.2uH, T_A=25℃, unless otherwise specified

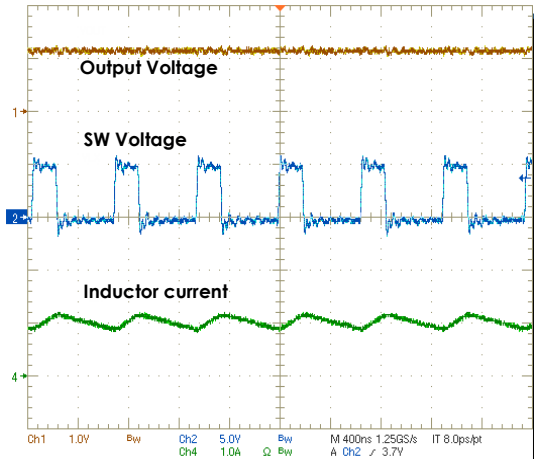
Power-ON from Run Pin (I_{OUT}=1A)



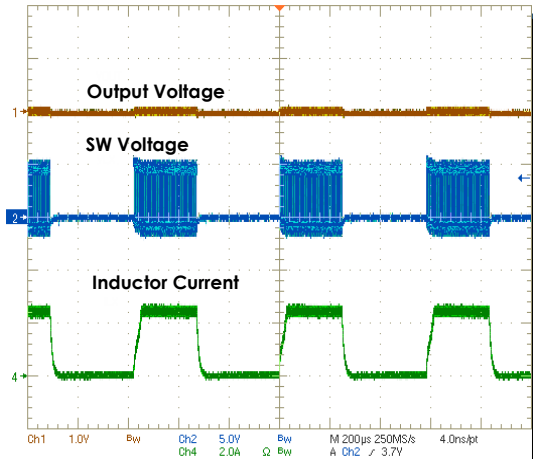
Power-OFF from Run Pin (I_{OUT}=1A)



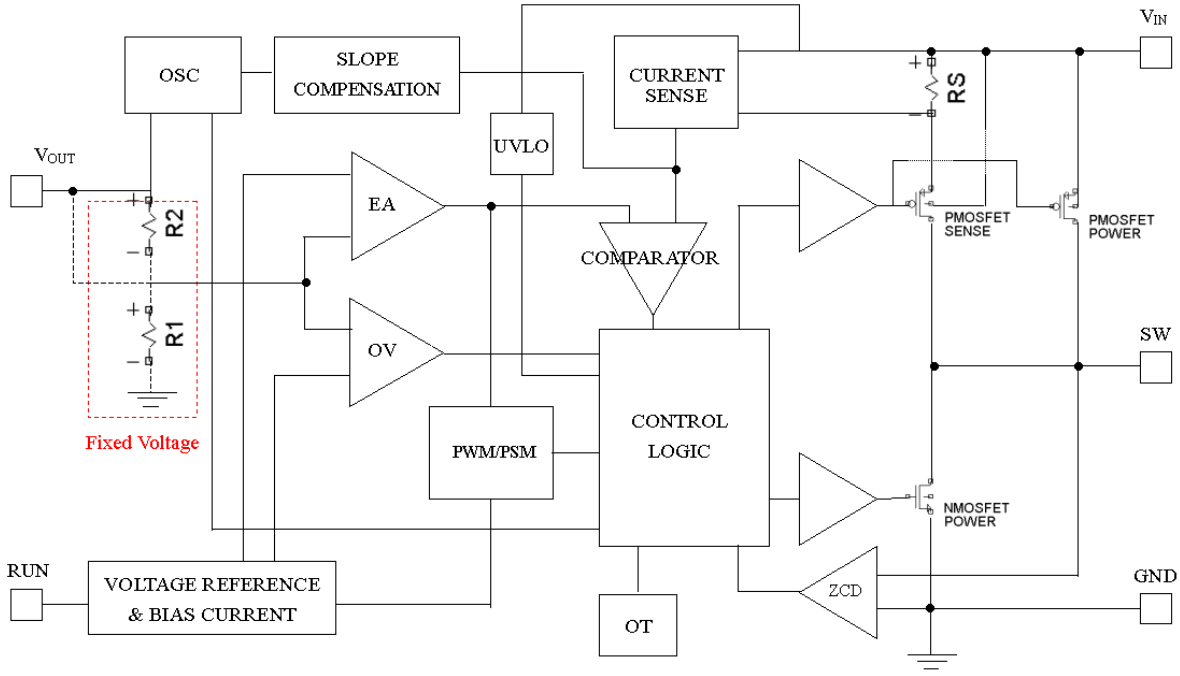
PWM Operation



Short Circuit Response



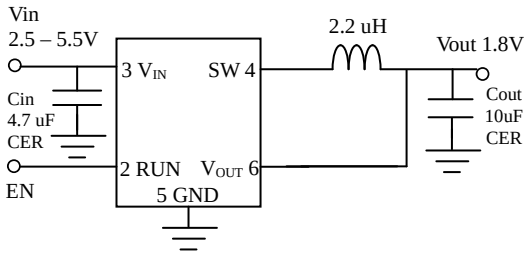
Functional Block Diagram



Applications

The typical application circuit of adjustable version is shown in Fig.1.

Fixed voltage version is shown below:



Inductor Selection

Inductor ripple current and core saturation current are the two main factors that decide the Inductor value. A low DCR inductor is preferred.

C_{IN} and C_{OUT} Selection

A low ESR input capacitor can prevent large voltage transients at V_{IN}. The RMS current of input capacitor is required larger than I_{RMS} calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{Eq. 1}$$

ESR is an important parameter to select C_{OUT}, which can be seen in the following output ripple V_{OUT} equation:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right) \quad \text{Eq. 2}$$

Cheaper and smaller ceramic capacitors with higher capacitance values are now commercially available. These ceramic capacitors have low ripple currents, high voltage ratings and low ESR which make them suitable for switching regulator applications. It is feasible to optimize very low output ripples by Cout since Cout does not affect the internal control loop stability. X5R or X7R types are recommended since they have the best temperature and voltage characteristics of all ceramics capacitors.

Output Voltage (EML3020 adjustable)

In the adjustable version, the output voltage can be determined by:

$$V_{OUT} = 0.6\,V \left(1 + \frac{R_2}{R_1} \right) \quad \text{Eq. 3}$$

Thermal Considerations

Although the thermal shutdown circuit is designed in EML3020 to protect the device from thermal damage, the total power dissipation that EML3020 can sustain depends on the thermal capability of the package. The formula to ensure the safe operation is shown in note 1 on page 3.

To avoid the EML3020 from exceeding the maximum junction temperature, the user should perform some thermal analysis during PCB design.

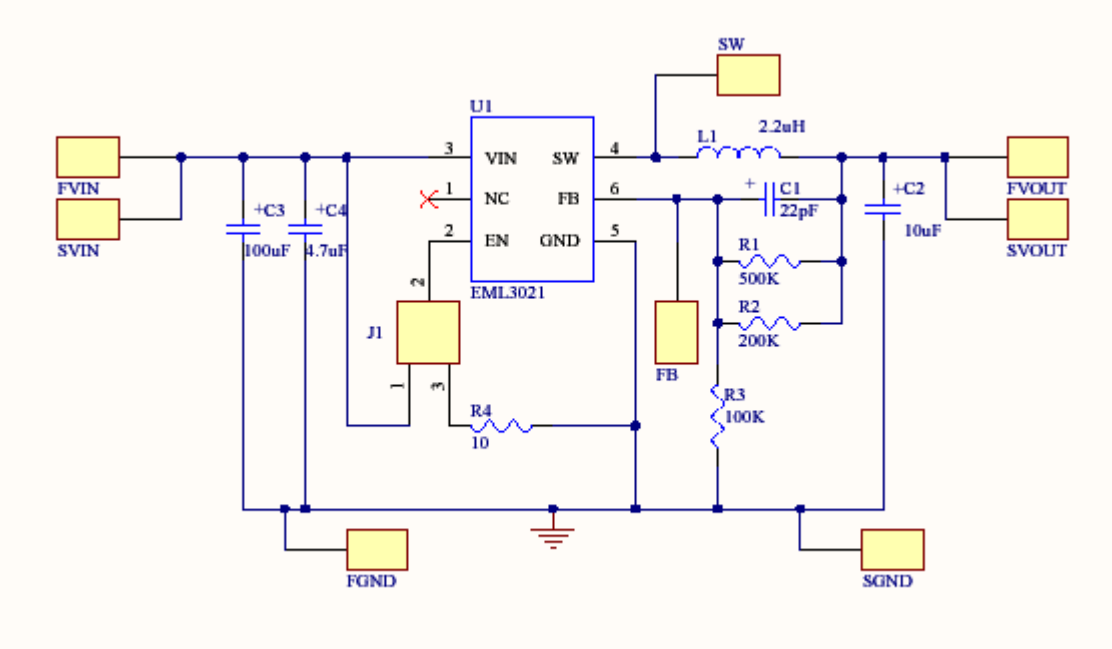
Guidelines for PCB Layout

To ensure proper operation of the EML3020, please note the following PCB layout guidelines:

1. The GND, SW and the VIN trace should be kept short, direct and wide.
2. V_{OUT} pin must be connected to output capacitor C_{OUT} directly.
3. The Input capacitor C_{IN} must be connected to the pin V_{IN} as close as possible.
4. Keep SW node away from the sensitive VFB node since this node has high frequency and voltage swing.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

Applications

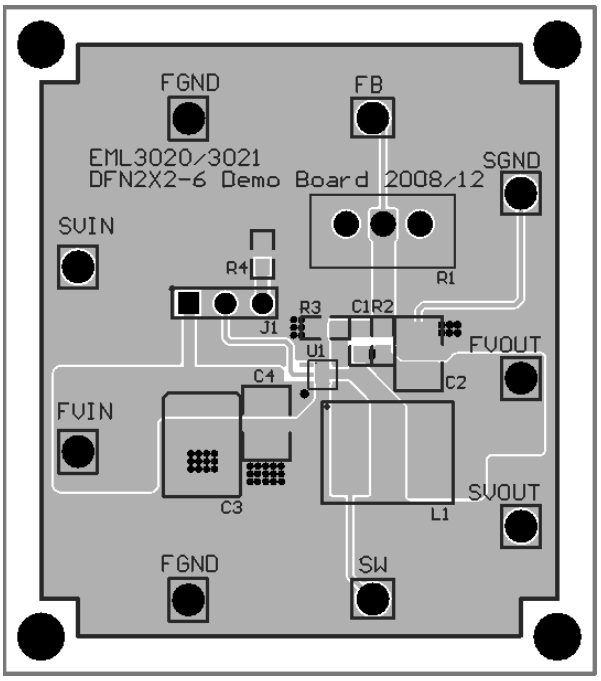
Typical schematic for PCB layout



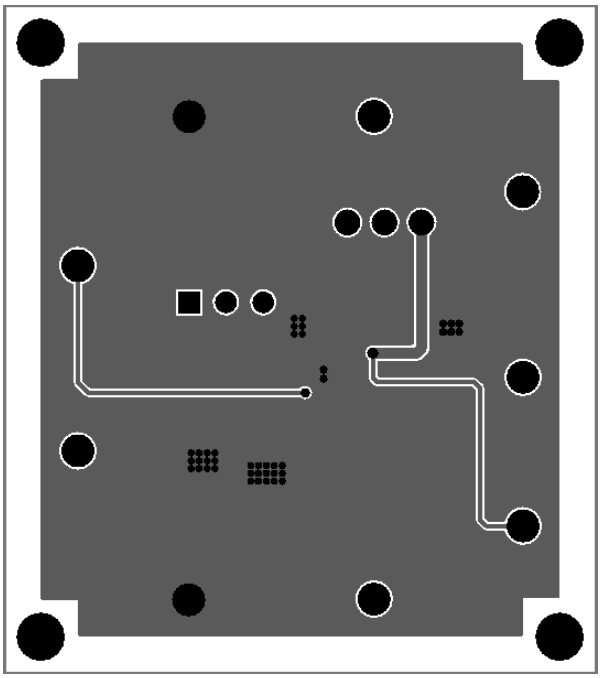
Note.

R2 and C3 are reserved locations for testing purposes. They are removed during normal applications.

Typical schematic for PCB layout (cont.)

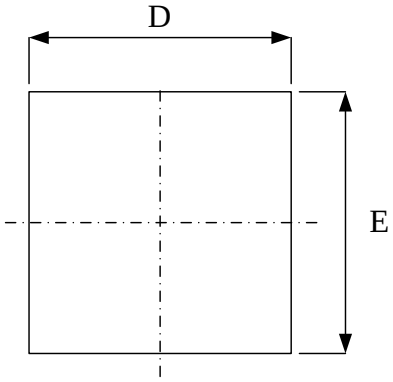


Top Layer

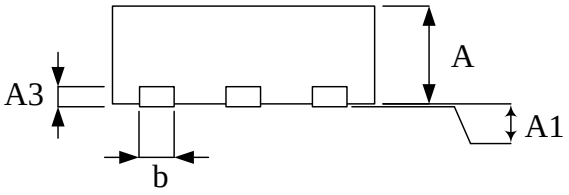


Bottom Layer

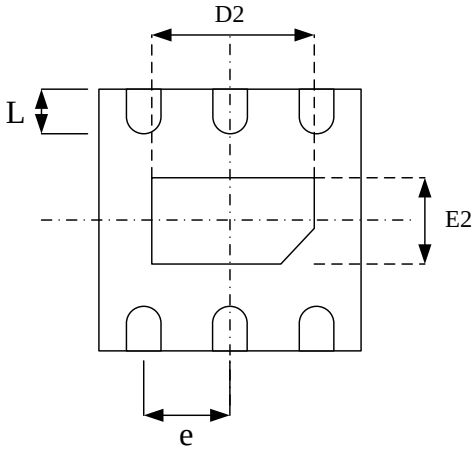
Package Outline Drawing
TDFN-6L (2x2 mm)



TOP VIEW



SIDE VIEW



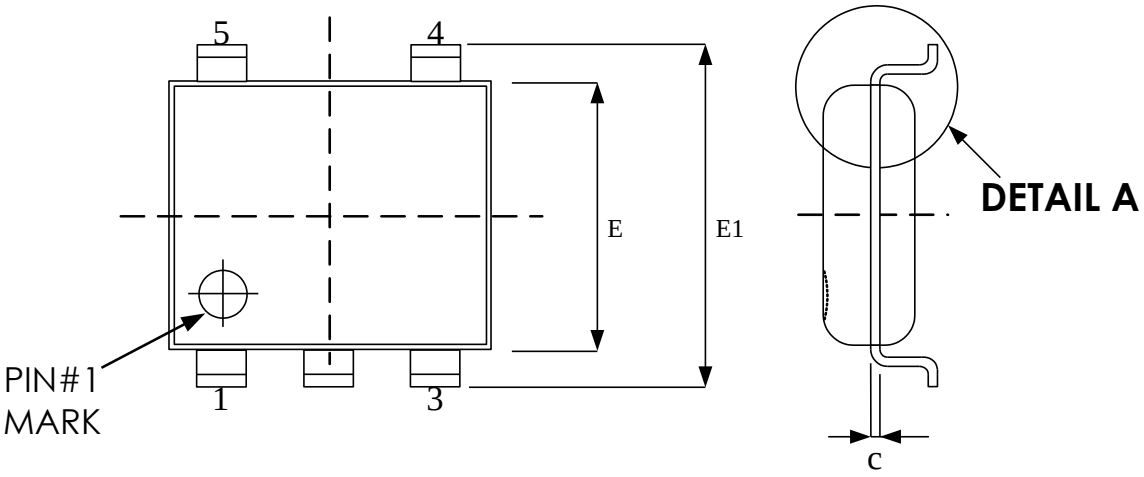
BOTTOM VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.18	0.25
b	0.25	0.35
D	1.95	2.05
E	1.95	2.05
e	0.65 BSC	
L	0.20	0.45

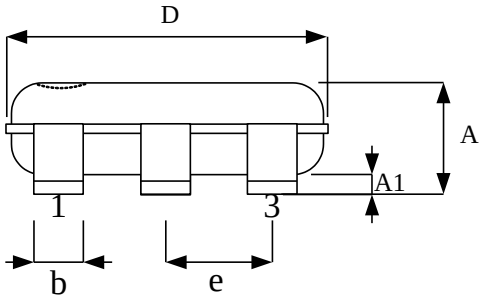
Exposed pad option

	Dimension in mm	
	Min	Max
D2	1.50	1.65
E2	0.90	1.05

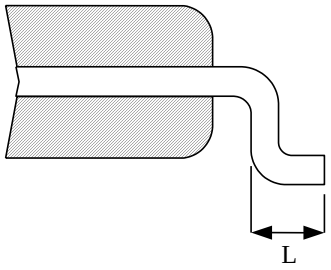
Package Outline Drawing
SOT-23-5



TOP VIEW



SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

Revision History

Revision	Date	Description
0.1	2009.05.14	Original.
0.2	2010.01.13	1. Modify DFN2x2-6 Thermo data. 2. Added SOT-23-5 package type.
0.3	2010.03.18	Revise Packing Tape & Reel number.
1.0	2010.07.28	The content wording revised on page 9.
1.1	2011.01.06	The content wording revised on page 4.
1.2	2011.08.11	Revise TDFN-6 and SOT23-5 outline spec
1.3	2015.12.09	1. Added the VIN UVLO Threshold & Hysteresis. 2. Added the Thermal shutdown & Hysteresis.
1.4	2018.04.17	1.Add 1.2V/3.3 voltage option for TDFN-6 2.Add 1.2V/1.8 voltage option for SOT23-5

Important Notice

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