Dual Channel 1A, Synchronous Step-Down Regulator

General Description

EML3022 is designed with high efficiency step down DC/DC converter and supports dual channel for portable devices applications. It features with extreme low quiescent current with no load which is the best fit for extending battery life during the standby mode.

The device operates from 2.5V to 5.5V input voltage and up to 1A output current capability. High 1.5MHz internal frequency makes small surface mount inductors and capacitors possible and reduces overall PCB board space. Further, build-in synchronous switch makes external Schottky diode is no longer needed and efficiency is improved. EML3022 is designed base on Pulse Width Modulation (PWM) for low output voltage ripple and fixed frequency noise, while Pulse Frequency Modulation (PFM) is used to improve light load efficiency, and Low Dropout (LDO) Mode provides 100% duty cycle operation. Low reference voltage is designed for achieving regulated output down to 0.6V.

The device is available in an adjustable version in E-SOP-8L package.

Features

- Achieve 97% efficiency
- Input Voltage : 2.5V to 5.5V
- Output Current up to 1A
- Reference voltage 0.6V
- Quiescent Current 30μ A with No Load
- Internal switching frequency 1.5MHz
- No Schottky Diode needed
- Low Dropout Operation: 100% Duty Cycle
- Shutdown current < 1μ A
- Excellent Line and Load Transient Response
- Over-temperature Protection

Applications

- Blue-Tooth devices
- Cellular and Smart Phones
- Personal multi-media Player (PMP)
- Wireless networking
- Digital Still Cameras
- Portable applications

Typical Application

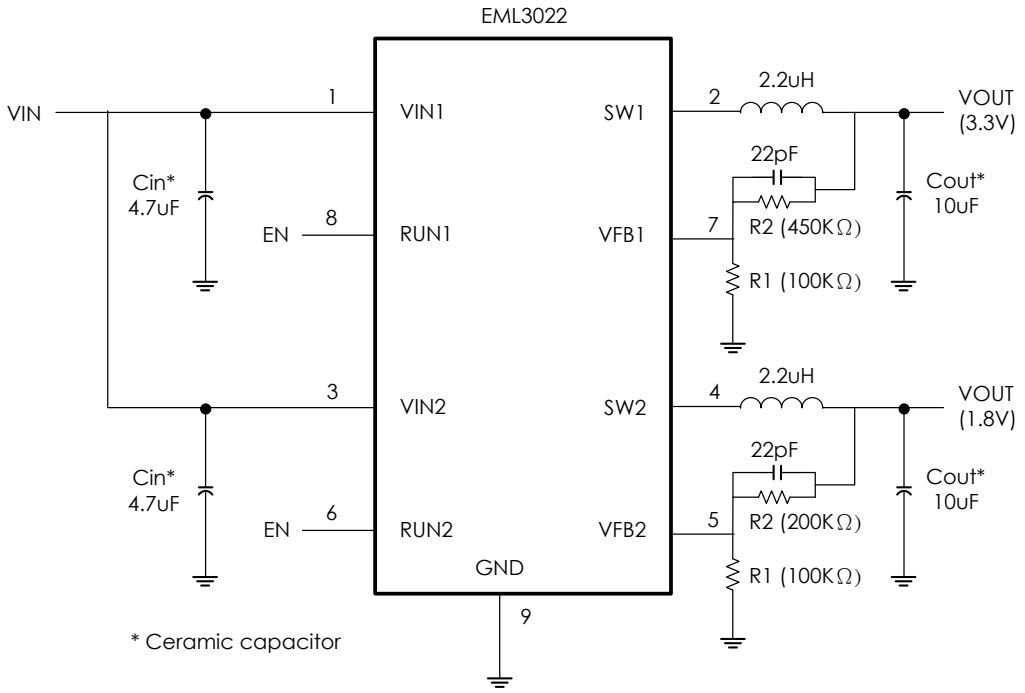
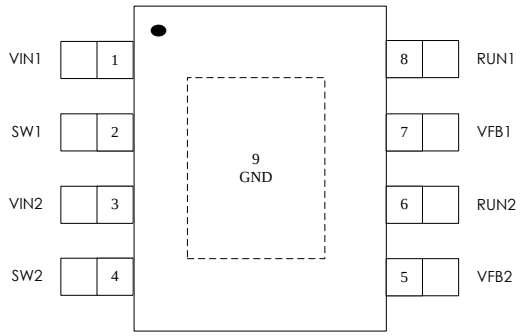


Fig. 1

Package Configuration



E-SOP-8L

EML3022-00SE08NRR

00 Adjustable

SE08 E-SOP-8L Package

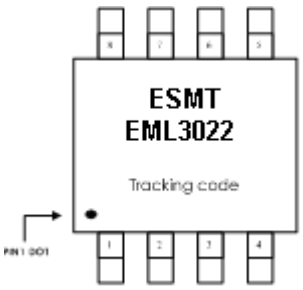
NRR RoHS & Halogen free package

Commercial Grade Temperature

Rating: -40 to 85°C

Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
E-SOP-8L	adjustable	EML3022-00SE08NRR		Tape & Reel 3K units

Pin Functions

Pin Name	E-SOP-8L	Function
VIN1	**1**	Power Input Pin. Must be closely decoupled to GND pin with a 4.7μF or greater ceramic capacitor.
SW1	**2**	Switch Pin. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
VIN2	**3**	Power Input Pin. Must be closely decoupled to GND pin with a 4.7μF or greater ceramic capacitor.
SW2	**4**	Switch Pin. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
VFB2 **(Adjustable)**	**5**	Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.
VOUT2 **(Fixed voltage)**		Output Voltage Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.
RUN2	**6**	Enable Pin. Minimum 1.2V to enable the device. Maximum 0.4V to shut down the device.
VFB1 **(Adjustable)**	**7**	Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.
VOUT1 **(Fixed voltage)**		Output Voltage Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.
RUN1	**8**	Enable Pin. Minimum 1.2V to enable the device. Maximum 0.4V to shut down the device.
GND **(Exposed pad)**	**9**	Connect to GND.

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage ---------- – 0.3V to 6V
EN, V_{FB} Voltages ---------- – 0.3V to V_{IN}
SW Voltage ---------- – 0.3V to (V_{IN} + 0.3V)
Lead Temperature (Soldering, 10 sec)---------- 260°C

Operating Temperature Range ---------- –40°C to 85°C
Junction Temperature (Notes 1, 3) ---------- 150°C
Storage Temperature Range ---------- – 65°C to 150°C
ESD Susceptibility HBM ---------- 2KV
MM ---------- 200V

Thermal data

Package	Thermal resistance	Parameter	Value
E-SOP-8L	θ JA (Note 4)	Junction-ambient	42°C/W
	θ JC (Note 5)	Junction-case	10°C/W

Electrical Characteristics

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.6V unless otherwise specified.

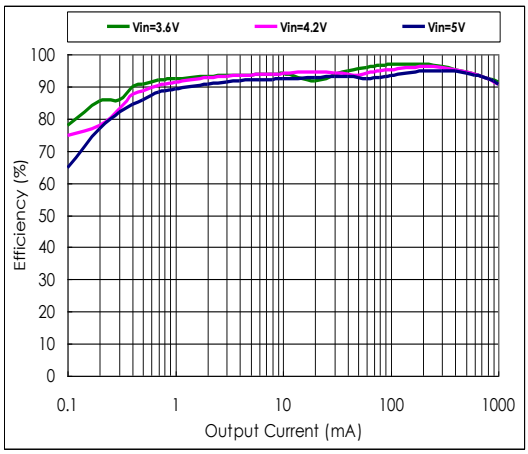
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IN}	Input Voltage Range			2.5		5.5	V
I_{VFB}	Feedback Current					±100	nA
V_{FB}	Regulated Feedback Voltage			0.588	0.600	0.612	V
V_{OUT}%	Output Voltage Accuracy	I_{OUT}=100mA	●	-3		+3	%
Δ V_{FB}	Reference Voltage Line Regulation	V_{IN} = 3.0V to 5.5V	●			0.6	%/V
Δ V_{OUT}	Output Voltage Line Regulation	V_{IN} = 3.0V to 5.5V	●			0.6	%/V
I_{PK}	Peak Inductor Current	V_{FB} = 0.5V or V_{OUT} = 90%,		1.5	2.3		A
I_S	PWM Quiescent Current (Note 2)	V_{FB} = 0.5V or V_{OUT} = 90%, dual channel			376		μ A
	PFM Quiescent Current	V_{FB} = 0.65V or V_{OUT} = 108%, dual channel			30		μ A
	Shutdown	V_{RUN} = 0V, V_{IN} = 4.2V, dual channel			0.1	1	μ A
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V or V_{OUT} = 100%	●	1.2	1.5	1.8	MHz
	Short-Circuit Oscillator Frequency	V_{FB} = 0V or V_{OUT} = 0V	●		900		kHz
R_{PFET}	$R_{DS(ON)}$ of PMOS	I_{SW} = 100mA			0.24		Ω
R_{NFET}	$R_{DS(ON)}$ of NMOS	I_{SW} = –100mA			0.21		Ω
V_{UVLO}	Under Voltage Lock Out				1.8		V
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V				±1	μ A
V_{RUN}	Enable Threshold		●			1.2	V
	Shutdown Threshold		●	0.4			V
I_{RUN}	RUN Leakage Current		●			±1	μ A

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D)(165°C/W)$)
Note 2: Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.
Note 3: This IC is build-in over-temperature protection to avoid damage from overload conditions.
Note 4: θ JA is measured in the natural convection at TA=25℃ on a high effective thermal conductivity test board (4 layers , 2S2P) of JEDEC 51-5 thermal measurement standard.
Note 5: θ JC represents the resistance to the heat flows the chip to package top case.

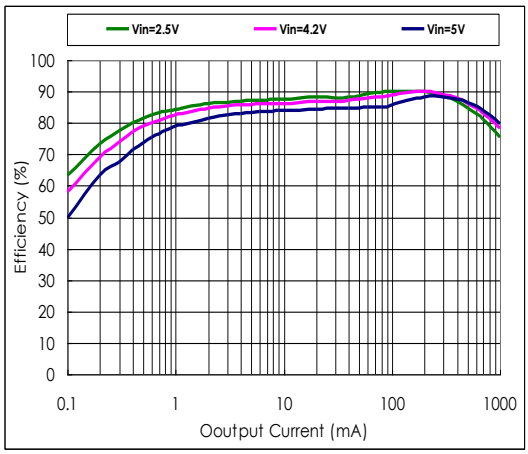
Typical Performance Characteristics

VIN=3.6V, T_A=25℃, unless otherwise specified

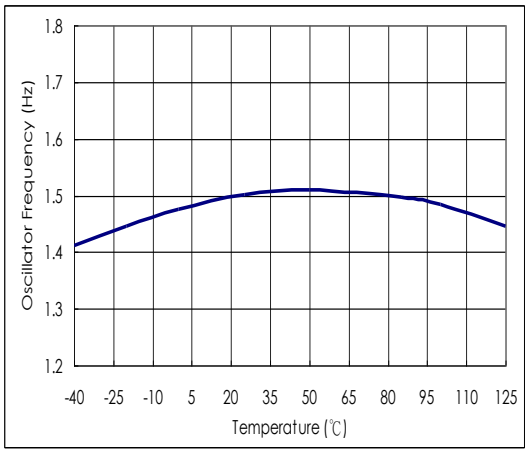
Efficiency vs Output Current (VOUT=3.3V)



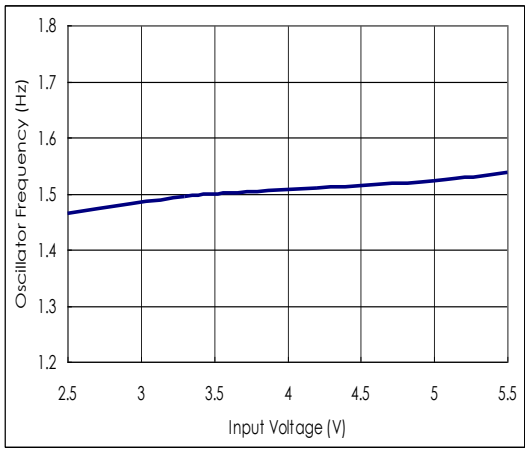
Efficiency vs Output Current (VOUT=1.2V)



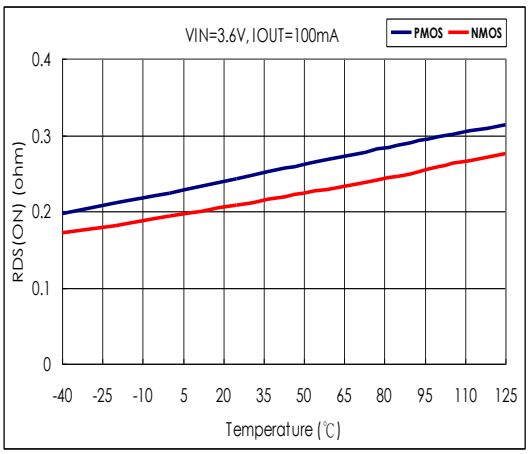
Oscillator Frequency vs Temperature



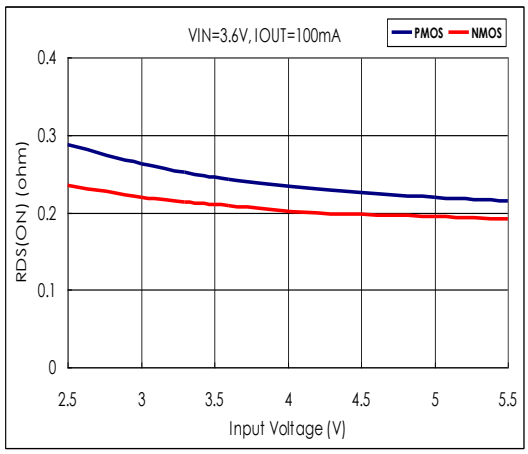
Oscillator Frequency vs Supply Voltage



$R_{DS(ON)}$ vs Temperature



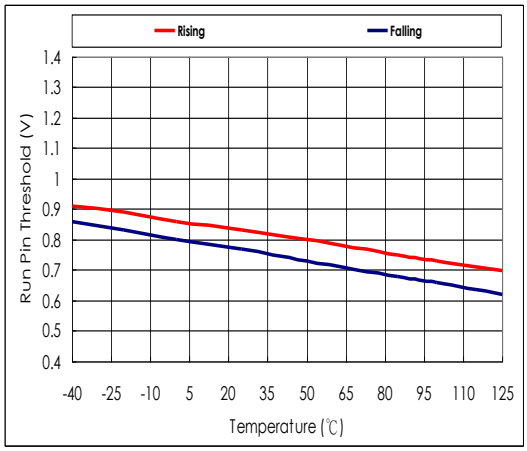
$R_{DS(ON)}$ vs Input Voltage



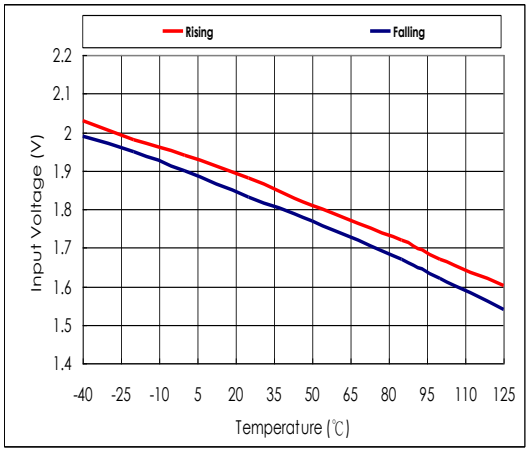
Typical Performance Characteristics (cont.)

VIN=3.6V, T_A=25℃, unless otherwise specified

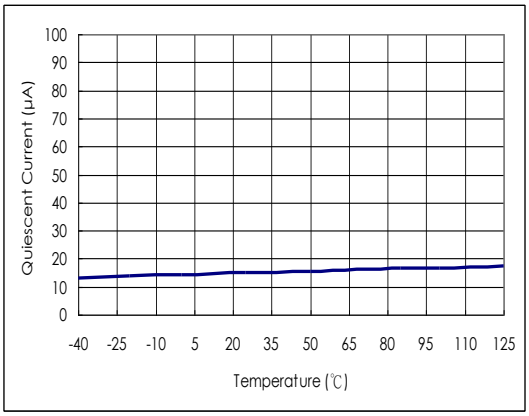
Run Pin Threshold vs Temperature



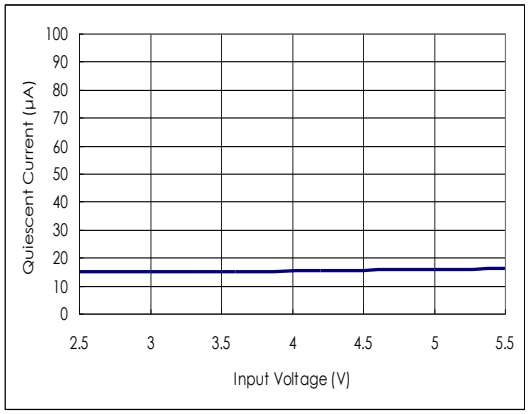
UVLO Threshold vs Temperature



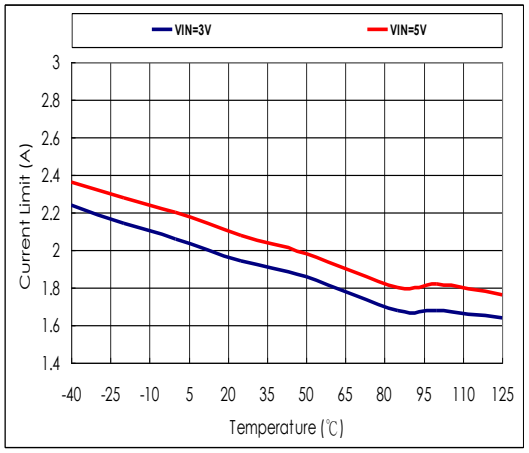
Quiescent Current vs Temperature (PFM Mode, one channel)



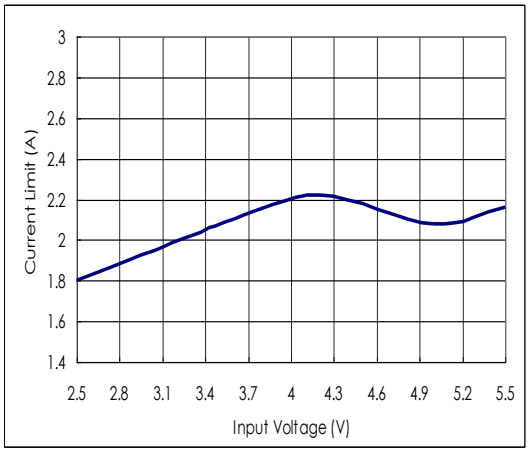
Quiescent Current vs Input Voltage (PFM Mode, one channel)



Current Limit vs Temperature (VOUT=1.2V)



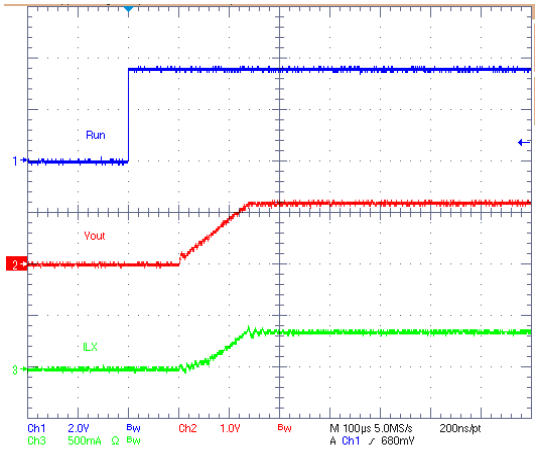
Current Limit vs Input Voltage (VOUT=1.2V)



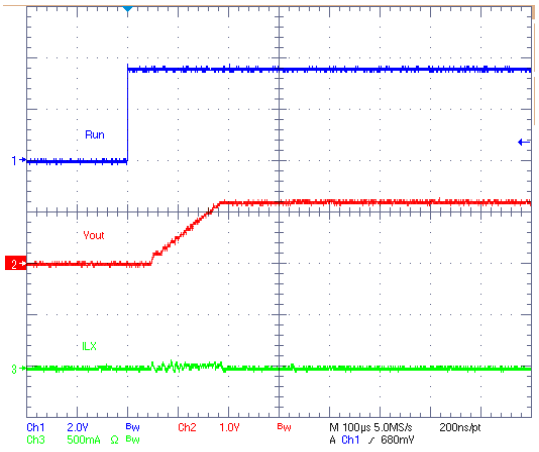
Typical Performance Characteristics (cont.)

VIN=3.6V, T_A=25℃, unless otherwise specified

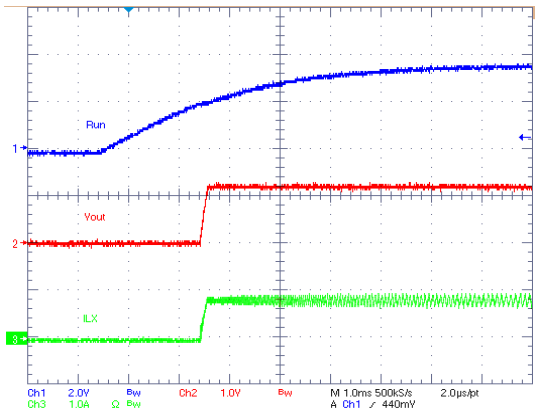
Power-On from RUN Pin (IOUT=1A)



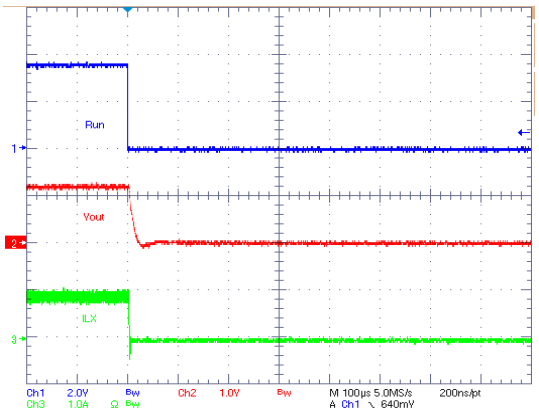
Power-On from RUN Pin (IOUT=10mA)



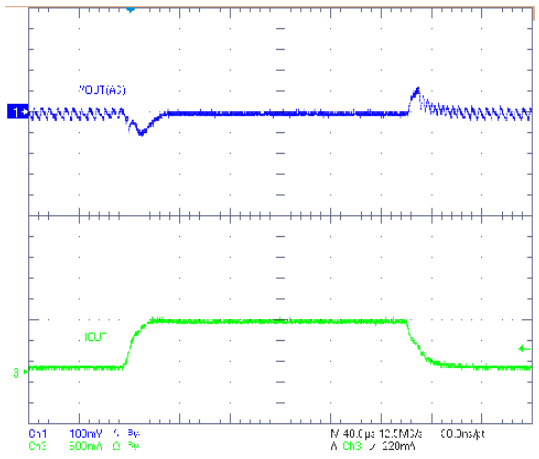
Power-On from VIN (IOUT=1A)



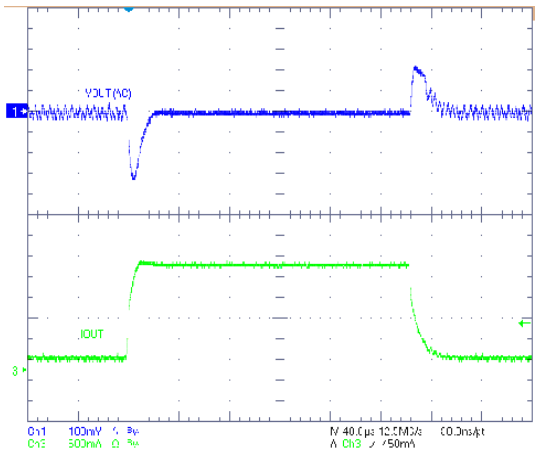
Power-Off from RUN Pin (IOUT=1A)



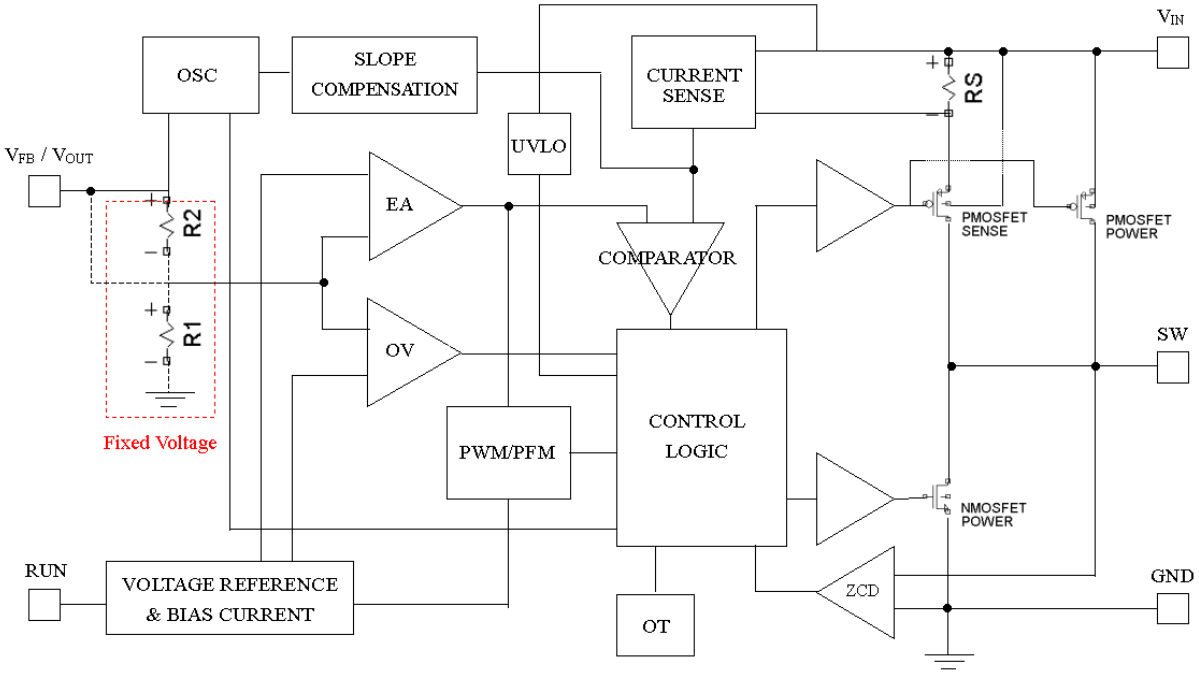
Load Step Response
(VOUT=1.2V, IOUT from 50mA to 500mA



Load Step Response
(VOUT=1.2V, IOUT from 50mA to 1A)



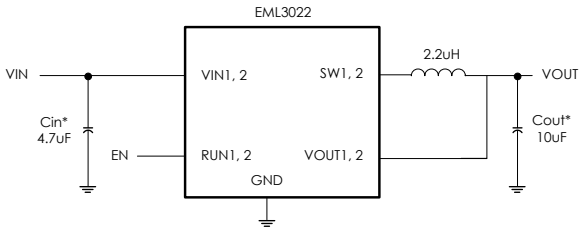
Functional Block Diagram



Applications

The typical application circuit of adjustable version is shown in Fig.1.

Fixed voltage version is shown below:



Inductor Selection

Basically, inductor ripple current and core saturation are two factors considered to decide the Inductor value. A low DCR inductor is preferred.

C_{IN} and C_{OUT} Selection

A low ESR input capacitor can prevent large voltage transients at V_{IN}. The RMS current of input capacitor is required larger than I_{RMS} calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}\left(V_{IN}-V_{OUT}\right)}}{V_{IN}} \qquad \text{Eq. 1}$$

ESR is an important parameter to select C_{OUT}. The output ripple V_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right) \qquad \text{Eq. 2}$$

Higher values, lower cost ceramic capacitors are now available in smaller sizes. These ceramic capacitors have high ripple currents, high voltage ratings and low ESR that make them ideal for switching regulator applications. Optimize very low output ripple and small circuit size is doable from Cout selection since Cout does not affect the internal control loop stability. It is recommended to use the X5R or X7R which have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage (EML3022 adjustable)

In the adjustable version, the output voltage can be determined by:

$$V_{OUT} = 0.6\,V\left(1+\frac{R_2}{R_1}\right) \qquad \text{Eq. 3}$$

Thermal Considerations

Although thermal shutdown is build-in in EML3022 that protect the device from thermal damage, the total power dissipation that EML3022 can sustain should be base on the package thermal capability. The formula to ensure the safe operation is shown in Note 1.

To avoid the EML3022 from exceeding the maximum junction temperature, the user will need to do some thermal analysis.

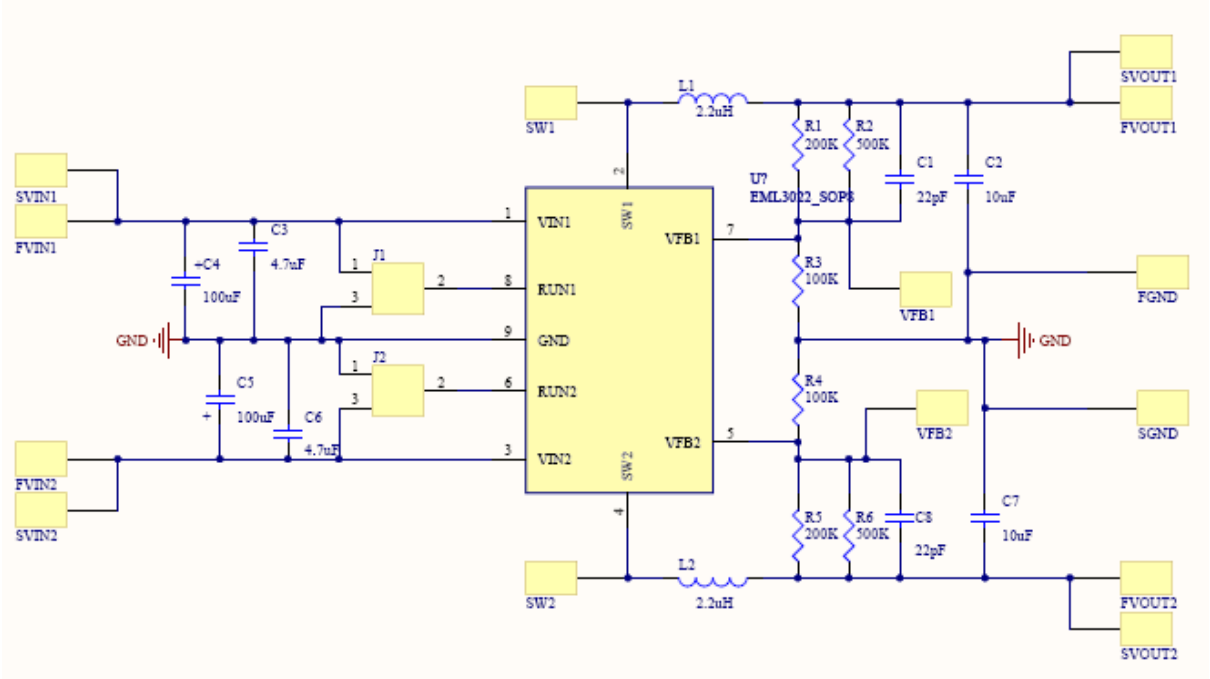
Guidelines for PCB Layout

To ensure proper operation of the EML3022, please note the following PCB layout guidelines:

1. The GND trace, the SW1, 2 trace and the VIN1, 2 trace should be kept short, direct and wide.
2. VFB1, 2 pin must be connected directly to the feedback resistors. Resistive divider R1/R1 must be connected and parallel to the output capacitor C_{OUT}.
3. The Input capacitor C_{IN} must be connected to pin VIN1, 2 as closely as possible.
4. Keep SW1, 2 nodes away from the sensitive VFB1, 2 nodes since this node is with high frequency and voltage swing.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

Applications

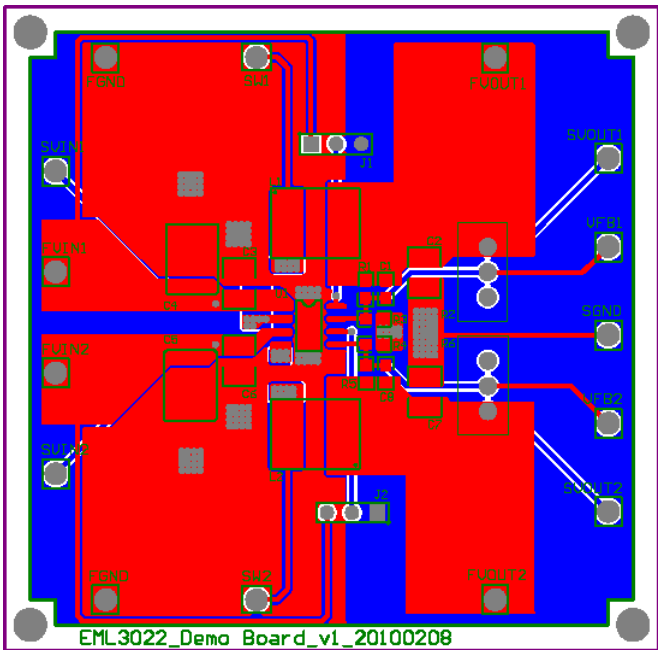
Typical schematic for PCB layout



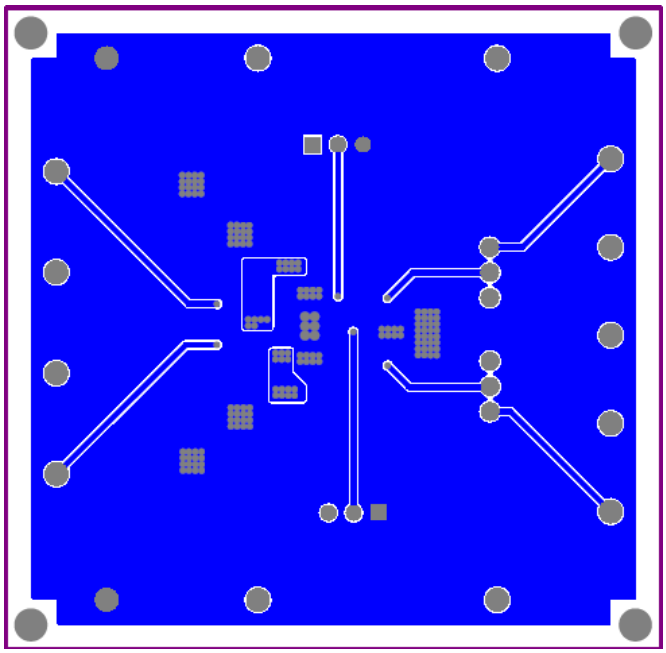
Note.

R2, R6 and C4, C5 are preserved passive component locations for testing purpose. Please remove it during normal application.

Typical schematic for PCB layout (cont.)

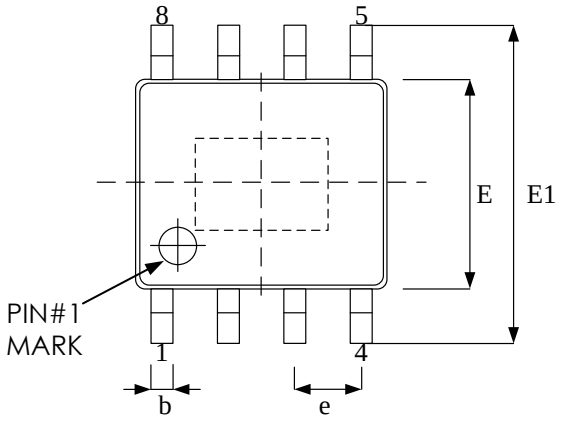


Top Layer

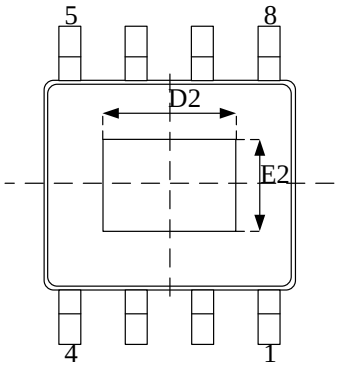


Bottom Layer

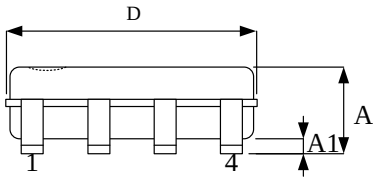
Package Outline Drawing
SOP-8 (E) (150 mil)



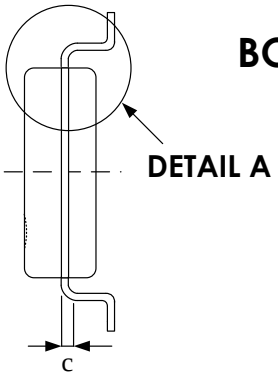
TOP VIEW

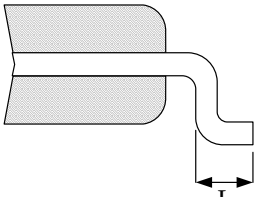


BOTTOM VIEW



SIDE VIEW





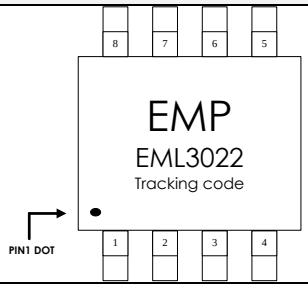
DETAIL A

Symbol	Dimension in mm	
	Min	Max
A	-	1.70
A1	0.00	0.15
b	0.31	0.51
c	0.10	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.40	1.27

Exposed pad

	Dimension in mm	
	Min	Max
D2	2.80	3.50
E2	2.00	2.60

Old order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
E-SOP-8L	adjustable	EML3022-00SE08NRR		Tape & Reel 3K units

Revision History

Revision	Date	Description
0.1	2010.04.29	Original
0.2	2010.09.16	1)Updated “Output Voltage Line Regulation” maximum is 0.6% 2)Updated “Reference Voltage Line Regulation” Maximum is 0.6%
0.3	2010.09.21	1)Skip “Preliminary” 2)Update package information
1.0	2012.08.23	Modify package outline drawing
1.1	2013.11.04	Marking logo change to ESMT POD format change
1.2	2021.07.14	Modify E-SOP-8 Dimension

Important Notice

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