# 1.5MHz 1A, Synchronous Step-Down Regulator

## General Description

EML3023 is a high efficiency step down DC/DC converter. It features an extremely low quiescent current, which is suitable for reducing standby power consumption, especially for portable applications.

The device can accept input voltage from 2.5V to 5.5V and deliver up to 1A output current. High 1.5MHz switching frequency allows the use of small surface mount inductors and capacitors to reduce overall PCB board space. Furthermore, the built-in synchronous switch improves efficiency and eliminates external Schottky diode. EML3023 uses different modulation algorithms for various loading conditions: (1) Pulse Width Modulation (PWM) for low output voltage ripple and fixed frequency noise, (2) Pulse Frequency Modulation (PFM) for improving light load efficiency, and (3) Low Dropout (LDO) Mode for providing 100% duty cycle operation during heavy loading. Adopting low reference voltage design reduces regulated output to 0.6V. The adjustable version of this device is available in both of TDFN-6 2x2mm and SOT-23-5 package.

## Features

- Achieve 97% efficiency
- Input voltage : 2.5V to 5.5V
- Output current up to 1A
- Reference voltage: 0.6V
- Quiescent current 15 $\mu$ A with no load
- Internal switching frequency: 1.5MHz
- No Schottky diode needed
- Low dropout operation: 100% duty cycle
- Shutdown current < 1 $\mu$ A
- Excellent line and load transient response
- Over-temperature protection

## Applications

- Blue-Tooth devices
- Cellular and Smart Phones
- Personal Multi-media Player (PMP)
- Wireless networking
- Digital Still Cameras
- Portable applications

## Typical Application

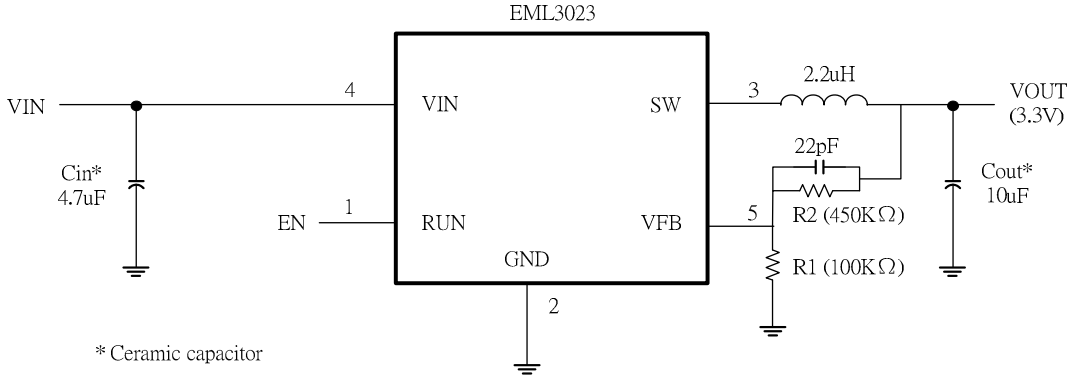
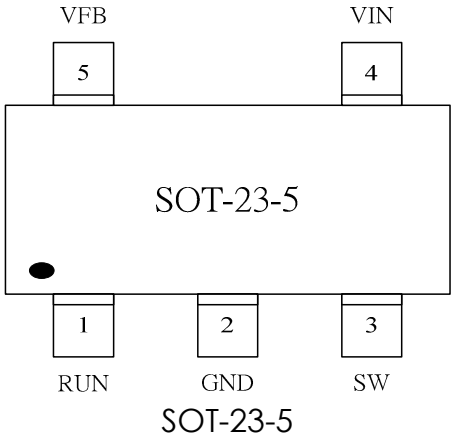



Fig. 1

## Package Configuration

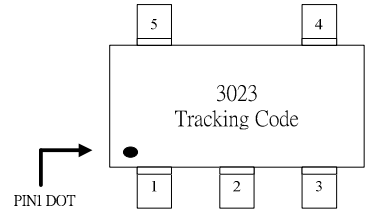


SOT-23-5

EML3023-00VF05NRR

| | |
|---|---|
| 00 | Adjustable |
| VF05 | SOT-23-5 Package |
| NRR | RoHS & Halogen free package<br>Commercial Grade Temperature Rating: -40 to 85°C<br>Package in Tape & Reel |

## Order, Mark & Packing information

| Package | Vout(V) | Product ID | Marking | Packing |
|---|---|---|---|---|
| SOT-23-5 | adjustable | EML3023-00VF05NRR |  | Tape & Reel<br>3K units |

## Pin Functions

| Pin Name | SOT-23-5 | Function |
|---|---|---|
| **RUN** | **1** | Enable Pin. Minimum 1.2V to enable the device. Maximum 0.4V to shut down the device. |
| **VIN** | **4** | Power Input Pin. Must be closely decoupled to GND pin with a 4.7μF or greater ceramic capacitor. |
| **SW** | **3** | Switch Pin. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches. |
| **GND** | **2** | Ground Pin. |
| **VFB (Adjustable)** | **5** | Feedback Pin. Receives the feedback voltage from an external resistive divider across the output. |

## Absolute Maximum Ratings

**Devices are subjected to fail if they stay above absolute maximum ratings.**

Input Voltage ---------- – 0.3V to 6V
RUN, VFB Voltages ---------- – 0.3V to $V_{IN}$
SW Voltage ---------- – 0.3V to ($V_{IN}$ + 0.3V)
Lead Temperature (Soldering, 10 sec)---------- 260°C

Operating Temperature Range ---------- –40°C to 85°C
Junction Temperature (Notes 1, 3) ---------- 150°C
Storage Temperature Range ---------- – 65°C to 150°C
ESD Susceptibility HBM ---------- 2KV
MM ---------- 200V

## Thermal data

| Package | Thermal resistance | Parameter | Value |
|---|---|---|---|
| TDFN-6 (2x2 mm) | $\theta_{JA}$ (Note 4) | Junction-ambient | 74.7°C/W |
| | $\theta_{JC}$ (Note 5) | Junction-case | 24°C/W |
| SOT-23-5 | $\theta_{JA}$ (Note 4) | Junction-ambient | 134.5°C/W |
| | $\theta_{JC}$ (Note 5) | Junction-case | 81°C/W |

## Electrical Characteristics

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A$ = 25°C. $V_{IN}$ = 3.6V unless otherwise specified.**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage Range | | | 2.5 | | 5.5 | V |
| $I_{VFB}$ | Feedback Current | | | | | ±100 | nA |
| $V_{FB}$ | Regulated Feedback Voltage | | | 0.588 | 0.600 | 0.612 | V |
| $V_{OUT}$% | Output Voltage Accuracy | $I_{OUT}$=100mA | ● | -3 | | +3 | % |
| $\Delta V_{FB}$ | Reference Voltage Line Regulation | $V_{IN}$ = 2.5V to 5.5V | ● | | | 0.4 | %/V |
| $\Delta V_{OUT}$ | Output Voltage Line Regulation | $V_{IN}$ = 2.5V to 5.5V | ● | | | 0.4 | %/V |
| $I_{PK}$ | Peak Inductor Current | $V_{FB}$ = 0.5V or $V_{OUT}$ = 90%, | | 1.5 | 2.3 | | A |
| $I_S$ | PWM Quiescent Current (Note 2) | $V_{FB}$ = 0.5V or $V_{OUT}$ = 90% | | | 188 | | μA |
| | PFM Quiescent Current | $V_{FB}$ = 0.65V or $V_{OUT}$ = 108% | | | 15 | | μA |
| | Shutdown | $V_{RUN}$ = 0V, $V_{IN}$ = 4.2V | | | 0.1 | 1 | μA |
| $f_{OSC}$ | Oscillator Frequency | $V_{FB}$ = 0.6V or $V_{OUT}$ = 100% | ● | 1.2 | 1.5 | 1.8 | MHz |
| | Short-Circuit Oscillator Frequency | $V_{FB}$ = 0V or $V_{OUT}$ = 0V | ● | | 900 | | kHz |
| $R_{PFET}$ | $R_{DS(ON)}$ of PMOS | $I_{SW}$ = 100mA | | | 0.24 | | Ω |
| $R_{NFET}$ | $R_{DS(ON)}$ of NMOS | $I_{SW}$ = –100mA | | | 0.21 | | Ω |
| $V_{UVLO}$ | VIN UVLO Threshold | | | | 1.8 | | V |
| | VIN UVLO Hysteresis | | | | 50 | | mV |
| $I_{LSW}$ | SW Leakage | $V_{RUN}$ = 0V, $V_{SW}$ = 0V or 5V, $V_{IN}$ = 5V | | | | ±1 | μA |
| $V_{RUN}$ | Enable Threshold | | ● | 1.2 | | | V |
| | Shutdown Threshold | | ● | | | 0.4 | V |
| $I_{RUN}$ | RUN Leakage Current | | ● | | | ±1 | μA |
| $T_{SD}$ | Thermal Shutdown | | | | 170 | | ℃ |
| | Thermal Shutdown Hysteresis | | | | 30 | | ℃ |

**Note 1:** $T_J$ is a function of the ambient temperature $T_A$ and power dissipation $P_D$ ($T_J = T_A + (P_D) * (165°C/W)$).

**Note 2:** Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.

**Note 3:** This IC has a built-in over-temperature protection to avoid damage from overloaded conditions.

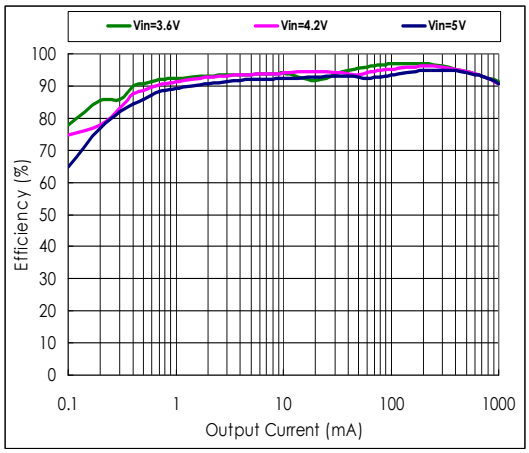
**Note 4:** $\theta_{JA}$ is measured in the natural convection at $T_A$=25℃ on a highly effective thermal conductivity test board (2 layers , 2S0P ) according to the JEDEC 51-7 thermal measurement standard.

**Note 5:** $\theta_{JC}$ represents the heat resistance between the chip and the package top case.

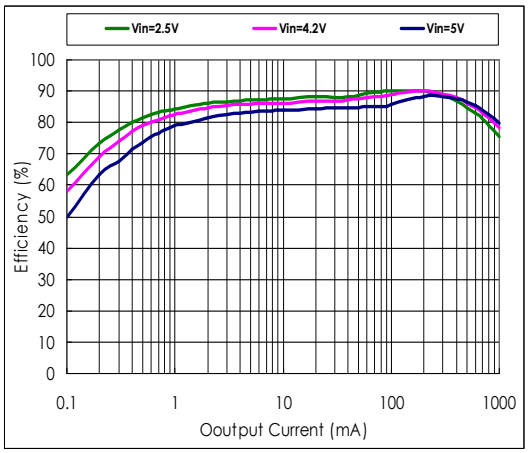
## Typical Performance Characteristics

**$V_{IN}$=3.6V, $T_A$=25℃, unless otherwise specified**

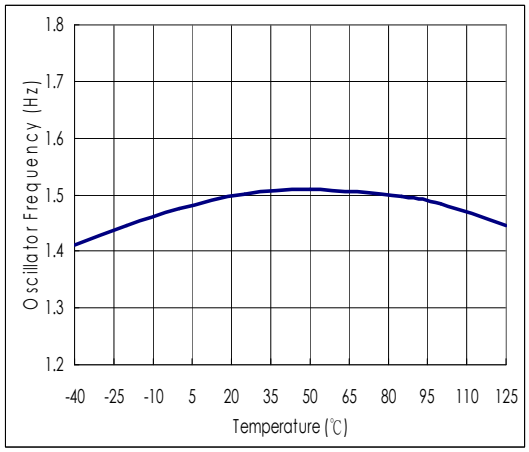
**Efficiency vs. Output Current ($V_{OUT}$=3.3V)**



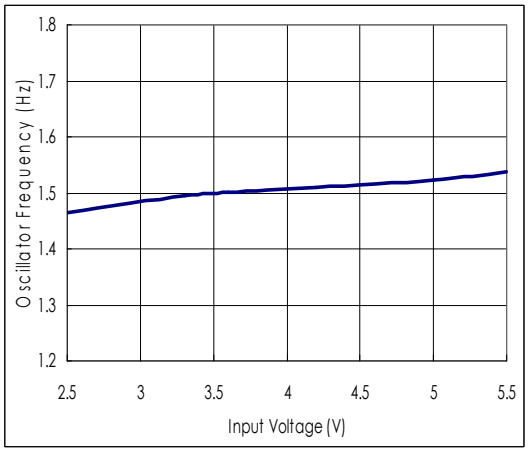

**Efficiency vs. Output Current ($V_{OUT}$=1.2V)**



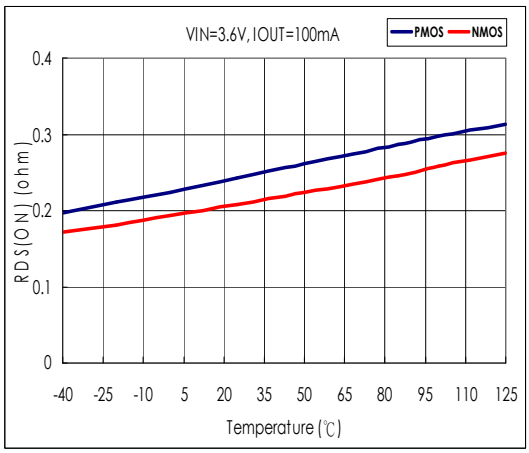

**Oscillator Frequency vs. Temperature**



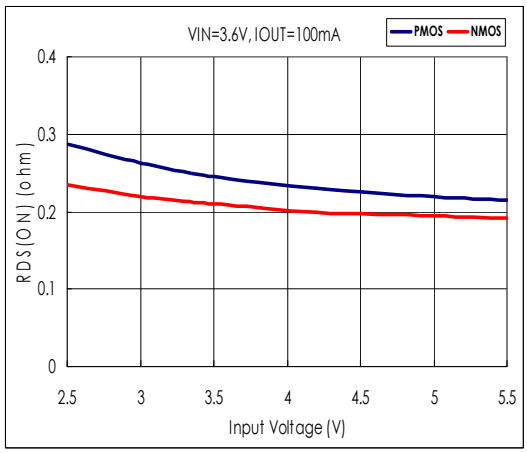

**Oscillator Frequency vs. Supply Voltage**




**$R_{DS(ON)}$ vs. Temperature**



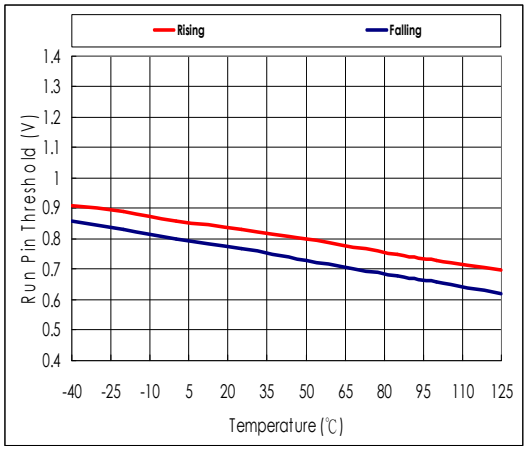

**$R_{DS(ON)}$ vs. Input Voltage**



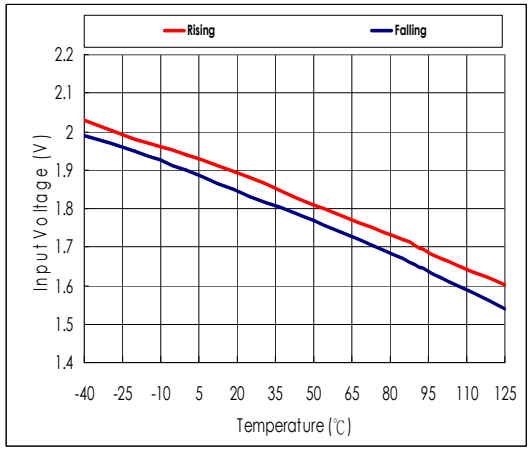
## Typical Performance Characteristics (cont.)

**$V_{IN}$=3.6V, $T_A$=25℃, unless otherwise specified**

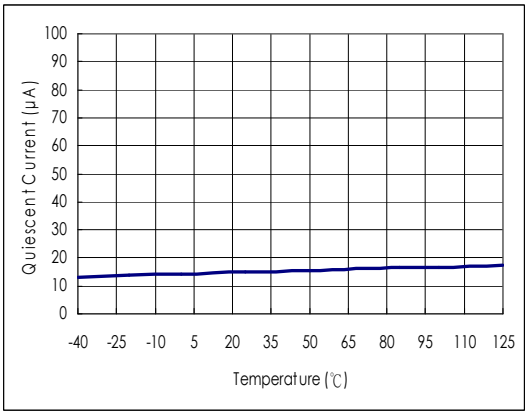
### Run Pin Threshold vs. Temperature



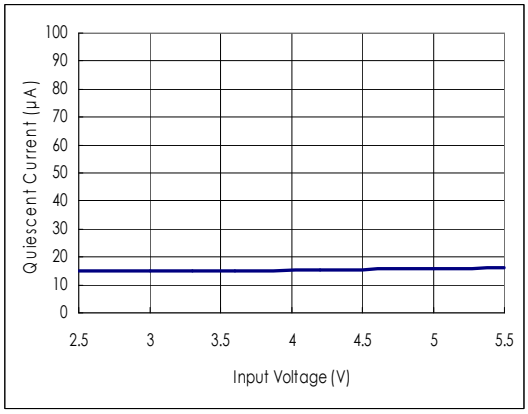

### UVLO Threshold vs. Temperature



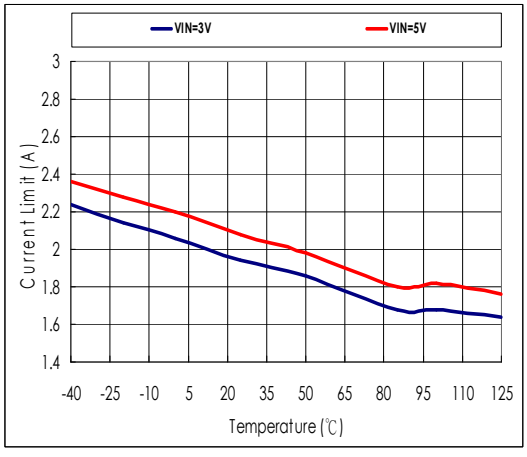

### Quiescent Current vs. Temperature (PFM Mode)



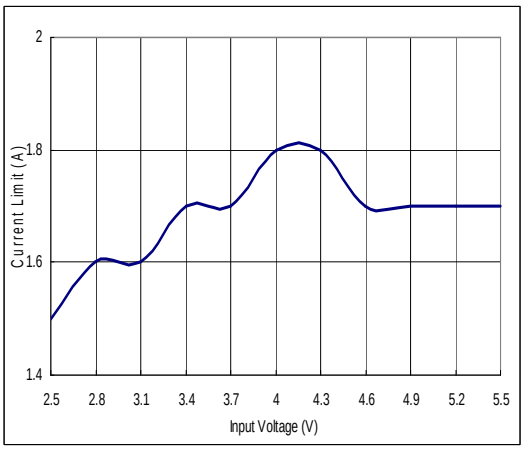

### Quiescent Current vs. Input Voltage (PFM Mode)




### Current Limit vs. Temperature ($V_{OUT}$=1.2V)



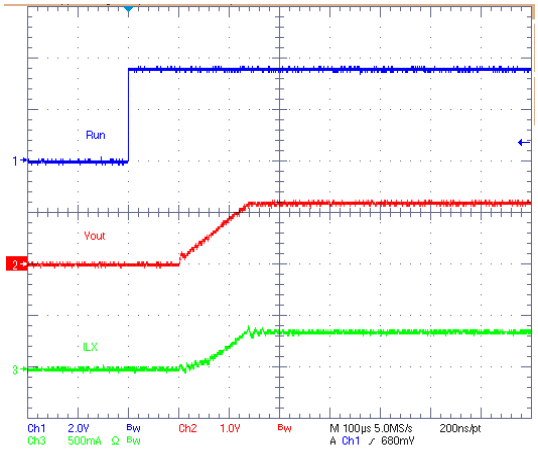

### Current Limit vs. Input Voltage ($V_{OUT}$=1.2V)



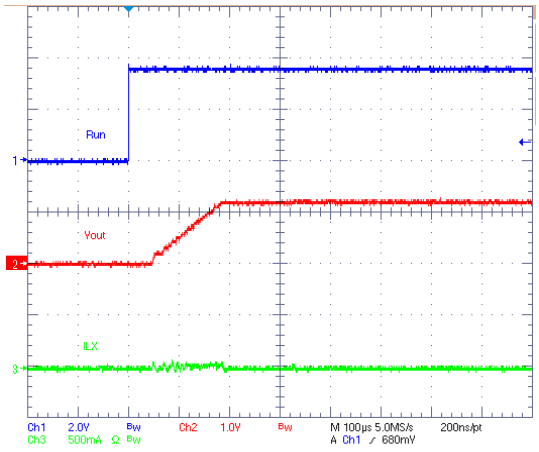
## Typical Performance Characteristics (cont.)

**$V_{IN}$=3.6V, $T_A$=25℃, unless otherwise specified**

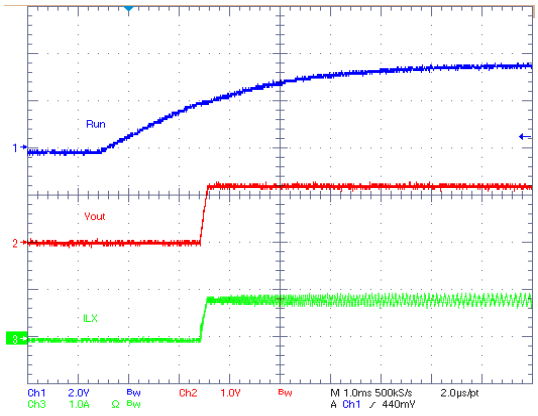
**Power-On from RUN Pin ($I_{OUT}$=1A)**



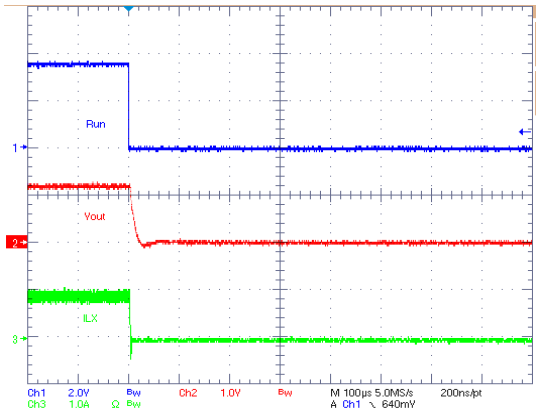

**Power-On from RUN Pin ($I_{OUT}$=10mA)**



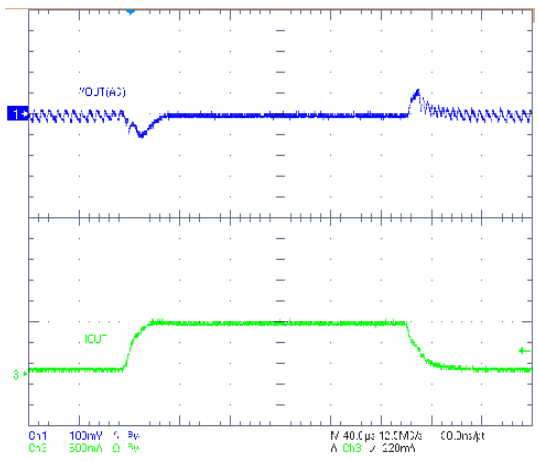

**Power-On from VIN ($I_{OUT}$=1A)**



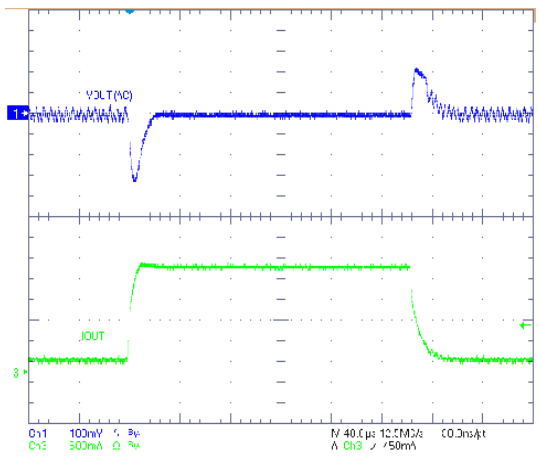

**Power-Off from RUN Pin ($I_{OUT}$=1A)**



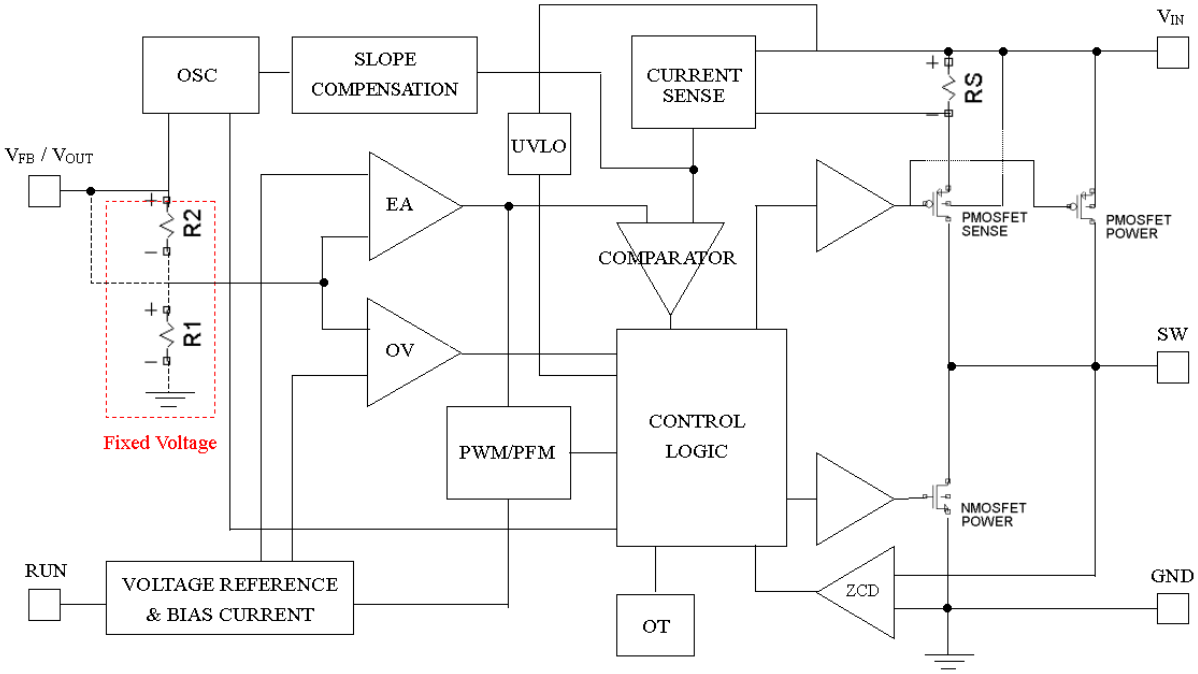

**Load Step Response ($V_{OUT}$=1.2V, $I_{OUT}$ from 50mA to 500mA**




**Load Step Response ($V_{OUT}$=1.2V, $I_{OUT}$ from 50mA to 1A)**



## Functional Block Diagram



## Applications

The typical application circuit of adjustable version is shown in Fig.1.

**Inductor Selection**

Inductor ripple current and core saturation current are the two main factors that decide the Inductor value. A low DCR inductor is preferred.

**$C_{IN}$ and $C_{OUT}$ Selection**

A low ESR input capacitor can prevent large voltage transients at $V_{IN}$. The RMS current of input capacitor is required larger than $I_{RMS}$ calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{Eq. 1}$$

ESR is an important parameter to select $C_{OUT}$, which can be seen in the following output ripple $V_{OUT}$ equation:

$$\Delta V_{OUT} \cong \Delta I_L \left( ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right) \quad \text{Eq. 2}$$

Cheaper and smaller ceramic capacitors with higher capacitance values are now commercially available. These ceramic capacitors have low ripple currents, high voltage ratings and low ESR which make them suitable for switching regulator applications. It is feasible to optimize very low output ripples by Cout since Cout does not affect the internal control loop stability. X5R or X7R types are recommended since they have the best temperature and voltage characteristics of all ceramics capacitors.

**Output Voltage (EML3023 adjustable)**

In the adjustable version, the output voltage can be determined by:

$$V_{OUT} = 0.6\,V \left( 1 + \frac{R_2}{R_1} \right) \quad \text{Eq. 3}$$

**Thermal Considerations**

Although the thermal shutdown circuit is designed in EML3023 to protect the device from thermal damage, the total power dissipation that EML3023 can sustain depends on the thermal capability of the package. The formula to ensure the safe operation is shown in note 1 on page 5.

To avoid the EML3023 from exceeding the maximum junction temperature, the user should perform some thermal analysis during PCB design.

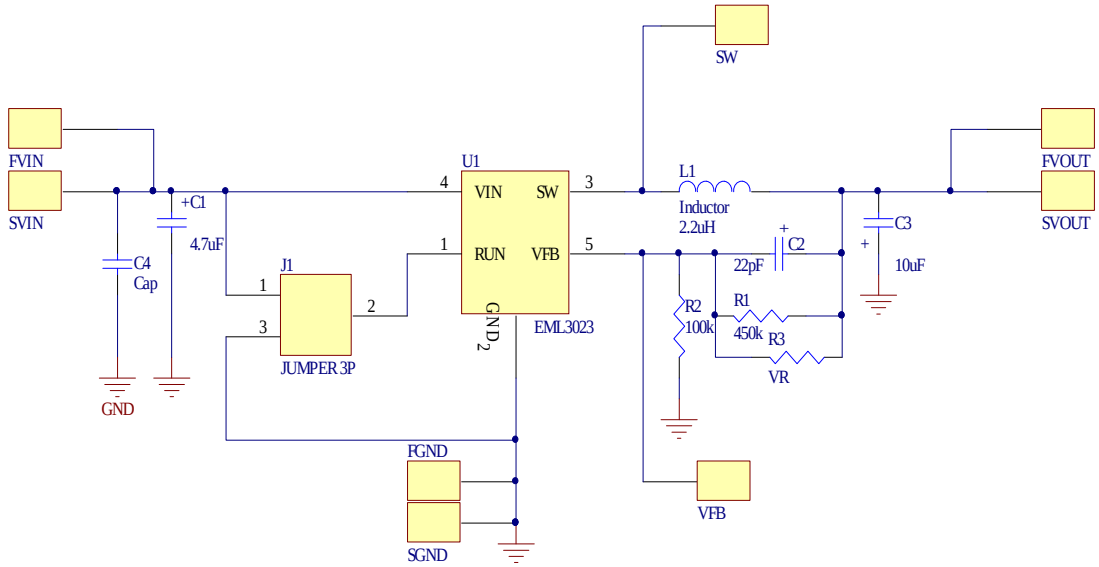
**Guidelines for PCB Layout**

To ensure proper operation of the EML3023, please note the following PCB layout guidelines:

1. The GND, SW and the VIN trace should be kept short, direct and wide.
2. VFB pin must be connected directly to the feedback resistors. Resistive divider R1/R1 must be connected parallel to the output capacitor $C_{OUT}$.
3. The Input capacitor $C_{IN}$ must be connected to the pin VIN as close as possible.
4. Keep SW node away from the sensitive VFB node since this node has high frequency and voltage swing.
5. Keep the (–) plates of $C_{IN}$ and $C_{OUT}$ as close as possible.

## Applications

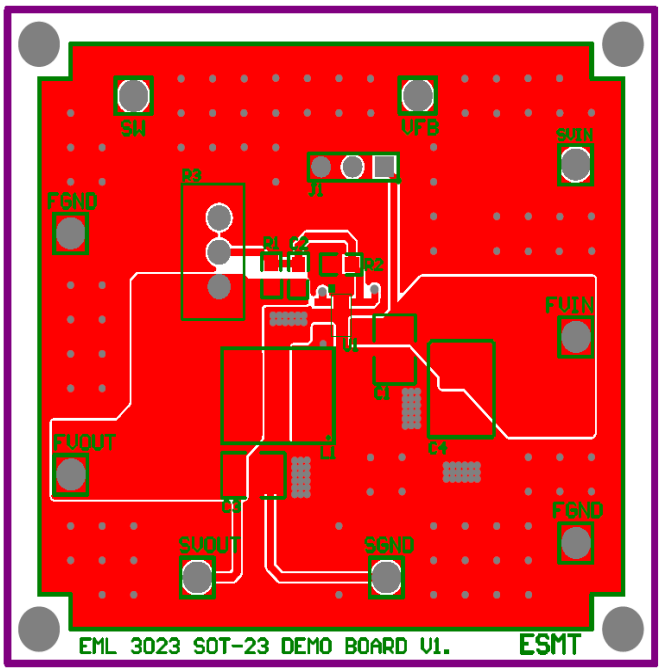
## Typical schematic for PCB layout



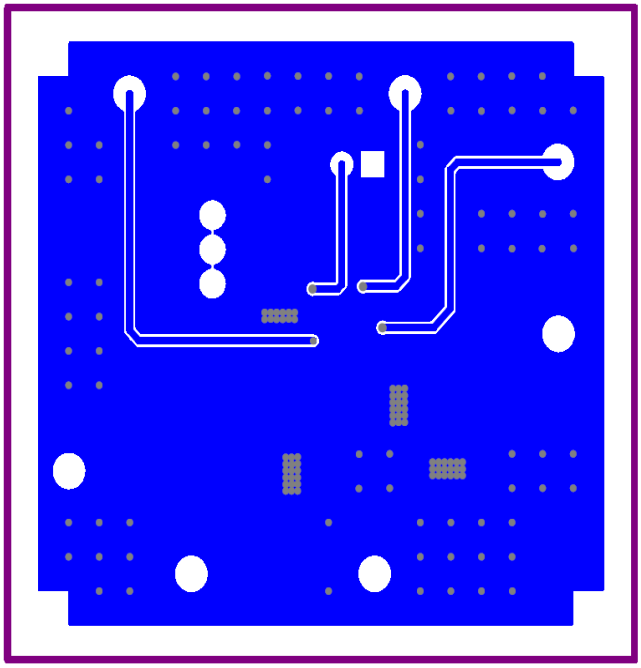

Note.

R3 and C4 are reserved locations for testing purposes. They are removed during normal applications.

## Typical schematic for PCB layout (cont.)

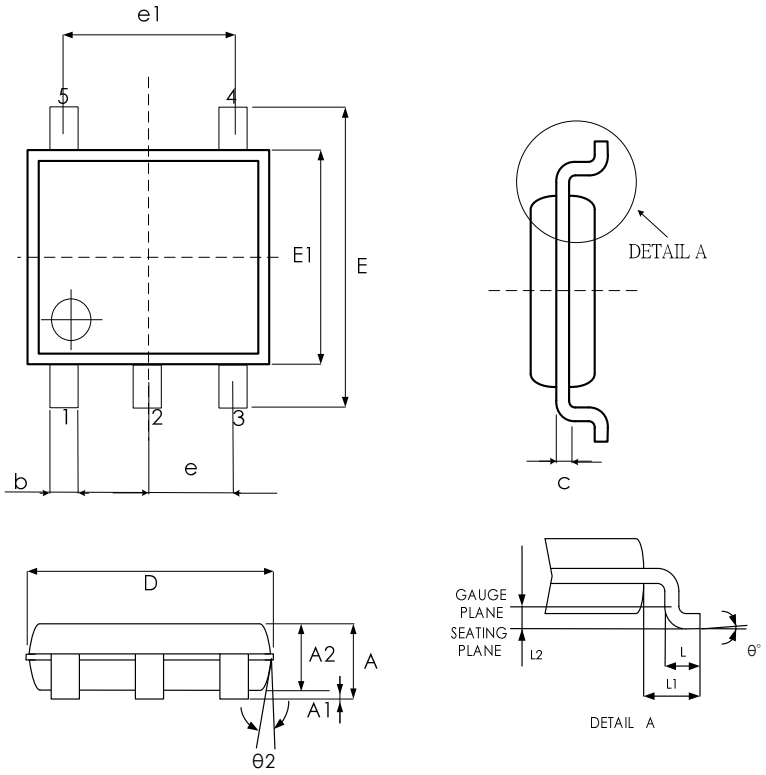



Top Layer



Bottom Layer

**Package Outline Drawing**
**SOT-23-5**




| SYMBPLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 1.05 | 1.20 | 1.35 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 1.00 | 1.10 | 1.20 |
| B | 0.30 | — | 0.50 |
| C | 0.08 | — | 0.20 |
| D | 2.80 | 2.90 | 3.00 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.50 | 1.60 | 1.70 |
| E | 0.95 BSC | | |
| e1 | 1.90 BSC | | |
| L | 0.30 | 0.45 | 0.55 |
| L1 | 0.60 REF | | |
| θ° | 0 | 5 | 10 |
| θ2° | 6 | 8 | 10 |

UNIT: mm

## Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 2011.04.07 | Original. |
| 1.1 | 2011.04.20 | 1.Fix product ID<br>2.Fix enable/shutdown threshold spec |
| 1.2 | 2015.12.09 | 1. Added the VIN UVLO Threshold & Hysteresis.<br>2. Added the Thermal shutdown & Hysteresis. |

Important Notice



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