2.0A, Synchronous Step-Down DC-DC Converter

General Description

EML3171 is a high efficiency, DC-DC synchronous buck converter which provides 2.0A output loading after output voltage reach preset voltage. EML3171 uses different modulation algorithms for various loading conditions. Under heavy load, EML3171 regulates the output voltage using Pulse Width Modulation (PWM). The PWM mode provides low output voltage ripple and fixed frequency noise. While in light load, it enters Power Skip Modulation (PSM) automatically to ensure a highly efficient operation at light load condition. Under very heavy load condition or when the input voltage approaches the output voltage, EML3171 enters low dropout voltage operation under 100% duty cycle.

The internal generated 0.8V precision feedback reference voltage is designed for low output voltage request. Low Power-FET Ron synchronous switch dramatically reduces conduction loss.

The EML3171 is available in an 8-pin, space-saving TDFN-3x3 package.

Features

- Wide Operating Voltage Ranges : 2.6V to 5.5V
- 2.0A Output Current
- High efficiency Buck Power Converter
- Auto-select PSM/PWM
- LDO mode: duty cycle: 100%
- Synchronous Power Switches Rectification, no Schottky Diode Required
- 1.4MHz Switching Frequency
- Internal Soft-Start
- Current Limit Protection
- Over Temperature Protection
- Output Shorting Protect
- Output Over Voltage Protection

Applications

- Cellular telephone
- Wireless and DSL Modems
- Digital Still Cameras
- Portable Products
- MP3 Players

Typical Application

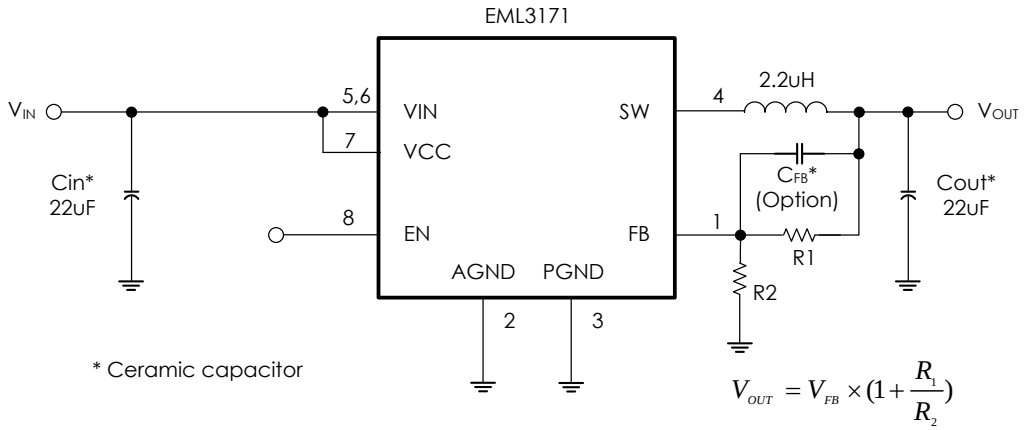
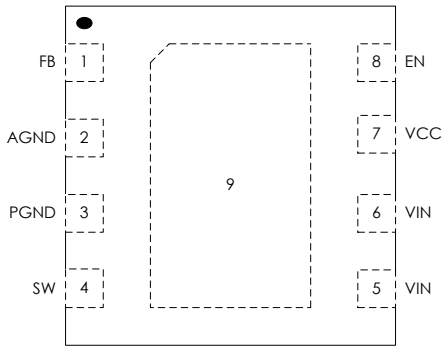


Fig. 1 EML3171 application circuit

Package Configuration

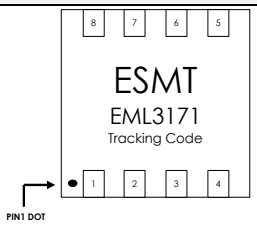


TDFN-8L

EML3171-XXFH08NRR

XX	Output Voltage
00	Adjustable Output
FH08	TDFN-8L (3x3mm) Package
NRR	RoHS & Halogen free package Commercial Grade Temperature Rating: -40 to 85°C Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
TDFN-8L (3x3mm)	Adjustable	EML3171-00FH08NRR		Tape & Reel 5K units

Functional Block Diagram

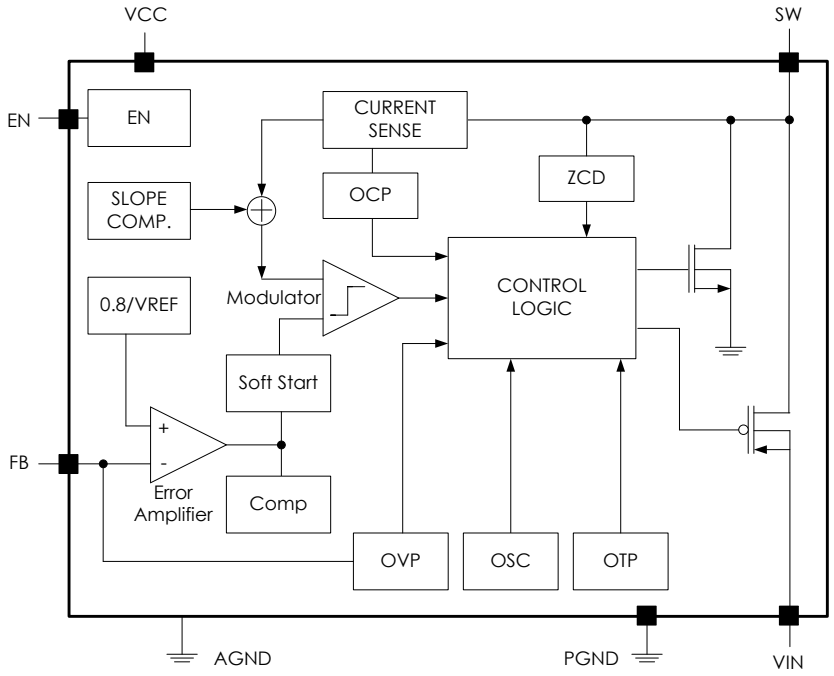


Fig. 2

Pin Functions

Pin Name	TDFN-8L	Function
FB	1	**Feedback Pin.** Receives the feedback voltage from an external resistive divider across the output.
AGND	2	**Analog Ground Pin.**
PGND	3	**Power Switch Ground Pin.**
SW	4	**Switch Pin.** Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
VIN	5, 6	**Power Supply Pin.** Must be closely decoupled to PGND pin with a 22μF or greater ceramic capacitor.
VCC	7	**Analog Input Pin.** Supply power to internal circuit.
EN	8	**Enable Pin.** Chip enable pin (1:Enable ; 0:Disable).
Exposed pad	9	**Thermal pad.** Recommend connecting the thermal pad to the PGND for excellent power dissipation.

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage (VIN, VCC) ---------- – 0.3V to 6.0V
EN, FB Voltages ---------- – 0.3V to V_{IN}
SW Voltage ---------- – 0.3V to (V_{IN} + 0.3V)
Lead Temperature (Soldering, 10 sec) ---------- 260°C

Operating Temperature Range ----- –40°C to 85°C
Junction Temperature (Note 1) ---------- 150°C
Storage Temperature Range -------- – 65°C to 150°C

Thermal data

Package	Thermal resistance	Parameter	Value
TDFN-8 (3x3mm)	θ_{JA} (Note 2)	Junction-ambient	110°C/W
	θ_{JT} (Note 3)	Junction-top of package	8.5°C/W

Electrical Characteristics

V_{IN}=V_{VCC}=V_{EN}=3.6V, V_{OUT}=1.2V, V_{FB}=0.8V, L=2.2uH, C_{IN}=22uF, C_{OUT}=22uF, T_A = 25°C unless otherwise specified.

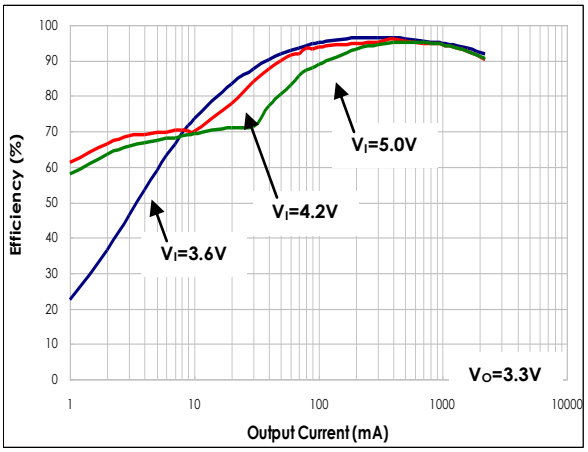
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.6		5.5	V
I_Q	Supply Current V_{IN}=3.6V	Switching (EN=VCC)		170		μA
		Shutdown (EN=0)			1	μA
UVLO	Under Voltage Lockout	When SW starts/stops switching	1.8		2.1	V
Vref	Reference Voltage	V_{IN} = 2.6V to 5.0V	0.784	0.8	0.816	V
V_{EN}	EN Input Low Voltage	-40℃ ~ +85℃			0.4	V
	EN Input High Voltage		1.5			V
V_O	Output Voltage Range	When using external feedback resistors to drive FB	0.8		VIN	V
Vout	Output Voltage Accuracy	2.6V≦V_I≦5.5V, 0mA≦I_O≦3A	0.97xV_{NOM}	V_{NOM}	1.03xV_{NOM}	V
$\Delta V_{OUT}/\Delta V_{OU}$	Line Regulation	V_{IN} = 2.6V to 5.0V, I_{OUT}=10mA		0.04		%/V
		V_{IN} = 2.6V to 5.0V, I_{OUT}=2.0A		0.08		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{out} = 1mA to 2.0A		0.01		%/A
$R_{ON(P)}$	$R_{DS(ON)}$ of PMOS	I_{OUT}=100mA		100		mΩ
$R_{ON(N)}$	$R_{DS(ON)}$ of NMOS	I_{OUT}=100mA		100		mΩ
I_{OCH}	High Side Current Limt	Duty Cycle = 100%, V_{IN} = 2.6V to 5.0V	3.75	4.5	6	A
I_{OCL}	Low Side Current Limt			-0.6		A
F_{OSC}	Oscillator Frequency	VFB=0.8V, -40℃~+85℃	1.12	1.4	1.68	MHz
Max. Duty	Maximum Duty	V_{IN} = 2.6V to 5.0V	100			%
Min. Duty	Minimum Duty.			15		%
OTP	Thermal Shutdown	Hysteresis=35℃		165		℃

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D (T_J = T_A + (P_D) *θ_{JA})).
Note 2: θ_{JA} is measured in the natural convection at T_A=25℃ on a highly effective thermal conductivity test board(2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.
Note 3: θ_{JT} represents the heat resistance between the chip and the center of package top.

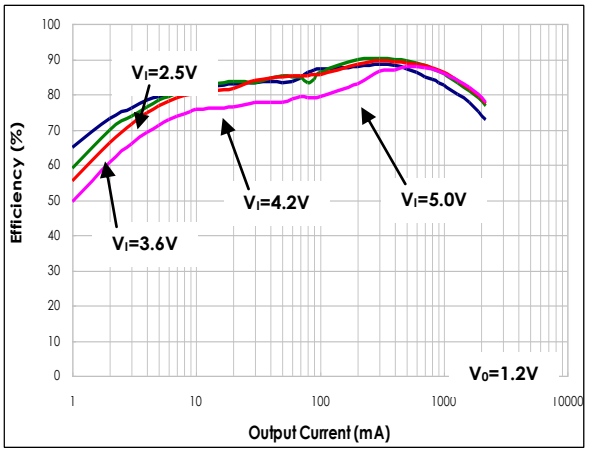
Typical Performance Characteristics

V_{IN}=5.0V, T_A=25℃, L=2.2uH, C_{IN}=22Uf, C_{OUT}=22Uf,unless otherwise specified

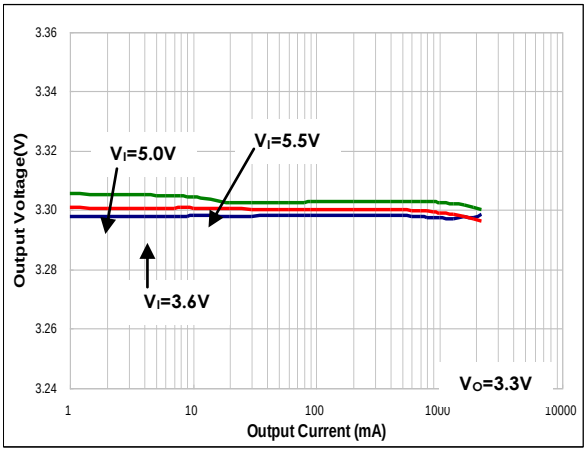
Efficiency vs. Load (Fig. 3)



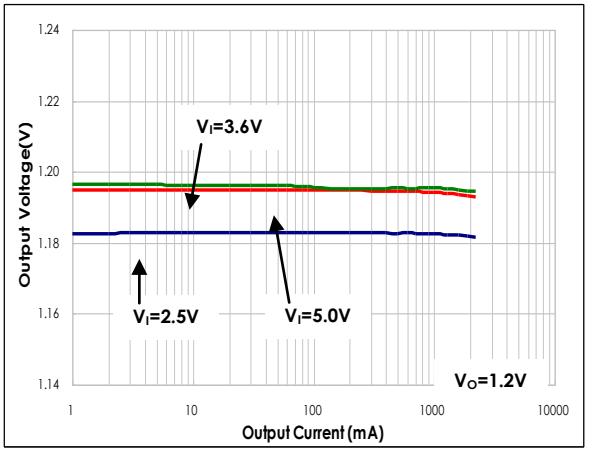
Efficiency vs. Load (Fig. 4)



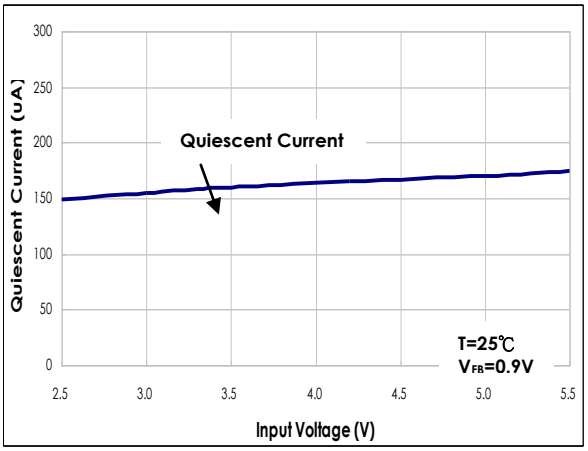
Load Regulation (Fig. 5)



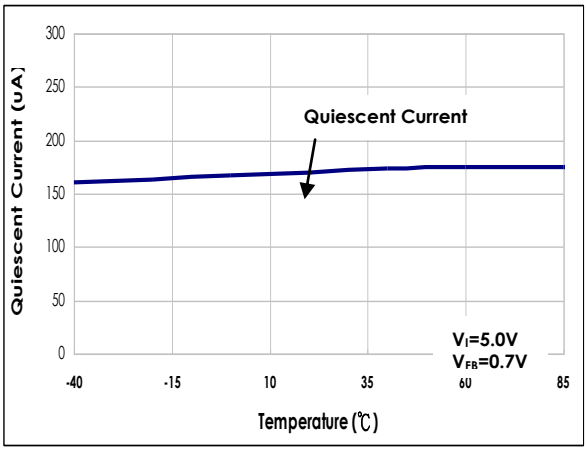
Load Regulation (Fig. 6)



Quiescent Current vs. Input Voltage (Fig. 7)



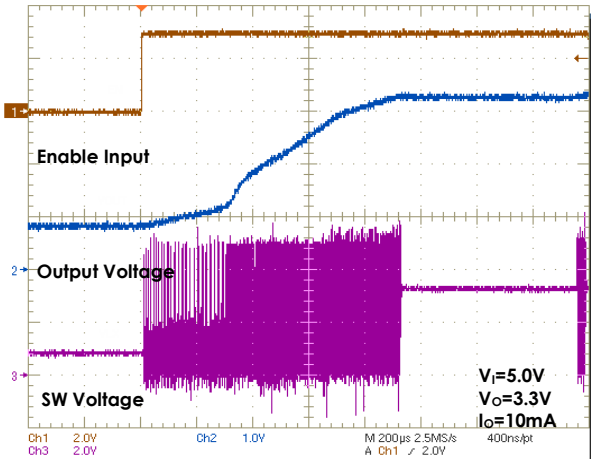
Quiescent Current vs. Temperature (Fig. 8)



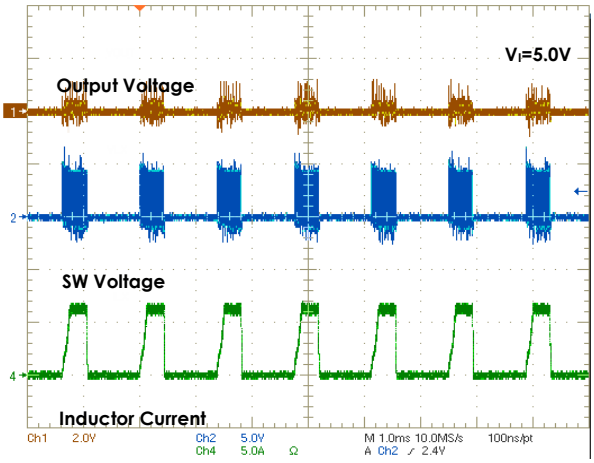
Typical Performance Characteristics

V_{IN}=5.0V, T_A=25℃, L=2.2Uh, C_{IN}=22Uf, C_{OUT}=22Uf,unless otherwise specified

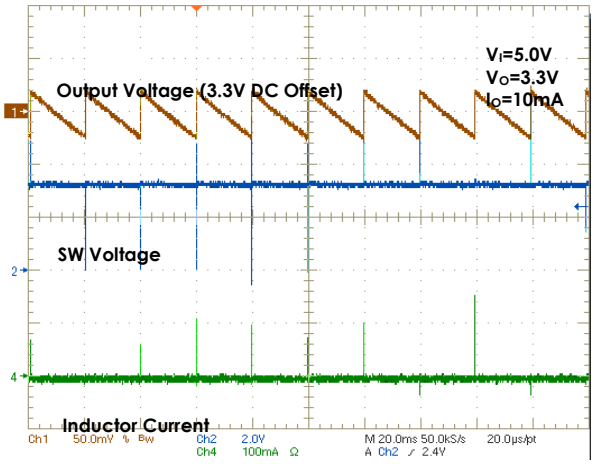
Start-up, Enable from EN Pin (Fig. 9)



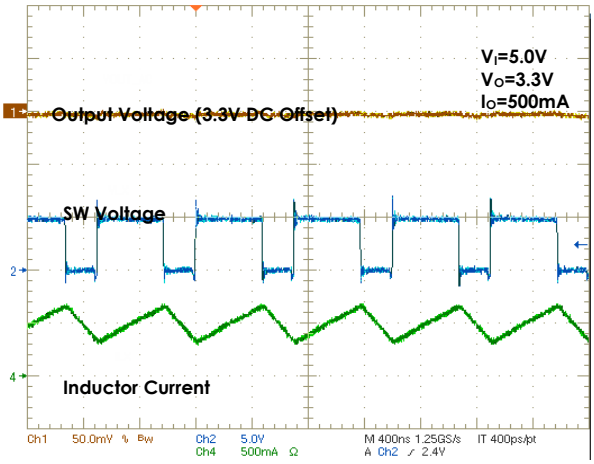
Short Circuit Response (Fig. 10)



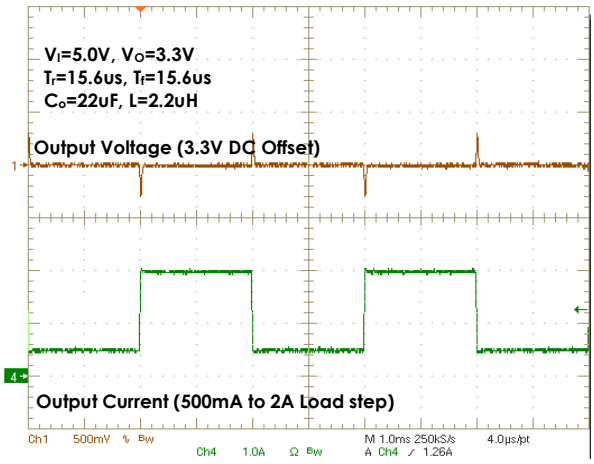
PSM Operation (Fig. 11)



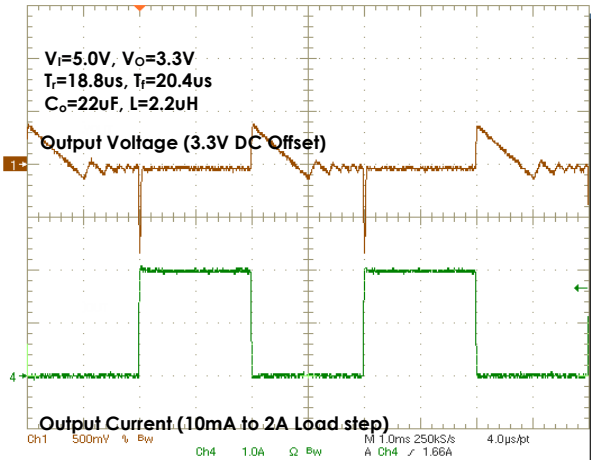
PWM Operation (Fig. 12)



Load Transient Response (Fig. 13)



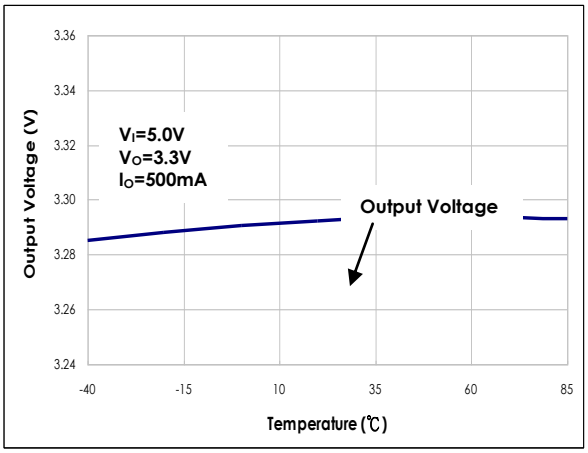
Load Transient Response (Fig. 14)



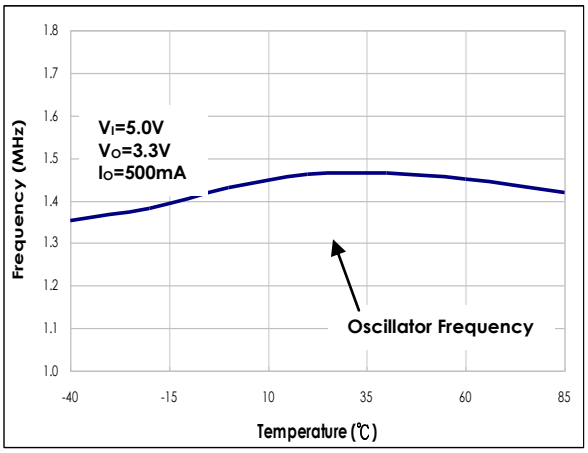
Typical Performance Characteristics (cont.)

V_{IN}=5.0V, T_A=25℃, L=2.2Uh, C_{IN}=22Uf, C_{OUT}=22Uf, unless otherwise specified

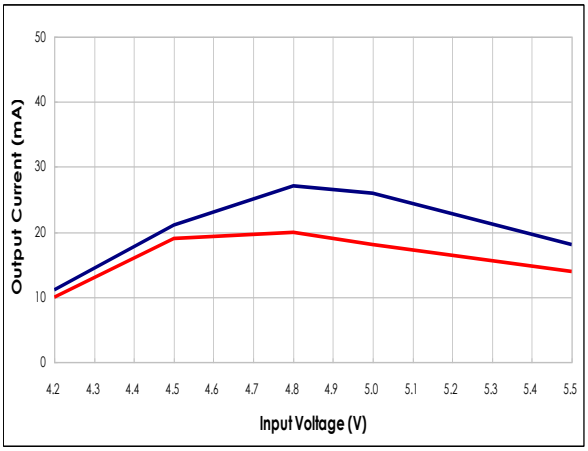
Output Voltage vs. Temperature (Fig. 15)



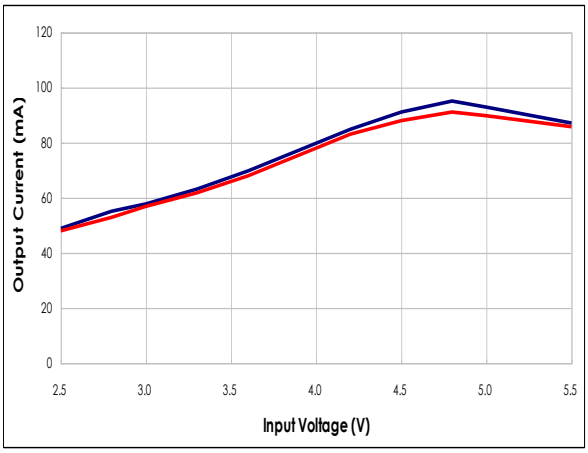
Oscillator Frequency vs. Temperature (Fig.16)



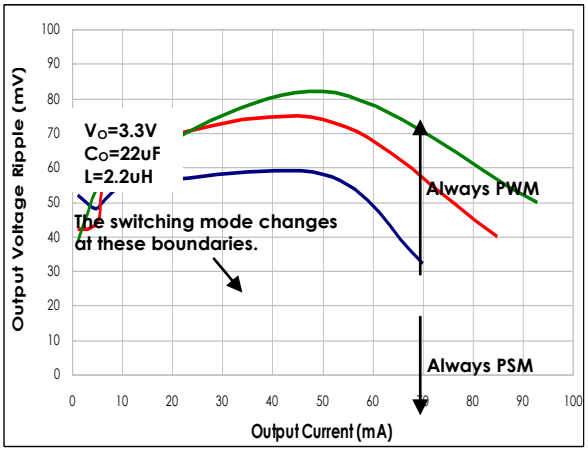
PSM/PWM Boundaries (Fig.17)



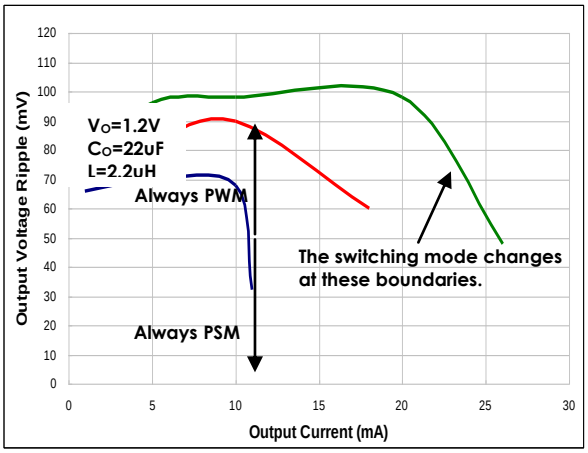
PSM/PWM Boundaries (Fig.18)



Output Voltage Ripple (Fig.19)



Output Voltage Ripple (Fig.20)



Application Information

Detailed Description

The EML3171 is a synchronous, step-down DC/DC converter. It allows up to 2A current output with adjustable output voltage. Throughout the entire operating range, EML3171 can maintain high efficiency using both PWM (heavy load) and PSM (light load) modes with very small output voltage ripple performance.

During normal operation, the internal oscillator sends a pulse signal to set latch to turn on/off internal high-side MOSFET and low-side MOSFET during each clock cycle. When the current-mode ramp signal which is the sum of internal high-side MOSFET current and slope compensation ramp exceeds output voltage of error amplifier, the PWM comparator will send a signal to reset latch and turn off/on internal high-side MOSFET/low-side MOSFET. The error amplifier adjusts its output voltage by comparing the reference voltage and the feedback voltage.

The basic EML3171 application circuits are shown as in Figure 1, External components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

PSM

In order to increase light load efficiency, save switching loss is used in EML3171. During in light load, the device only switching when output voltage is below the pre-set threshold. This function can skip some switching cycle that save unnecessary loss. The fig.11 illustrates, as the loading increases, the operation frequency increases until IC goes into normal operation frequency 1.4MHz. The fig.11 and fig.12 illustrate the difference between PSM and PWM output voltage ripple. The switching frequency and output ripple is dependant on factors such as loading, inductor and output capacitance. Besides, the input and output voltage ratio is a factor which affects device going PSM mode or not. Reference fig.17, as input voltage decreases, PSM/PWM boundary decreases to close 0Ma. Keep light load in PSM, V_{IN} > V_{OUT}+1V is necessary.

Inductor Selection

The value of the inductor is selected based on the desired ripple current. Large inductance gives low inductor ripple current and small inductance result in high ripple current. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current. In experience, the value is to allow the peak-to-peak ripple current in the inductor to be 10%~20% maximum load current. The inductance value can be calculated by:

$$L = \frac{(V_{IN} - V_{OUT})}{F_{OSC} * \Delta I_L} * \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{F_{OSC} * (2 * (10\% \sim 20\%) * I_{LOAD})} * \frac{V_{OUT}}{V_{IN}}$$

The inductor ripple current can be calculated by:

$$\Delta I_L = \frac{V_{OUT}}{F_{OSC} * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Choose an inductor that does not saturate under the worst-case load conditions, which is the load current plus half the peak-to-peak inductor ripple current, even at the highest operating temperature. The peak inductor current is:

$$I_{L\_PEAK} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The inductors in different shape and style are available from manufacturers. Shielded inductors are small and radiate less EMI issue. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Recommend Table

Inductor Value (μH)	Dimensions (mm)	Component Supplier	Model	ISAT (A)	DCR (Mω)
2.2	5.2 x 4.9 x 3.0 max.	CYNTEC	PCMB053T-2R2MS	9	29 typ.
2.2	4.9 x 4.9 x 4.1 typ.	TAIYO YUDEN	NRS5040T2R2NMGJ	5	28.6 typ.

Input Capacitor Selection

The input capacitor must be connected to the VIN pin and GND pin of EML3171 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage. In normal operation, the input current is discontinuous in a buck converter. The source current waveform of the high-side MOSFET is a square wave. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The RMS value of input capacitor current can be calculated by:

$$I_{RMS} = I_{LOAD\_MAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $I_{O\_MAX}/2$. A 22Mf*2ea ceramic capacitor is recommended value in typical application.

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. The output ripple is determined by:

$$\Delta V_{OUT} = \Delta I_L * \left(ESR_{COUT} + \frac{1}{8 * F_{OSC} * C_{OUT}}\right)$$

Where F_{OSC} = operating frequency, C_{OUT}= output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. A 22Mf ceramic capacitor is recommended value in typical application.

Recommend Table

Capacitor Value (μF)	Case Size	Component Supplier	Model
22	1206	TDK	C3216X5R1E226K

Using Ceramic Input and Output Capacitors

Care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush current through the long wires can potentially cause a voltage spike at V_{IN}, which may large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R or X7R specification. Their dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, VOUT immediately shifts by an amount equal to

$$\Delta I_{LOAD} * ESR_{COUT}$$

ESR is the effective series resistance of output capacitor. $\triangle I_{LOAD}$ also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Short-Circuit Protection

When EML3171 output node is shorted to GND, chip will enter soft-start to protect itself, when short circuit is removed, EML3171 enter normal operation again. If EML3171 reach OCP threshold while short circuit, EML3171 will enter soft-start cycle until the current under OCP threshold. If short circuit protection needs to work well under VIN > 5.5V, C_{IN}=22Mf x 2ea is necessary.

Over Temperature Protection

The internal high-side MOSFET is turned off when the internal thermal sensor detects that the junction temperature exceeds 165℃, entering the Over Temperature Protection mode (OTP). The OTP mode is unlocked at 130℃, i.e. a 35℃ hysteresis.

Output Voltage Setting

The output voltage of EML3171 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} * \left(1 + \frac{R_1}{R_2}\right) = 0.8 * \left(1 + \frac{R_1}{R_2}\right)$$

The resistive divider senses the fraction of the output voltage as shown in Fig.21 Using large feedback resistor can increase efficiency, but too large value affects the device's output accuracy because of leakage current going into device's FB pin. The recommended value for R2 is therefore in the range of 50KΩ.

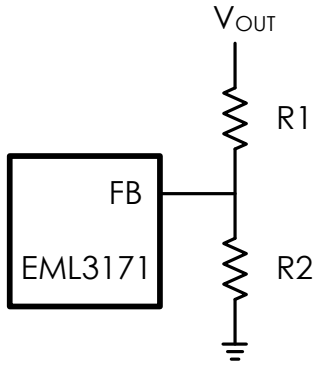


Fig. 21 Setting the Output Voltage

Under Voltage Lock Out

The under-voltage lockout (UVLO) circuitry ensures that the Eml3171 starts up with adequate voltage. The regulator output is disabled whenever VIN is below UVLO. The hysteresis of UVLO is designed to be 100 Mv.

Applications

Typical Schematic for PCB layout

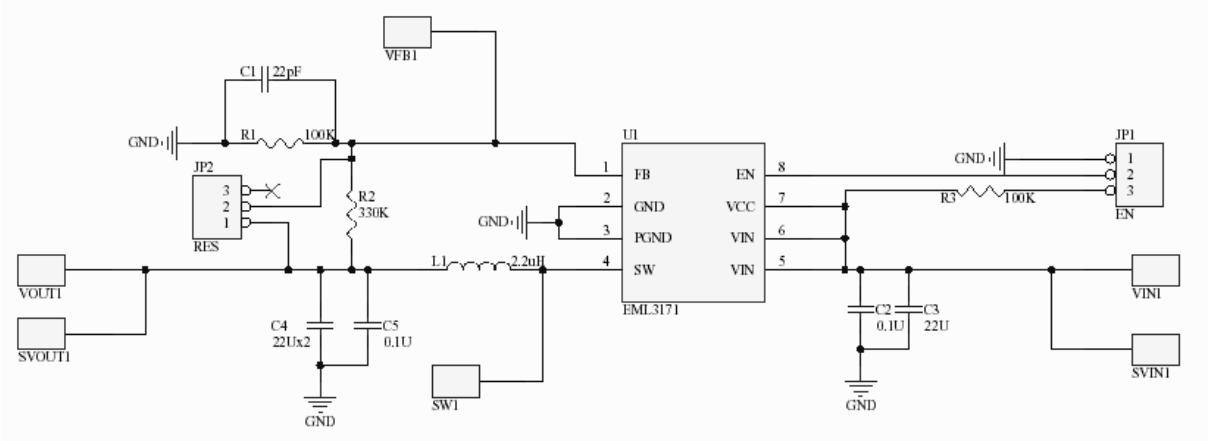


Fig. 22

PCB Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to optimize the performance of EML3171.

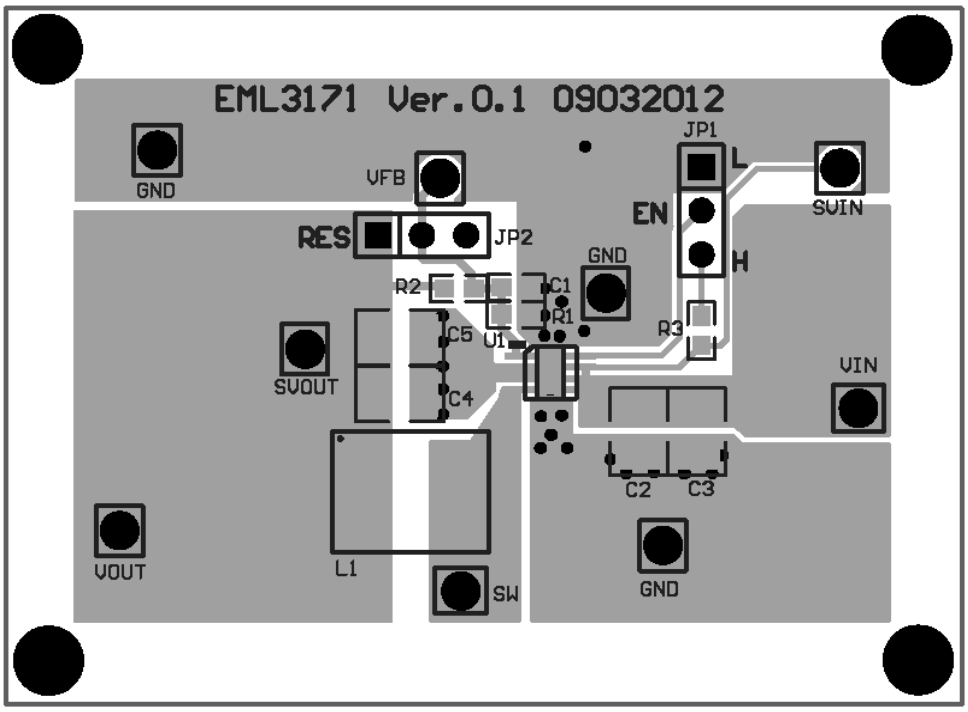
1. The power traces, including the GND trace, the SW trace and the V_{IN} trace should be kept direct, short and wide.

2. Put input capacitor as close as possible to the V_{IN} and GND pins.

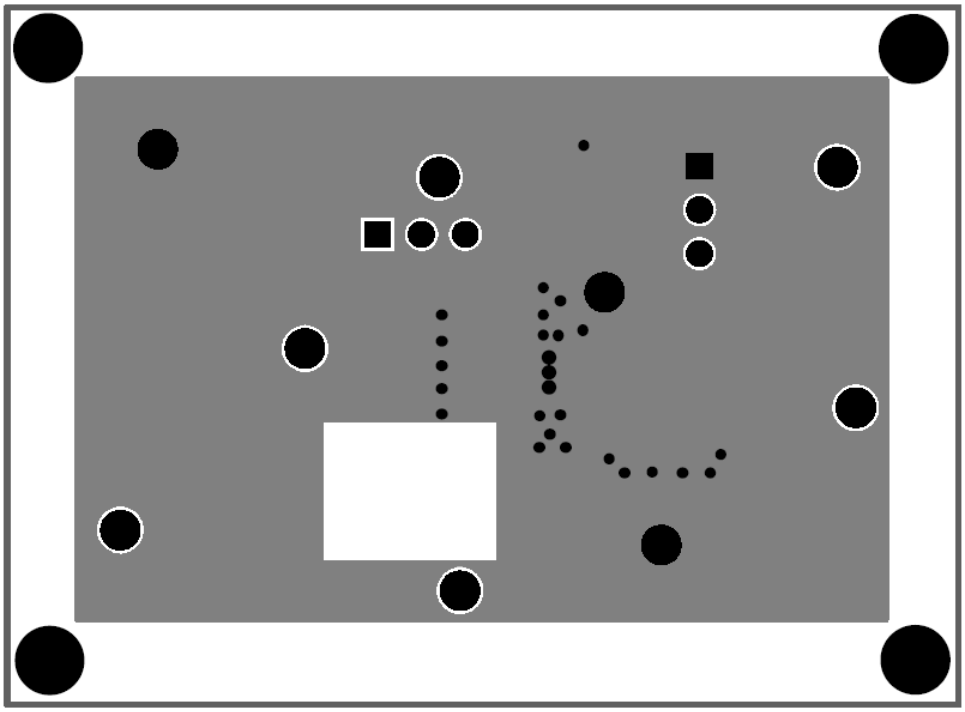
3. The FB pin should be connected directly to the feedback resistor divider.

4. Keep the switching node, SW, away from the sensitive FB pin and the node should be kept small area.

Typical Schematic for PCB layout (cont.)



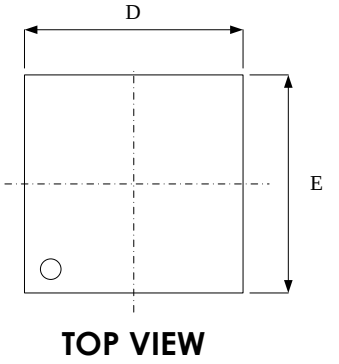
Top Layer



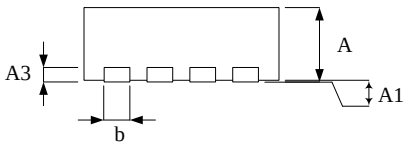
Bottom Layer

Package Outline Drawing

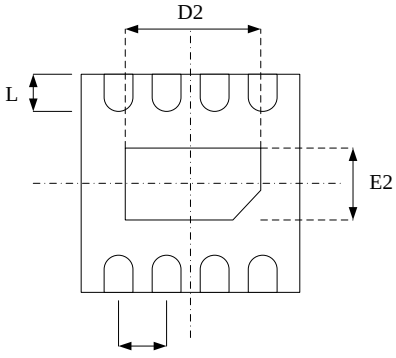
TDFN-8L (3x3 mm)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.7	0.85
A1	0	0.05
A3	0.175	0.25
b	0.25	0.35
D	2.95	3.05
E	2.95	3.05
e	0.65 BSC	
L	0.3	0.5

Exposed pad

	Dimension in mm	
Option 1	Min	Max
D2	1.60	2.50
E2	1.35	1.75
Option 2		
D2	2.20	2.40
E2	1.40	1.70

Revision History

Revision	Date	Description
0.1	2013.12.04	Initial version.
1.0	2015.03.05	Revise version to 1.0
1.1	2016.12.01	Updated the EN threshold voltage information.

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