5A, 36V, 420kHz Non-synchronous Step-Down Converter

General Description

The EML3190 is a 5A, current-mode step-down converter with an integrated high-side switch. The EML3190 operates with the wide input voltage from 4.5V to 36V and provides an adjustable output voltage from 0.808V to 30V. The EML3190 features a PWM mode operation with internally fixed 420kHz switching frequency. The EML3190 provides a single highly efficient solution with current mode control for fast loop response and easy compensation. The EML3190 also automatically enters PSM mode at light load.

Cycle-by-cycle current limiting and thermal shutdown are provided for fault condition protections. An internal 2ms soft-start design reduces input start-up current and prevents the output voltage and inductor current from overshooting during power-up.

The EML3190 requires a minimum number of external components and is available in E-SOP-8L with thermally enhanced package.

Features

- 4.5V to 36V Input Voltage Range
- 5A Continuous Output Current
- 60mΩ Internal Power MOSFET Switch
- Output Adjustable from 0.808V
- Fixed 420kHz Switching Frequency
- Synchronize up to 1.5MHz
- Power Good Indicator
- Cycle-by-Cycle Current Limit, Frequency Fold Back and thermal shutdown
- Stable with Low ESR Output Ceramic Capacitors
- 2ms Internal Soft-Start
- Thermally Enhanced E-SOP-8L Package

Applications

- 12V and 24V Distributed Power Systems
- Battery Powered Systems
- Industrial Power Systems
- LCD and Plasma TVs
- Automotive System

Typical Application

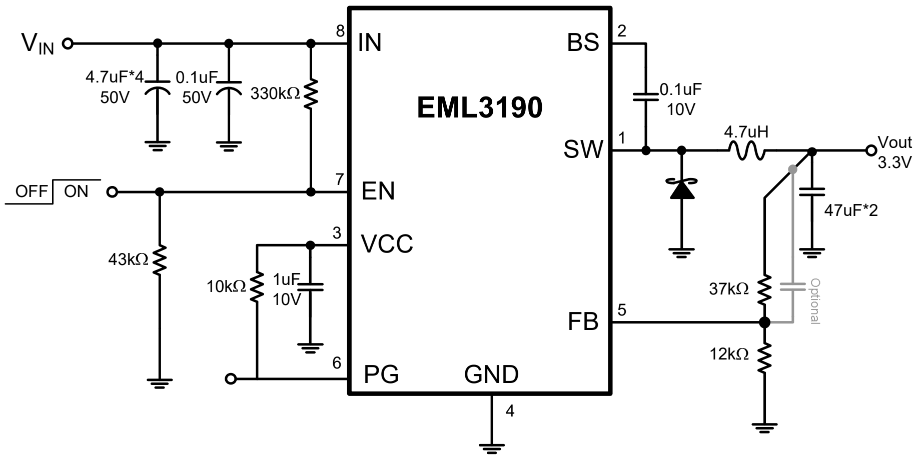
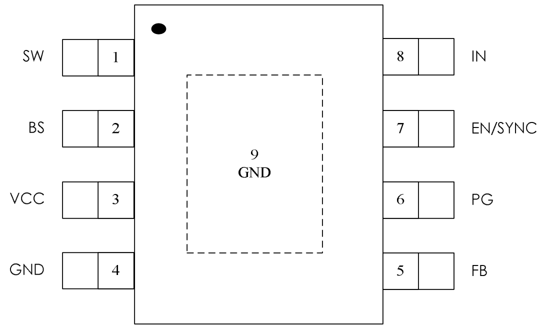


Fig. 1

Package Configuration

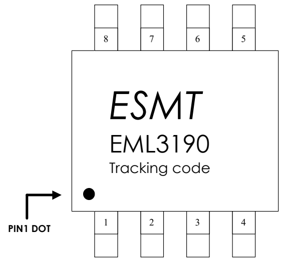


E-SOP-8L

EML3190-00SG08NRR

00	Adjustable
SG08	E-SOP-8L Package
NRR	RoHS & Halogen free package
	Commercial Grade Temperature
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Mark & Packing information

Package	Vout(V)	Product ID	Marking	Packing
E-SOP-8L	Adjustable	EML3190-00SG08NRR		Tape & Reel 3K units

Functional Block Diagram

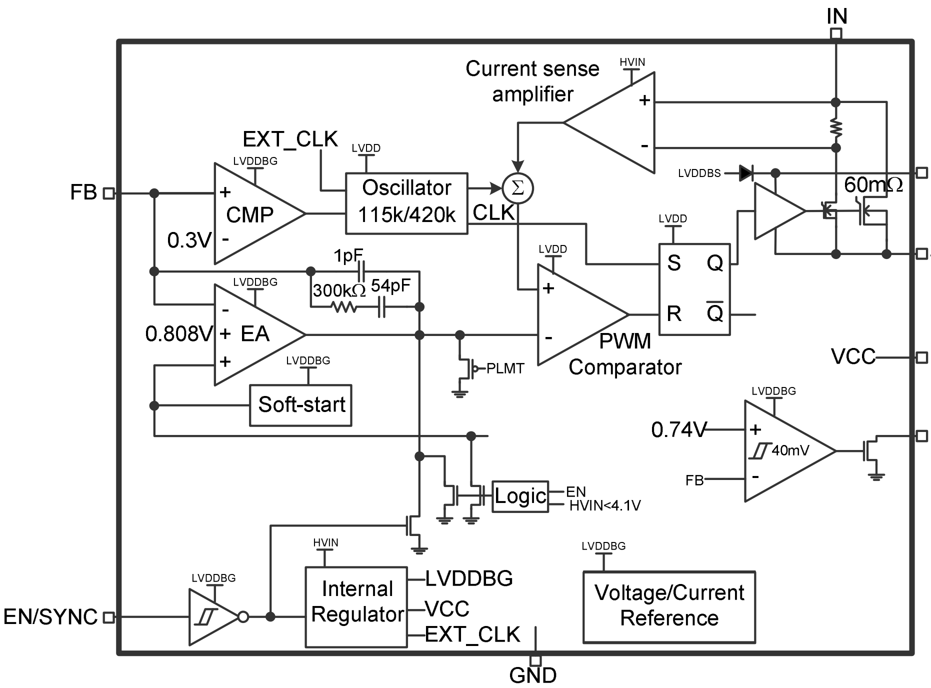


Fig. 2

Pin Functions

Pin Name	E-SOP-8L	Function
SW	**1**	**Switch Pin.** Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
BS	**2**	**Bootstrap.** A 10nF or greater capacitor must be connected from this pin to SW. It can boost the gate drive to fully turn on the internal high side NMOS.
VCC	**3**	**Bias Supply** Decouple this pin with a 1uF capacitor
GND	**4**	**Ground Pin.**
FB	**5**	**Feedback Pin.** Receives the feedback voltage from an external resistive divider across the output, it regulates at 0.808V.
PG	**6**	**Power Good Indicator.** Connect this pin to Vcc or Vout by a 100KΩ pull-up resistor.
EN/SYNC	**7**	**Enable Pin.** This pin provides a digital control to turn the converter on or off. Connect to V_{IN} with a 100KΩ resistor for self-startup.
IN	**8**	**Power Input Pin.** Drive 4.5V to 36V voltage to this pin to power on this chip. Connecting a 10uF ceramic bypass capacitor between V_{IN} and GND to eliminate noise.
GND	**9**	**Ground Pin/Thermal Pad** This Pin must be connected to ground. The thermal pad with large thermal land area on the PCB will helpful chip power dissipation.

Absolute Maximum Ratings

Devices are subjected to fail if they stay above absolute maximum ratings.

Input Voltage (IN) --------------------------------- –0.3V to +42V
Switch Voltage (SW) ------------------------- –0.3V to Vin+0.3V
Switch Voltage (SW, 10ns transient) –1.4V to Vin+0.3V
Boost Voltage (BS) ---------------------- V_{SW}-0.3V to V_{SW}+7.3V
Enable Voltage (EN) ----------------------------------- –0.3 to Vin
All Other Pins (VCC, FB, PG) ---------------------- –0.3V to +6V

Lead Temperature (Soldering, 10 sec) ---------------- 260°C
Junction Temperature (Notes 1, 3) -------- –40°C to 150°C
Storage Temperature Range --------------- – 65°C to 150°C
ESD Susceptibility HBM -------------------------------------- 2KV
MM ------------------------------------- 200V

Recommended Operating Conditions

Input Voltage(VIN) ----------------------------- +4.5V to +36V

Junction Operating Temperature Range –40°C to 125°C

Thermal data

Package	Thermal resistance	Parameter	Value
E-SOP-8L	θ_{JA} (Note 2)	Junction-to-ambient	50°C/W
	$\theta_{JC\ (top)}$(Note 3)	Junction-case (top)	39°C/W
	$\theta_{JC(bottom)}$ (Note 4)	Junction-case (bottom)	10°C/W

Electrical Characteristics

VIN=12V, T_A=+25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	4.5V≦V_{IN}≦36V	0.788	0.808	0.828	V
I_{FB}	Feedback Current	V_{FB} =0.8V		1		nA
$R_{DS(ON)}$	Switch on Resistance			60	100	mΩ
Isw	High-side Switch Leakage	V_{EN}=0V, V_{SW}=0V			10	μA
I_{LIM}	Current Limit			8.7		A
f_{OSC}	Oscillation Frequency	V_{FB}=0.6V	240	420	600	kHz
	Fold-Back Frequency	V_{FB}=0V	25	115	205	kHz
T_{ON}	Minimum On Time (note5)			100		ns
T_{OFF}	Minimum Off Time (note5)			200		ns
V_{UVLO}	Under Voltage Lock Out	Rising	3.9	4.2	4.5	V
	Under Voltage Lock Out Hysteresis			800		mV
	EN Input Low Voltage				0.4	V
	EN Input High Voltage		1.2			V
I_{EN}	Enable Input Current	V_{EN}=2V		-5		μA
		V_{EN}=0V		-1		μA
F_{SYNCL}	Sync Frequency Range(Low)			300		kHz
	Sync Frequency Range(High)			1.5		MHz
$T_{EN,Low}$	Enable Turn OFF			5		μs
T_{SD}	Thermal Shutdown			150		℃
	Thermal Shutdown Hysteresis			20		℃
I_{SD}	Shutdown Supply Current	V_{EN}=0		10	20	μA
I_Q	Quiescent Supply Current	V_{EN}=2V, No load, switching supply current		0.6	0.8	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		V_{EN}=2V, V_{FB}=1V, nonswitching supply current		0.5	0.7	mA
	Power Good Threshold Rising		0.69	0.74	0.79	V
	Power Good Threshold Hysteresis			40		mV
V_{PG}	Power Good Pin level	PG Sink 4Ma			0.4	V

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D ($T_J = T_A + (P_D) * \theta_{JA}$)).

Note 2: θ_{JA} is simulated in the natural convection at T_A=25℃ on a highly effective thermal conductivity (thermal land area completed with >3x3cm^2 area) board (2 layers , 2S0P) according to the JEDEC 51-7 thermal measurement standard.

Note 3: $\theta_{JC(top)}$ represents the heat resistance between the chip junction and the top surface of package.

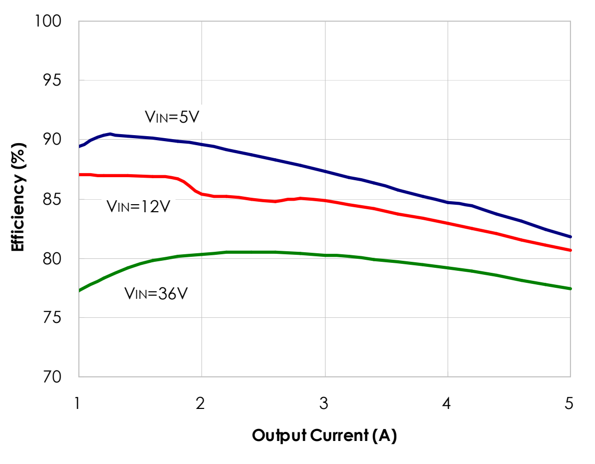
Note 4: $\theta_{JC(bottom)}$ represents the heat resistance between the chip junction and the center of the exposed pad on the underside of the package.

Note 5: Guaranteed by design.

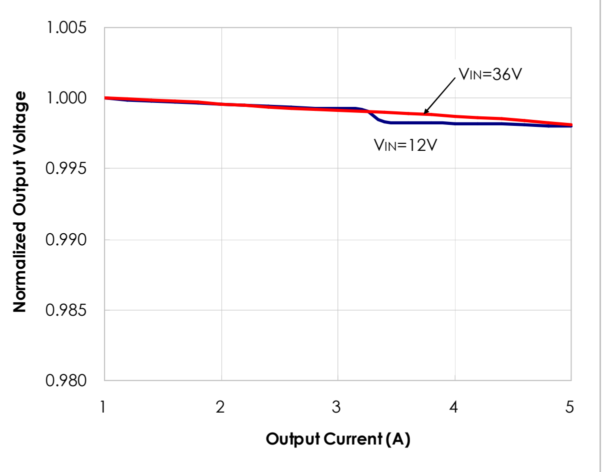
Typical Performance Characteristics

V_{IN}=12V, V_{OUT}=3.3V, T_A=25℃, unless otherwise specified.

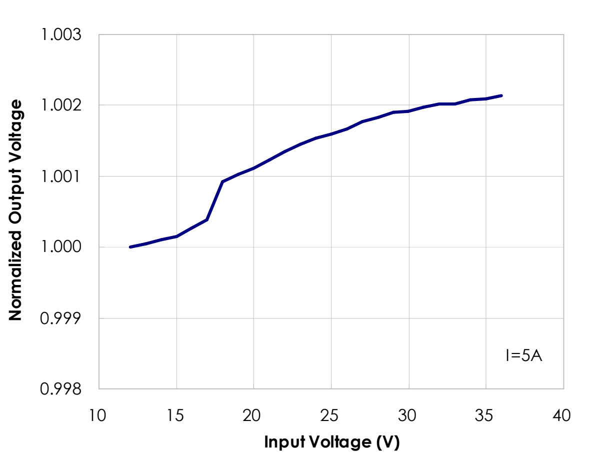
Efficiency vs. Output Current (Fig.3)



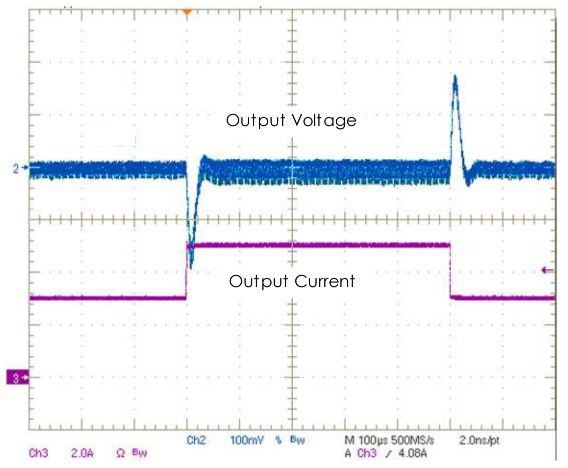
Load Regulation (Fig.4)



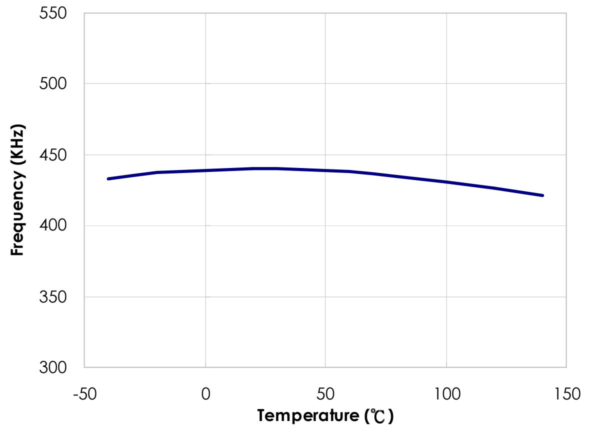
Line Regulation (Fig.5)



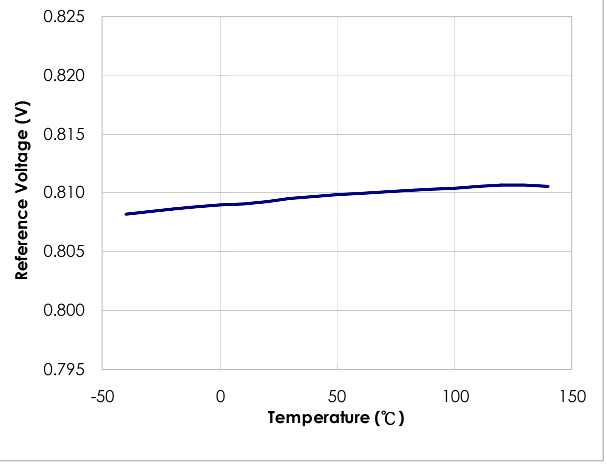
Load Transient (Fig.6)



Oscillator Frequency vs. Temperature (Fig.7)



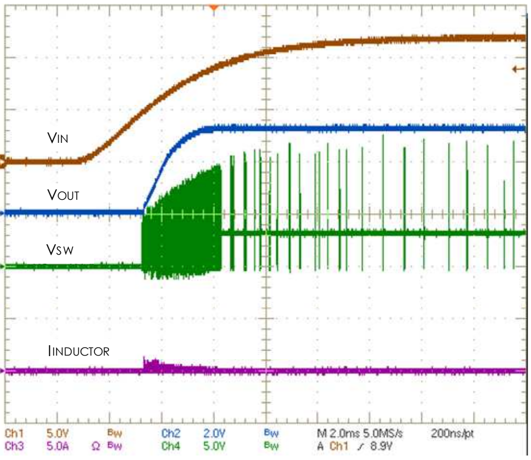
Reference Voltage vs. Temperature (Fig.8)



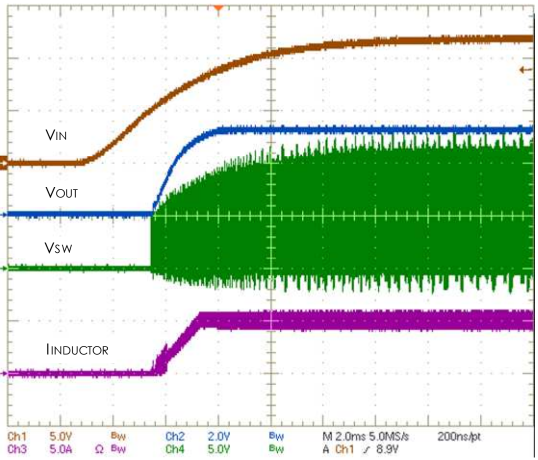
Typical Performance Characteristics

V_{IN}=12V, V_{OUT}=3.3V, T_A=25℃, unless otherwise specified.

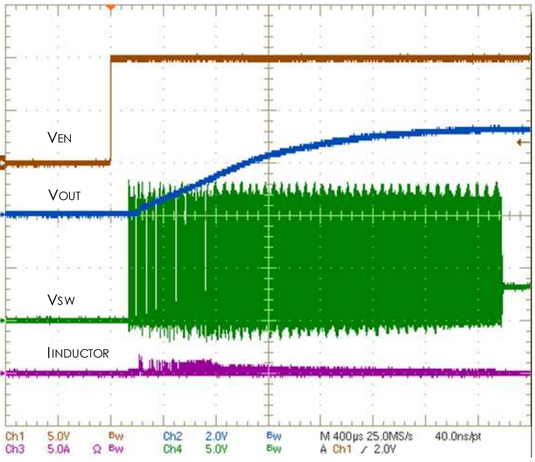
Power Up Without Load (Fig.9)



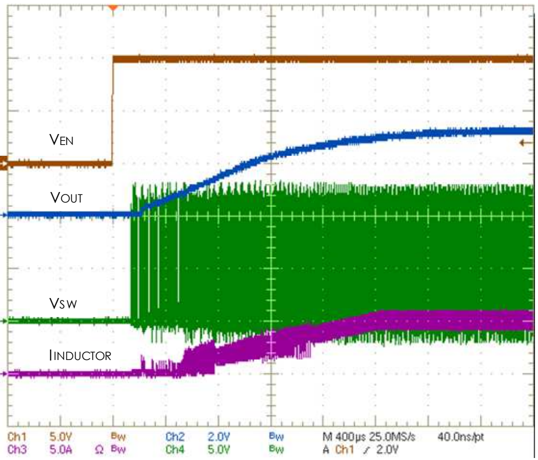
Power Up With 5A Load (Fig.10)



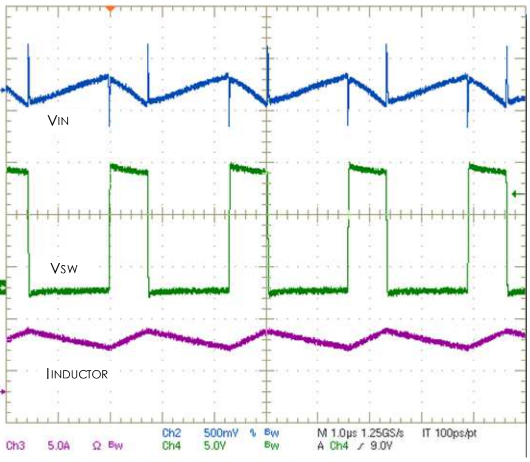
Enable Startup at No Load (Fig.11)



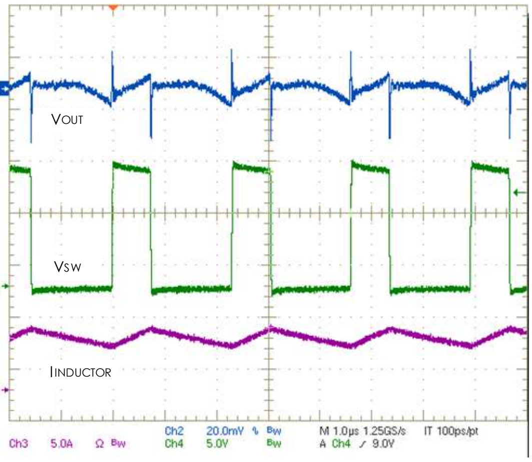
Enable Startup at Full Load (Fig.12)



Input Ripple Voltage (Fig.13)



Output Ripple Voltage (Fig.14)



Detailed Description

The EML3190 is a constant-frequency, current mode, automotive buck converter with an integrated high-side switch. The device operates with input voltages from 4.5V to 36V and tolerates input transients up to 42V. During light-load conditions, the device enters PSM automatically.

Wide Input Voltage Range (4.5V to 36V)

The EML3190 includes two separate supply inputs, IN and BS, specified for a wide 4.5V to 36V input voltage range. IN provides power to the device and BS provides power to the internal high-side switch driver.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.808V reference and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

The EML3190 includes a 5V linear regulator, VCC, which provides power to the internal circuitry. Connect a 1Uf capacitor from VCC to GND to bypass the internal LDO. Loading on this LDO is not recommended.

Power Good Indicator

Typically, a 100kΩ resistor connected between VCC or Vout and PG pin is recommended. When the FB is below 0.70V, the PG pin will be internally pulled low. When the FB is above 0.74V, The PG becomes an open-drain output.

Minimum On-Time

The device features a 100ns minimum on-time that ensures proper operation at 420kHz switching frequency and high differential voltage between the input and the output.

Enable/Sync Control

The EML3190 has a dedicated Enable/SYNC control pin. By pulling it high or low, that can be enabled and disabled. Tie EN to IN through a 100kΩ resistor for automatic start up. To disable the part, EN must be pulled low for at least 5us.

When floating, EN is pulled up to about 2.0V by an internal 1Ua current source so it is enabled. To pull it down, 1Ua current capability is needed.

The EML3190 can also be synchronized to external clock range from 300kHz up to 1.5MHz through the EN/SYNC pin. The internal clock rising edge is synchronized to the external clock rising edge.

Over-Temperature protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds 150℃, an internal thermal sensor shuts down the whole chip. The thermal sensor turns on the IC again after the junction temperature is cooled by 10℃

Under Voltage Lock-out (UVLO)

UVLO is implemented to protect the chip from operating at insufficient supply voltage. The UVLO rising threshold is about 4.2V while its falling threshold is about 3.4V. If a higher UVLO is required for a specified application, as the EN pin shown in Fig.15 below to adjust input voltage UVLO via two external resistors and a filter capacitor.

The EN enable threshold is around 1.0V (EN_{ON}), and with 100mV hysteresis window (EN_{OFF}) for shutdown. An internal pull-up current source I_E (0.9uA) is in default operating when EN pin floats. Once the EN pin voltage exceed the EN_{ON}, an additional 2.9 μA of hysteresis, I_H, is added. This additional current facilitates adjustable input voltage UVLO hysteresis. Use Equation (a) to set the external UVLO hysteresis voltage. Use Equation (b) to set the external UVLO start voltage. For example, choosing R_3=330kΩ and R_4=43kΩ, the external UVLO V_{UVLO_start} and V_{UVLO_stop} would be around 9V and 7V.

$$R_3 = \frac{V_{UVLO\_start} - k \cdot V_{UVLO\_stiop}}{k \cdot 3.8u - 0.9u} \text{..(a)}$$

$$R_4 = \frac{EN_{on}}{\frac{V_{UVLO\_start} - EN_{on}}{R_3} + 0.9u} \text{..(b)}$$

$$k = \frac{EN_{on}}{EN_{off}} = 1.1$$

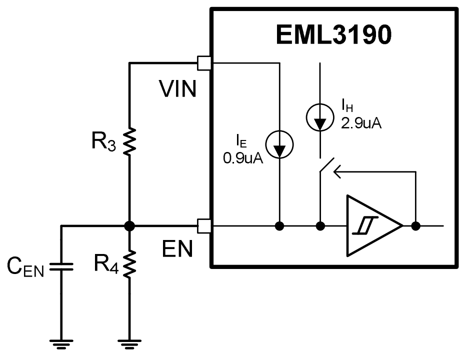


Fig.15 External UVLO Lock-out

Boost Capacitor

Connect a 1Uf capacitor between the BS pin and SW pin. This capacitor provides the gate driver voltage for the high-side MOSFET. Also, an UVLO in the floating supply is implemented to protect the high-side MOSFET and its driver from operating at insufficient supply voltage. The UVLO rising threshold is about 2.2V while its hysteresis is about 0.16V.

Over-Current protection

Over-current limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the over-current threshold limit. If the drain-to-source voltage exceeds the over-current threshold limit, the over-current indicator is set true. Once over-current indicator is set true, over-current limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle. The output voltage will start to drop if the output is dead-short to ground, suddenly. Once the FB is lower than 0.3V, the EML3190 is restarted periodically till the dead-short event is removed.

Application Information

The schematic on the front page shows a typical application circuit. The EML3190 can provide up to 5A output current at a 3.3V output voltage. For proper thermal performances, the exposed pad of the device must be soldered down to the PCB. With the optimized internal compensation network, minimize the external component counts and simplify the control loop design.

Setting the Output Voltage

The external resistor divider is not only used to set the output voltage, but also sets the system loop bandwidth with the internal compensation capacitor. The R1 should be chosen around 40.2kΩ for better transient performance, and the R2 is then derived by:

$$R_2 = R_1 \cdot \frac{0.808V}{V_{OUT} - 0.808V}$$

Table1-Resistor Selection for Common Output Voltages

Vout	R1 (kΩ)	R2 (kΩ)
1.8V	33.1 (1%)	27 (1%)
2.5V	50.3 (1%)	24 (1%)
3.3V	37 (1%)	12 (1%)
5.0V	62.3 (1%)	12 (1%)

Selecting the Inductor

The common rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be between 20% and 40% of the DC maximum load current, typical 30%. And also have sufficiently high saturation current rating and a DCR as low as possible. Generally, it is desirable to have lower inductance in switching power supplies, because it usually corresponding to faster transient response, smaller DCR and reduced size for more compact designs. But too low of an inductance results in higher ripple current such that over-current protection at full load could be falsely triggered. Also, the output ripple voltage and efficiency become worse with lower inductance. Under light load condition, like below 100Ma, larger inductance is recommended for improved efficiency. The inductance and its peak current could be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$I_{LP} = I_{LOAD} + \frac{\Delta I_L}{2} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Which f_S is the switching frequency; I_{LOAD} is the load current.

Selecting the Input capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current for step-down converter to maintain the DC input voltage. Use low ESR capacitor for the best performance. The high frequency impedance of the capacitor should be lower than the input source impedance for bypassing the high frequency switching current locally. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To prevent excessive voltage ripple at input, the relationship between the input ripple and the capacitance could be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C_1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Diode

The diode connected between SW and GND is the path for the inductor current during the high-side MOSFET turns off. Choose the diode with minimum forward voltage drop and recovery time, like Schottky. And, the reverse voltage rating is greater than maximum input voltage and whose current rating is greater than the maximum load current.

Table2-Diode Selection Guide

Diode	Voltage/Current Rating	Manufacture
B540C	40V, 5A	Diodes Inc.

Selecting the Output capacitor

The output capacitor (C2) is required to maintain the DC output voltage, keeps the output ripple small, and ensures regulation loop stability. The lower ESR capacitors are preferred to keep lower output ripple. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right)$$

Which L is the inductance and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

In case of lower ESR capacitor adopted, the output ripple is mainly caused by the capacitance and the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

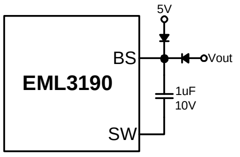
Or, the ESR dominates the impedance at switching frequency. After simplification, the output voltage ripple can approximated to

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the loop stability of regulation system. Low ESR ceramic capacitors with X5R or X7R dielectrics are recommended.

External Bootstrap Diode

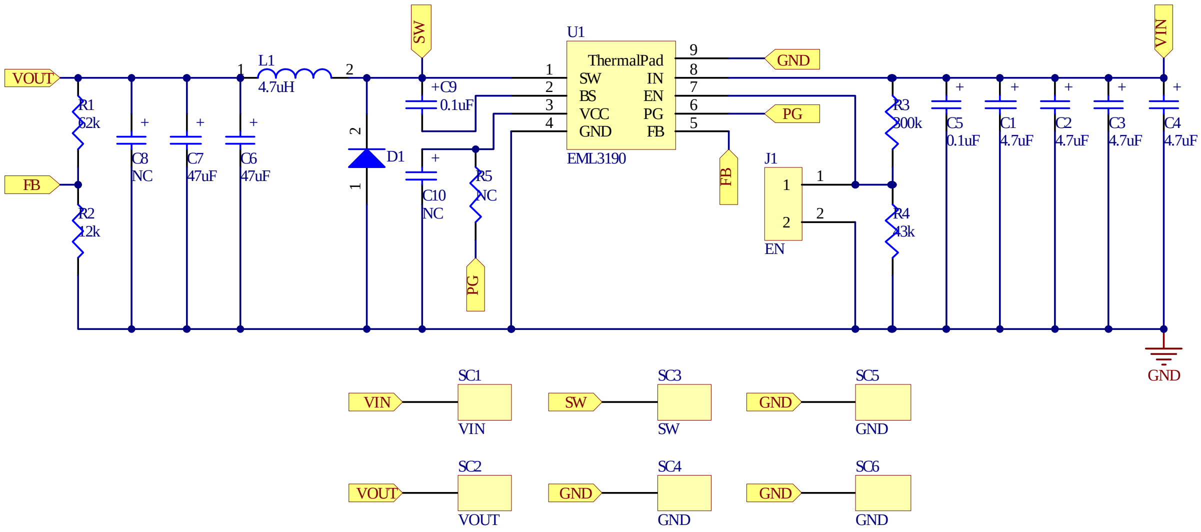
An external bootstrap diode is recommended to add between external 5V and BS pin to enhance efficiency of the regulator. The external 5V can be a 5V fixed input from system or a 5V output of the EML3190. The low cost diode, like 1N4148, is sufficient.



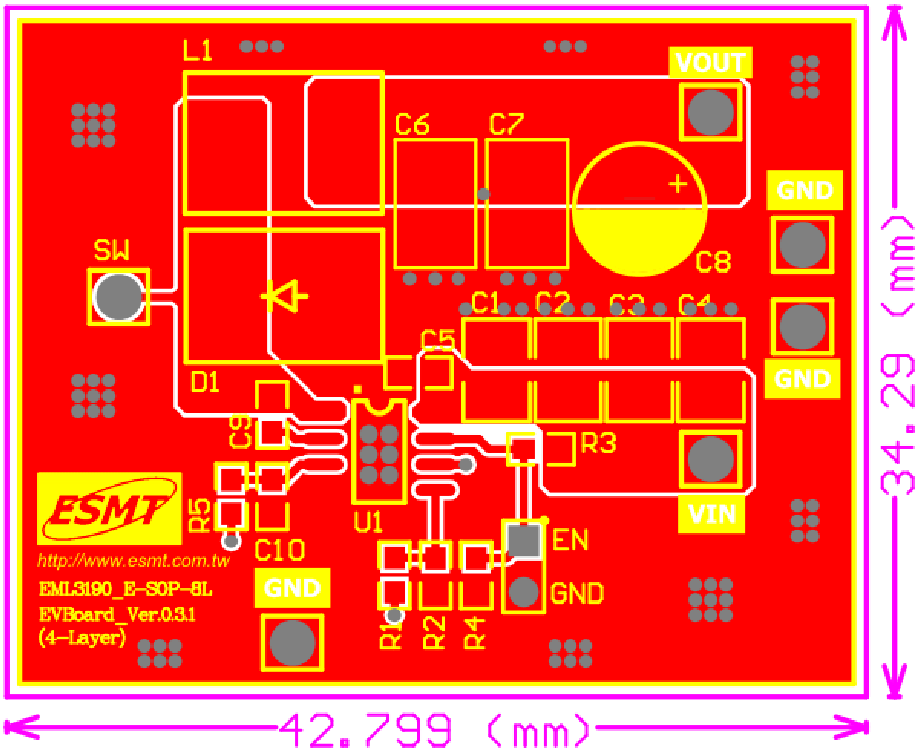
With such diode, 5V input voltage can output 3.3V and 2.5V with just 30Ma load.

Applications

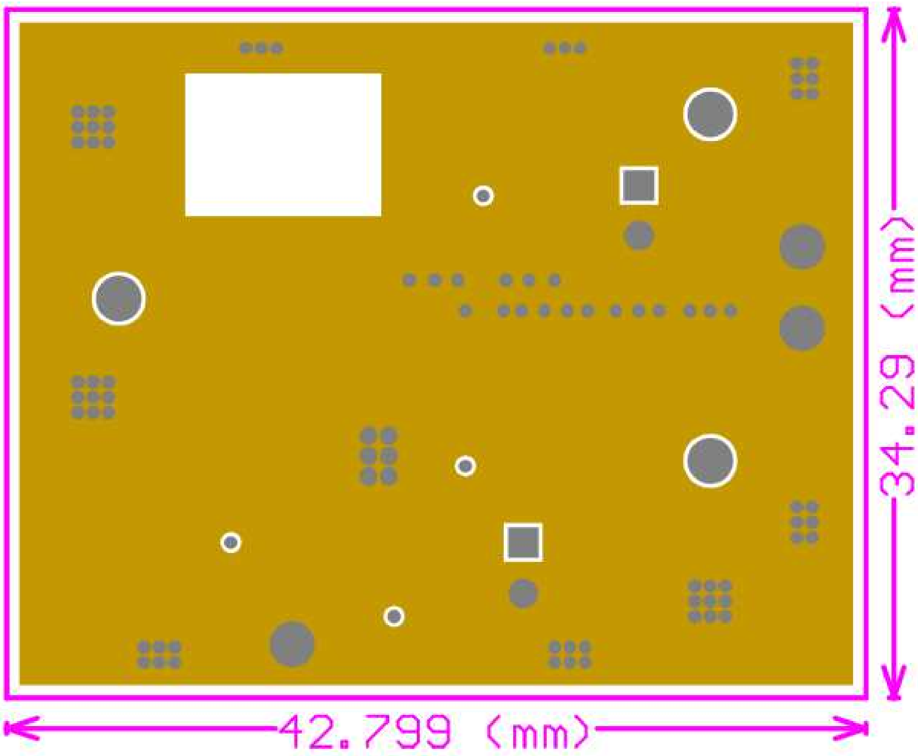
Typical schematic for PCB layout



Typical schematic for PCB layout (cont.)

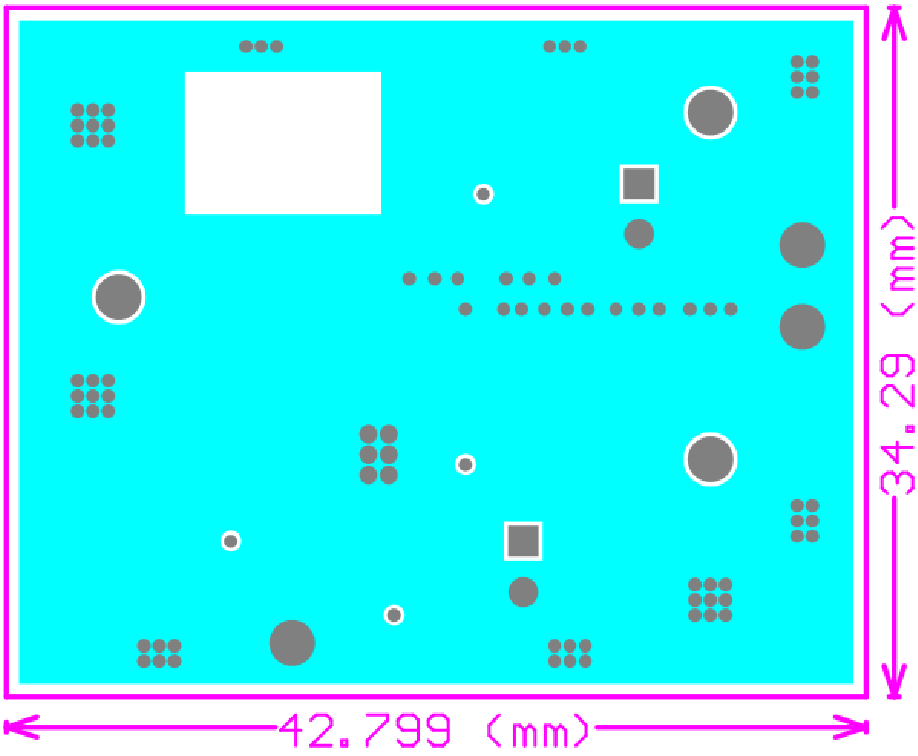


Top-side Layout

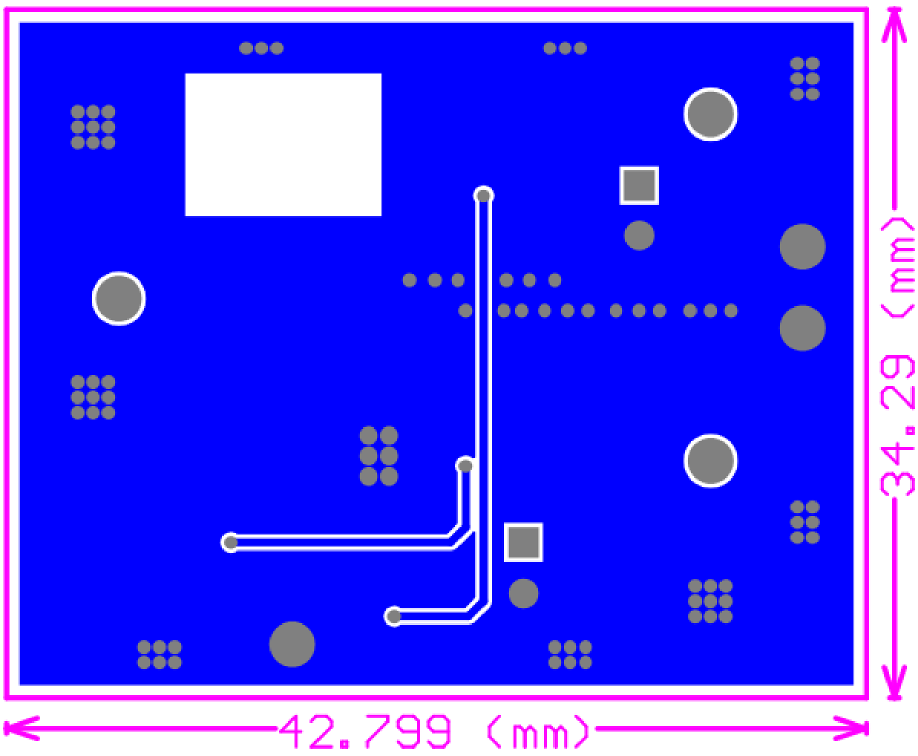


Layer 2 Layout

Typical schematic for PCB layout (cont.)

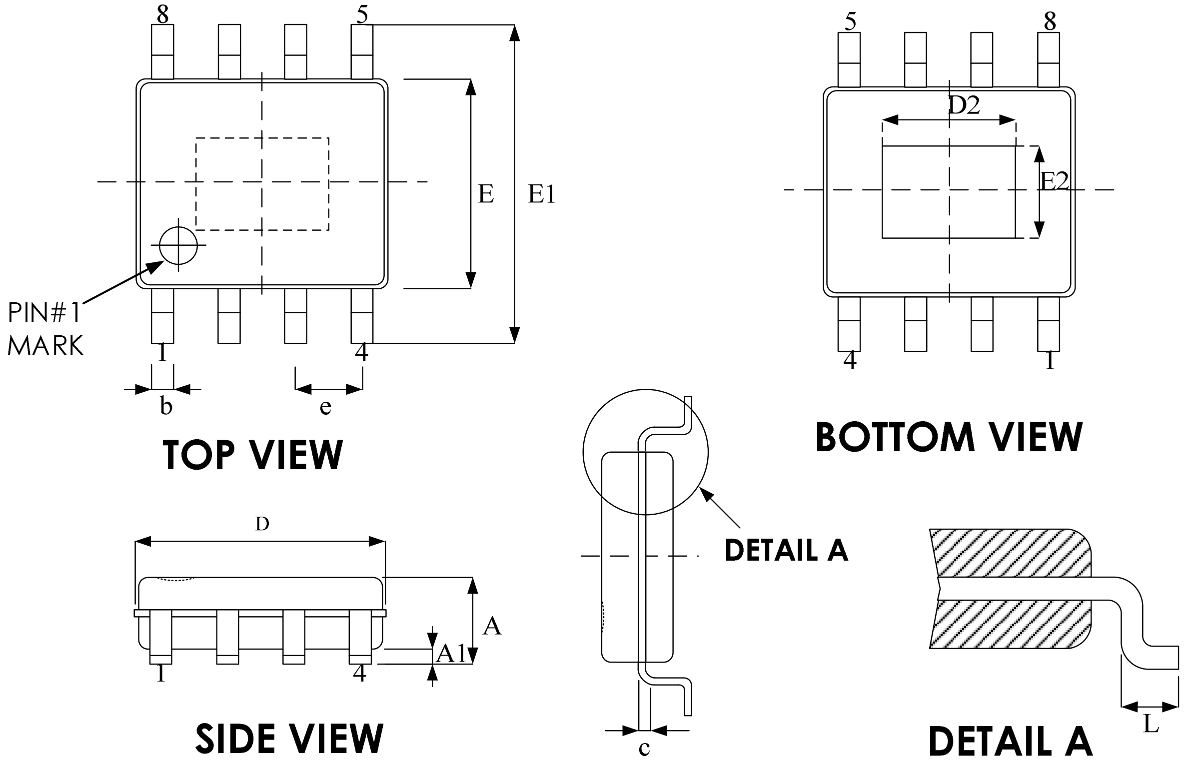


Layer 3 Layout



Bottom-side Layout

Package Outline Drawing
E-SOP-8L (150 mil)



Symbol	Dimension in mm	
	Min	Max
A	-	1.70
A1	0.00	0.15
b	0.31	0.51
c	0.10	0.25
D	4.80	5.00
E	3.81	4.00
E1	5.79	6.20
e	1.27 BSC	
L	0.40	1.27

Exposed pad

	Dimension in mm	
	Min	Max
D2	2.80	3.50
E2	2.00	2.60

Revision History

Revision	Date	Description
0.1	2015.12.09	Initial version.
1.0	2015.12.31	Remove preliminary word and modify version to 1.0
1.1	2016.02.01	Modified the Absolute Maximum Ratings.
1.2	2016.04.19	1. Updated the typical application circuit. 2. Updated the functional block diagram. 3. Updated the detailed description of UVLO control. 4. Updated the PCB schematic.
1.3	2016.05.12	Updated Package Outline Drawing
1.4	2016.06.06	Added the Recommended Operating Conditions.
1.5	2016.07.11	Modified the thermal parameter.
1.6	2016.10.07	1. Updated the typical application circuit. 2. Update the EN threshold spec. in electrical characteristics. 3. Updated the detailed description of UVLO control. 4. Updated the typical schematic for PCB layout.
1.7	2017.02.20	1. Modify marking information. 2. Updated the quiescent current information in electrical characteristics.
1.8	2021.07.14	Modify E-SOP-8 Dimension
1.9	2022.06.16	Update AMR SW and BS spec.