EMP202

Single-Chip Dual-Channel AC'97 Audio Codec for PC Audio Systems

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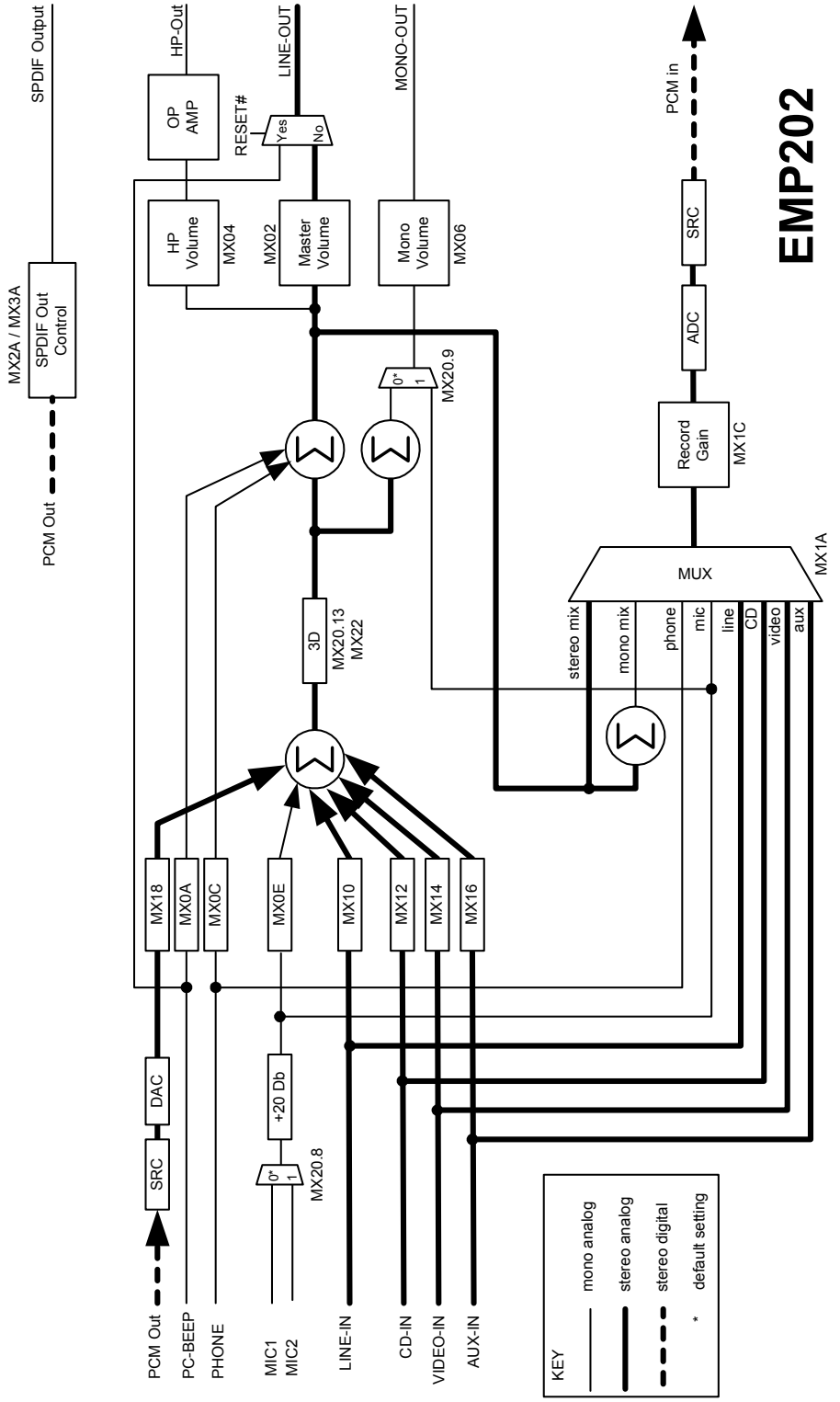
Features

- **High performance CODEC with high S/N ratio (>90 dB).**
- **Compliant with AC'97 2.2 specifications**
- **20-bit stereo Digital-to-Analog Converter with variable sampling rate.**
- **20-bit stereo Analog-to-Digital Converter with variable sampling rate.**
- **4 analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, VIDEO, AUX.**
- **2 analog line-level mono inputs: PC_BEEP, PHONE_IN.**
- **Mono output with 5-bit volume control.**
- **Stereo output with 5-bit volume control.**
- **2 MIC inputs are software selectable.**
- **Power management capabilities.**
- **3D Stereo Enhancement**
- **Embedded 50mW/20 Ω OP at LINE output.**
- **External amplifier power down capability.**
- **Digital S/PDIF output.**
- **Built in 14.318M 24.576MHz PLL to save external 24.576MHz crystal**
- **Supports 2 general-purpose I/O pins.**
- **Power supply: Digital: 3.3V; Analog: 5V/3.3V**
- **Standard 48-Pin LQFP Package**

1. General Description

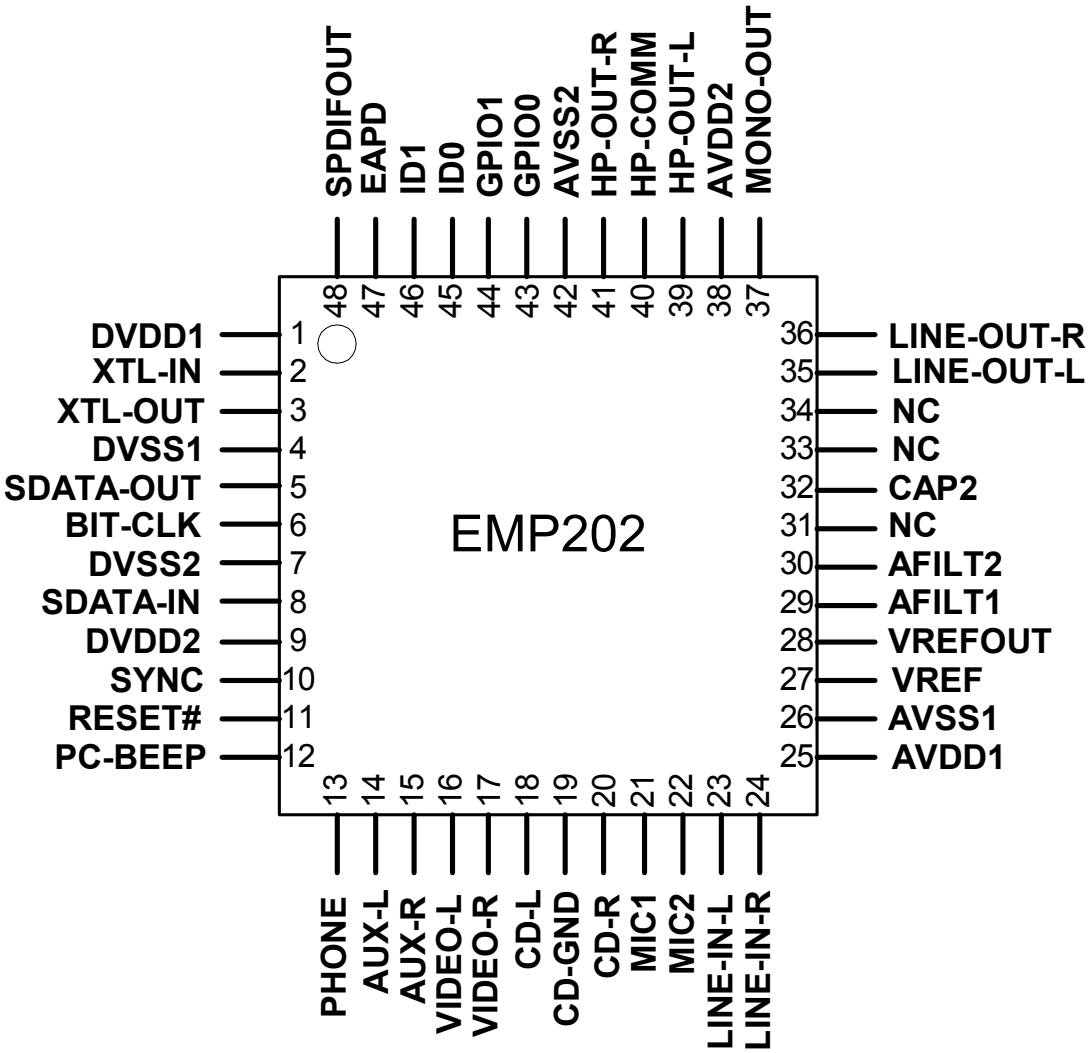
The EMP202 is a 2 channel, 20-bit DAC and 20-bit ADC, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including soft/host audio and riser card based designs. The EMP202 incorporates proprietary converter technology. The EMP202 AC'97 CODEC supports with independent variable hardware sampling rates. The EMP202 CODEC provides two pairs of stereo outputs with independent volume controls, a mono output, a headphone output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The EMP202 CODEC operates from a 3.3V power supply with EAPD (External Amplifier Power Down) control for use in notebook and PC applications. To save BOM costs, the EMP202 integrates a 50mW/20 Ω headset audio amplifier into the CODEC with Headphone Output. The EMP202 also supports an AC'97 2.2 compliant SPDIF out function which allows easy connection from the PC to consumer electronic products. The EMP202 CODEC supports soft/host audio from Intel 810/815/820/845 chipsets as well as audio controller based VIA/SIS/ALI chipsets. Windows WDM drivers that support Win95/98.ME/2K/NT and XP provide a complete solution. Finally, internal PLL circuits generate required timing signals, eliminating the need for external clocking devices.

2. Block Diagram



Mixer Functional Diagram

3. Pin Assignments



Pin Assignment Diagram

4. Pin Description

4.1. Digital I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
RESET#	I	11	AC'97 master H/W reset	Schmitt input, vL=0.3Vdd, vH=0.4Vdd
XTL-IN	I	2	Crystal input pad (24.576Mhz)	Crystal input pad
XTL-OUT	O	3	Crystal output pad	Crystal output pad
SYNC	I	10	Sample Sync (48Khz)	Schmitt input, vL=0.3Vdd, vH=0.4Vdd
BIT-CLK	IO	6	Bit clock output (12.288Mhz)	CMOS input/output, Vt=0.35Vdd, internal pull low by a 100K resistor.
SDATA-OUT	I	5	Serial TDM AC'97 output	Schmitt input, vL=0.3Vdd, vH=0.4Vdd
SDATA-IN	O	8	Serial TDM AC'97 input	CMOS output, internal pull low by a 100K resistor.
GPIO0	I/O	43	General Purpose Input/Output	Digital input/output
GPIO1	I/O	44	General Purpose Input/Output	Digital input/output
ID1	I	46	XTAL Elim Select	Digital input
ID0	I	45	XTAL Elim Select	Digital input
EAPD	I/O	47	External Amplifier power down control/GPIO	Digital output
SPDIFOUT	O	48	S/PDIF output	Digital output

TOTAL: 13 Pins

4.2. Analog I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
PC-BEEP	I	12	PC speaker input	Analog input (1Vrms)
PHONE	I	13	Speaker phone input	Analog input (1Vrms)
AUX-L	I	14	AUX Left channel	Analog input (1Vrms)
AUX-R	I	15	AUX Right channel	Analog input (1Vrms)
VIDEO-L	I	16	Video audio Left channel	Analog input (1Vrms)
VIDEO-R	I	17	Video audio Right channel	Analog input (1Vrms)
CD-L	I	18	CD audio Left channel	Analog input (1Vrms)
CD-GND	I	19	CD audio analog GND	Analog input (1Vrms)
CD-R	I	20	CD audio Right channel	Analog input (1Vrms)
MIC1	I	21	First Mic input	Analog input (1Vrms)
MIC2	I	22	Second Mic input	Analog input (1Vrms)
LINE-L	I	23	Line-In Left channel	Analog input (1Vrms)
LINE-R	I	24	Line-In Right channel	Analog input (1Vrms)
LINE-OUT-L	O	35	Line-Out Left channel	Analog output (1Vrms ~ 1.7Vrms)
LINE-OUT-R	O	36	Line-Out Right channel	Analog output (1Vrms ~ 1.7Vrms)
MONO-OUT	O	37	Speaker Phone output	Analog output (1Vrms)
HP-OUT-L	O	39	Headphone Out Left channel	Analog output (1Vrms)
HP-COMM	O	40	Headphone Ground Return	Analog output (1Vrms)
HP-OUT-R	O	41	Headphone Out Right channel	Analog output (1Vrms)

TOTAL: 19 Pins

4.3. Filter/References

Name	Type	Pin No	Description	Characteristic Definition
VREF	O	27	Reference voltage	Analog output
VREFOUT	O	28	Ref. voltage out with 5mA drive	Analog output
AFILT1	O	29	ADC left anti-aliasing filter capacitor	Analog output
AFILT2	O	30	ADC right anti-aliasing filter capacitor	Analog output
CAP2	O	32	ADC reference Cap	Analog output
NC	-	31,33,34	No Connect	

TOTAL: 8 Pins

4.4. Power/Ground

Name	Type	Pin No	Description	Characteristic Definition
AVDD1	I	25	Analog VDD (5.0V)	The minimum value is 3.0V, the maximum value is 5.5V
AVDD2	I	38	Analog VDD (5.0V)	The minimum value is 3.0V, the maximum value is 5.5V
AVSS1	I	26	Analog GND	
AVSS2	I	42	Analog GND	
VDD1	I	1	Digital VDD (3.3V)	The minimum value is 3.0V (DVdd-0.3), the maximum value is 3.6V (DVdd+0.3)
VDD2	I	9	Digital VDD (3.3V)	The minimum value is 3.0V (DVdd-0.3), the maximum value is 3.6V (DVdd+0.3)
VSS1	I	4	Digital GND	
VSS2	I	7	Digital GND	

TOTAL: 8 Pins

4.5. Crystal Selection

XTL-OUT Status	ID1 Config	ID0 Config	Input Clock Source
XTAL connected	Float	Float	24.576MHz XTAL
XTAL connected or open	Float	Pulldown	12.2888MHz BIT-CLK
XTAL connected or open	Pulldown	Float	12.2888MHz BIT-CLK
XTAL connected or open	Pulldown	Pulldown	12.2888MHz BIT-CLK
XTAL shorted to GND	Float	Float	14.31818MHz Source
XTAL shorted to GND	Float	Pulldown	27MHz Source
XTAL shorted to GND	Pulldown	Float	48MHz Source
XTAL shorted to GND	Pulldown	Pulldown	24.576MHz Source

5. Registers

Access to registers with an odd number will return a 0. Reading unimplemented registers will also return a 0.

REG. (HEX)	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6A90h
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04H	HEADPHONE Volume	Mute	X	X	HPL4	HPL3	HPL2	HPL1	HPL0	X	X	X	HPL4	HPL3	HPL2	HPL1	HPL0	8000h
06h	Mono-Out Volume	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PB3	PB2	PB1	PB0	X	0000h
0Ch	PHONE Volume	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-In Volume	Mute	X	X	NL4	NL3	NL2	NL1	NL0	X	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Volume	Mute	X	X	CL4	CL3	CL2	CL1	CL0	X	X	X	CR4	CR3	CR2	CR1	CR0	8808h
14h	Video Volume	Mute	X	X	VL4	VL3	VL2	VL1	VL0	X	X	X	VR4	VR3	VR2	VR1	VR0	8808h
16h	Aux Volume	Mute	X	X	AL4	AL3	AL2	AL1	AL0	X	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Out Volume	Mute	X	X	PL4	PL3	PL2	PL1	PL0	X	X	X	PR4	PR3	PR2	PR1	PR0	8808h
1Ah	Record Select	X	X	X	X	X	LRS2	LRS1	LRS0	X	X	X	X	X	RRS2	RRS1	RRS0	0000h
1Ch	Record Gain	Mute	X	X	X	LRG3	LRG2	LRG1	LRG0	X	X	X	X	RRG3	RRG2	RRG1	RRG0	8000h
20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2			0000h
26h	Power Down Ctrl/Status	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	X	X	REV1	REV0	AMAP	X	X	X	X	DSA1	DSA0	SPDIF	X	VRA	0605h
2Ah	Extended Audio Status	X	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0400h
2Ch	PCM Out Sample Rate	FSR 15	FSR1 4	FSR1 3	FSR1 2	FSR1 1	FSR1 0	FSR9	FSR8	FSR7	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0	BB80h
32h	PCM Input Sample Rate	ISR 15	ISR 14	ISR 13	ISR 12	ISR 11	ISR 10	ISR 9	ISR 8	ISR 7	ISR 6	ISR 5	ISR 4	ISR 3	ISR 2	ISR 1	ISR 0	BB80h
3Ah	S/PDIF Ctl	V	DRS	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO	2000h
3Eh	Ext'd Modem Stat/Ctrl	X	X	X	X	X	X	X	PRA	X	X	X	X	X	X	X	GPIO	0100h
4Ch	GPIO Pin Config	X	X	X	X	X	X	X	X	X	X	X	X	X	X	GC1	GC0	0300h
4Eh	GPIO Pin Polarity/Type	X	X	X	X	X	X	X	X	X	X	X	X	X	X	GP1	GP0	FFFFh
50h	GPIO Pin Sticky	X	X	X	X	X	X	X	X	X	X	X	X	X	X	GS1	GS0	0000h
52h	GPIO Mask	X	X	X	X	X	X	X	X	X	X	X	X	X	X	GW1	GW0	0000h
54h	GPIO Pin Status	X	X	X	X	X	X	X	X	X	X	X	X	X	X	GI1	GI0	0000h
6Ah	SPDIF Output Select	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DO1	X	0000h
72h	Antipop	X	X	X	X	X	X	X	X	APOP	X	X	X	X	X	X	X	0000H
74h	EAPD/GPIO Access	EAPD	X	X	X	EAPD OEN	X	X	X	X	X	X	X	X	INTDIS	GPIO ACC	GPIO SLT12	0800H
7Ch	Vendor ID1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFh
7Eh	Vendor ID2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFFh

X: Reserved bit

5.1. Mixer Registers

5.1.1. MX00 Reset

Default: 6A90H

Writing any value to this register will start a register reset, and causes all of the registers to revert to their default values. The written data is ignored. Reading this register returns the ID code of the specific part.

Bit	Type	Function
15	-	Reserved
14:10	R	3D Code
9	R	Read as 1 (Support 20-bit ADC)
8	R	Read as 0
7	R	Read as 1 (Support 20-bit DAC)
6	R	Read as 0 (Support 18-bit DAC)
5	R	Read as 0 (No Loudness support)
4	R	Read as 1 (Support Headphone output)
3	R	Read as 0 (No simulated stereo, for analog 3D block use)
2	R	Read as 0 (No Bass & Treble Control)
1	R	Read as 0 (No Modem Line support)
0	R	Read as 0 (No Dedicated Mic PCM input channel)

5.1.2. MX02 Master Volume

Default: 8000H

These registers control the overall volume level of the output functions. Each step on the left and right channels corresponds to 1.5dB in increase/decrease in volume.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:13	-	Reserved
12:8	R/W	Master Left Volume: (ML[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	Master Right Volume: (MR[4:0]) in 1.5 dB steps

1) For MR/ML: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

2) MR/ML are 5-bit R/W variables. The 6th bit implementation is optional. For this reason, when the 6th bit is written with a 1, it is the equivalent to writing the low 5-bits with 1. For example, writing 1xxxxx will read back 01111.

5.1.3. MX04 Headphone Volume

Default: 8000H

These registers control the overall volume level of the output functions. Each step on the left and right channels corresponds to 1.5dB in increase/decrease in volume.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:13	-	Reserved
12:8	R/W	Headphone Left Volume: (HPL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	Headphone Right Volume: (HPR[4:0]) in 1.5 dB steps

1) For HPL/HPR: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

2 HPL/HPR are 5-bit R/W variables. The 6th bit implementation is optional. For this reason, when the 6th bit is written with a 1, it is the equivalent to writing the low 5-bits with 1. For example, writing 1xxxxx will read back 01111.

5.1.4. MX06 MONO_OUT Volume

Default: 8000H

Mono output is the same data sent on all output channels. Each step in bits 4:0 corresponds to 1.5dB in increase/decrease in volume, allowing 32 levels of volume from 00000 to 11111.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:5	-	Reserved
4:0	R/W	Mono Master Volume: (MM[4:0]) in 1.5 dB steps

1) For MM: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

2) Implements 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and will respond, when read, with x11111.

5.1.5. MX0A PC BEEP Volume

Default: 8000H

This register controls the input volume for the PC beep signal. Each step in bits 4:1 corresponds to a 3dB increase/decrease in volume. 16 levels of volume are available, from 0000 to 1111.

The purpose of this register is to allow the PC Beep signals to pass through the EMP202, eliminating the need for an external system speaker/buzzer. The PC BEEP pin is directly routed (internally hardwired) to the LINE-OUTL & R pins. If the PC speaker/buzzer is eliminated, it is recommended to connect the external speakers at all times so the POST codes can be heard during reset.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:5	-	Reserved
4:1	R/W	PC Beep Volume: (PB[3:0]) in 3 dB steps
0	-	Reserved

1) For PB: 00h 0 dB attenuation
0Fh 45 dB attenuation

5.1.6. MX0C PHONE Volume

Default: 8008H

Register 0Ch controls the telephone input volume for software modem applications. Because software modem applications may not have a speaker, the CODEC can offer a speaker-out service. Each step in bits 4:0 corresponds to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:5	-	Reserved
4:0	R/W	Phone Volume: (PV[4:0]) in 1.5 dB steps

1) For PV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

5.1.7. MX0E MIC Volume

Default: 8008H

Register 0Eh controls the microphone input volume. Each step in bits 4:0 corresponds to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111. Each step in bit 6 corresponds to a magnification of 20dB increase in volume.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:7	-	Reserved
6	R/W	Mic Boost 0 0dB 1 20dB
5	-	Reserved
4:0	R/W	Mic Volume: (MV[4:0]) in 1.5 dB steps

1) For MV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

5.1.8. MX10 LINE_IN Volume

Default: 8808H

Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:13	-	Reserved
12:8	R/W	Line-In Left Volume: (NL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	Line-In Right Volume: (NR[4:0]) in 1.5 dB steps

1) For NL/NR: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

5.1.9. MX12 CD Volume

Default: 8808H

Each step in bits 44:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:13	-	Reserved
12:8	R/W	CD Left Volume: (CL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	CD Right Volume: (CR[4:0]) in 1.5 dB steps

1) For CL/CR: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

5.1.10. MX14 VIDEO Volume

Default: 8808H

Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:13	-	Reserved
12:8	R/W	Video Left Volume: (VL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	Video Right Volume: (VR[4:0]) in 1.5 dB steps

1) For VL/VR: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

5.1.11. MX16 AUX Volume

Default: 8808H

Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:13	-	Reserved
12:8	R/W	AUX Left Volume: (AL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	AUX Right Volume: (AR[4:0]) in 1.5 dB steps

1) For AL/AR: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

5.1.12. MX18 PCM_OUT Volume

Default: 8808H

Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:13	-	Reserved
12:8	R/W	PCM Left Volume: (PL[4:0]) in 1.5 dB steps
7:5	-	Reserved
4:0	R/W	PCM Right Volume: (PR[4:0]) in 1.5 dB steps

1) For PL/PR: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

5.1.13. MX1A Record Select

Default: 0000H

Each step in bits 2:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 7 levels of volume, from 000 to 111. Each step in bits 10:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 7 levels of volume, from 000 to 111.

Bit	Type	Function
15:11	-	Reserved
10:8	R/W	Left Record Source Select: (LRS[2:0])
7:3	-	Reserved
2:0	R/W	Right Record Source Select: (RRS[2:0])

1) For LRS:
0 MIC
1 CD LEFT
2 VIDEO LEFT
3 AUX LEFT
4 LINE LEFT
5 STEREO MIXER OUTPUT LEFT
6 MONO MIXER OUTPUT
7 PHONE

2) For RRS:
0 MIC
1 CD RIGHT
2 VIDEO RIGHT
3 AUX RIGHT
4 LINE RIGHT
5 STEREO MIXER OUTPUT RIGHT
6 MONO MIXER OUTPUT
7 PHONE

5.1.14. MX1C Record Gain

Default: 8000H

Each step in bits 3:0 correspond to 1.5dB in increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 correspond to 1.5dB in increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Bit	Type	Function
15	R/W	Mute Control: 0: Normal 1: Mute (- ‡dB)
14:12	-	Reserved
11:8	R/W	Left Record Gain Select: (LRG[3:0]) in 1.5 dB steps
7:4	-	Reserved
3:0	R/W	Right Record Gain Select: (RRG[3:0]) in 1.5 dB steps

1) For LRG/RRG: 0Fh +22.5dB
00h 0 dB (No Gain)

5.1.15. MX20 General Purpose Register

Default: 0000H

Bit	Type	Function
15:14	-	Reserved, read as 0
13	R/W	3D Control: Used to enable or disable 3D effects. 1: On 0: Off
12:10	-	Reserved, Read as 0
9	R/W	Mono Output Select: 0: MIX 1: MIC
8	R/W	Mic Select: 0: Mic 1 1: Mic 2
7	R/W	AD to DA Loop-back Control: Used to enable or disable ADC to front DAC loop-back. 0: Disable 1: Enable
6:0	-	Reserved

5.1.16. MX22 3D Control

Default: 0000H

Bit	Type	Function
15:4	-	Reserved, read as 0
3:2	R/W	LINE_OUT Separation Ration 00 0(off) 01 3(low) 10 4.3(med) 11 6(high)
1:0	-	Reserved, read as 0

5.1.17. MX26 Powerdown Control/Status

Default: 0000H

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status; a "1" indicating that the subsection is "ready." Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7 and bit 15.

When the AC-Link "CODEC Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this powerdown control/status register to determine exactly which subsections, if any are ready.

Bit	Type	Function
15	R/W	PR7 External Amplifier Power Down: (EAPD). 0: EAPD output low (enable external amplifier). 1: EAPD output high (shut down external amplifier)
14	R/W	PR6: 0: Normal 1: Power down Headphone
13	R/W	PR5: 0: Normal. 1: Disable internal clock usage (BITCLK still be output for modem CODEC)
12	R/W	PR4: 0: Normal 1: Power down AC-Link
11	R/W	R3: 0: Normal 1: Power down Mixer (VREF off)
10	R/W	PR2: 0: Normal 1: Power down Mixer (VREF on)
9	R/W	PR1: 0: Normal 1: Power down PCM DAC
8	R/W	PR0: 0: Normal 1: Power down PCM ADC and input MUX
7:4	-	Reserved, read as 0
3	R	VREF Status: 1: VREF normal level 0: Not yet
2	R	Analog Mixer Status: 1: Ready 0: Not yet
1	R	DAC Status: 1: Ready 0: Not yet
0	R	ADC Status: 1: Ready 0: Not yet

5.1.18. MX28 Extended Audio ID

Default: 0607H

Bit	Type	Function
15:14	R	ID[1:0]: 00=XTAL Out grounded ID13, ID0#=XTAL OUT crystal or floating
13:12	-	Reserved, read as 0
11:10	R	REV[1:0]=01 to indicates EMP202 is AC'97 rev2.2 compliant.
9	R	AMAP: Read as 1 (DAC mapping base on CODEC ID)
8:6	NA	Reserved, read as 0
5:4	R/W	DSA{1:0], DAC Slot Assignment ID[1:0]=00 – DSA[1:0] reset =00 where left slot 3, right slot 4 ID[1:0]=01 – DSA[1:0] reset =01 where left slot 7, right slot 8 ID[1:0]=10 – DSA[1:0] reset =01 where left slot 6, right slot 9 ID[1:0]=11 – DSA[1:0] reset =10 where left slot 10, right slot 11
3	-	Reserved, read as 0
2	R	SPDIF: Read as 1 (S/PDIF is supported)
1	R	DRA: Read as 1 (Double Rate Audio is supported)
0	R	VRA: Read as 1 (Variable Rate Audio is supported)

5.1.19. MX2A Extended Audio Status and Control

Default: 01F0H

This register contains two active bits for powerdown and status of the surrounding DACs. Bits 0, 1 & 2 are read/write bits which are used to enable or disable VRA, DRA and SPDIF respectively. Bits 4 & 5 are read/write bits used to determine the AC-LINK slot assignment of the S/PDIF. Bit 10 is a read only bit which tells the controller if the S/PDIF configuration is valid.

Bit	Type	Function
15:11	NA	Reserved
10	R	SPCV: (S/PDIF Configuration Valid). 0: Current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is not valid. 1: Current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is valid
9:6	NA	Reserved
5:4	R/W	SPSA[1:0]: (S/PDIF Slot Assignment). 00: S/PDIF source data assigned to AC-LINK slot3/4. 01: S/PDIF source data assigned to AC-LINK slot7/8. 10: S/PDIF source data assigned to AC-LINK slot6/9. 11: S/PDIF source data assigned to AC-LINK slot10/11 (default).
3	-	Reserved
2	R/W	SPDIF Enable: 1: Enable 0: Disable (Hi-Z)
1	-	Reserved
0	R/W	VRA Enable: 1: Enable 0: Disable

1) If VRA = 0, the EMP202 AD/DA operates at a fixed 48KHz sampling rate. Otherwise, it operates with variable sampling rates as defined in MX2C and MX32.
2.) If pin 48 is held high at power up, SPDIF is not available and D15:D1 cannot be written and will read back 0.

5.1.20. MX2C PCM Output Sample Rate

Default: BB80H

Bit	Type	Function
15:0	R/W	FOSR[15:0]: Output sampling rate

1) The EMP202 supports the following sampling rates as required in the PC99/PC2001 design guide.

Sampling rate	FOSR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0h
16000	3E80h
22050	5622h
24000	5DC0h
32000	7D00h
44100	AC44h
48000	BB80h

If the value written is not supported, the closest value is returned.

5.1.21. MX32 PCM Input Sample Rate

Default: BB80H

Bit	Type	Function
15:0	R/W	ISR[15:0]: Output sampling rate

1) The EMP202 supports the following sampling rates as required in the PC99/PC2001 design guide.

Sampling rate	ISR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0h
16000	3E80h
22050	5622h
24000	5DC0h
32000	7D00h
44100	AC44h
48000	BB80h

If the value written is not supported, the closest value is returned.

5.1.22. MX3A S/PDIF Output Channel Status and Control

Default: 2000H

Bit	Type	Function
15	R/W	Validity Control: (control V bit in Sub-Frame). 0: The V bit (valid flag) in sub-frame depends on whether or not the S/PDIF data is under-run. 1: The V bit in sub-frame is always sent as 1 to indicate the invalid data is not suitable for the receiver.
14	R	Double Rate S/PDIF: (DRS) This bit is always 0.
13:12	R/W	S/PDIF Sample Rate: (SPSR[1:0]). 00: Sample rate set to 44.1KHz, Fs[0:3]=0000. 01: Reserved. 10: Sample rate set to 48.0KHz, Fs[0:3]=0100 (default). 11: Sample rate set to 32.0KHz, Fs[0:3]=1100.
11	R/W	Generation Level: (LEVEL)
10:4	R/W	Category Code: (CC[6:0])
3	R/W	Preemphasis: (PRE). 0: None 1: Filter preemphasis is 50/15 µsec
2	R/W	Copyright: (COPY). 0: Asserted 1: Not asserted
1	R/W	Non-Audio Data Type: (/AUDIO). 0: PCM data 1: AC3 or other digital non-audio data.
0	R	Professional or Consumer Format: (PRO). 0: Consumer format 1: Professional format.

1) To ensure the control and status information started up correctly at the beginning of S/PDIF transmission, MX3A.[14:0] should only be written to when S/PDIF transmitter is disabled (MX2A.2=0).
2) If validity control is set (MX3A.15=1), those data bits (bit 8 ~ bit 27) should be forced to 0 to obtain better compatibility with mini disc devices.

5.2. GPIO Registers

5.2.1. MX3E Extended Modem Status and Control

Default: 0100H

Bit	Type	Function
15:9	-	Reserved
8	R/W	PRA 0 GPIO powered up/enabled 1 GPIO powered down/disabled
7:1	R	Reserved
0	R	GPIO 0 GPIO not ready (powered down) 1 GPIO Ready (powered up)

5.2.2. MX4C GPIO Pin Configuration

Default: 0003H

Bit	Type	Function
15:2	-	Reserved
1	R/W	GC1 0 GPIO1 configured as output 1 GPIO1 configured as input
0	R/W	GC0 0 GPIO0 configured as output 1 GPIO0 configured as input

5.2.3. MX4E GPIO Pin Polarity/Type

Default: FFFFH

Bit	Type	Function
15:2	-	Reserved
1	R/W	GP1 0 GPIO1 polarity inverted 1 GPIO1 polarity inverted
0	R/W	GP0 0 GPIO0 polarity inverted 1 GPIO0 polarity inverted

5.2.4. MX50 GPIO Pin Sticky

Default: 0000H

Bit	Type	Function
15:2	-	Reserved
1	R/W	GS1 0 GPIO1 non sticky 1 GPIO1 sticky
0	R/W	GS0 0 GPIO1 non sticky 1 GPIO1 sticky

5.2.5. MX50 GPIO Pin Status

Default: 0000H

Bit	Type	Function
15:2	-	Reserved
1:0	R/W	GI1 (GPIO1/0) As output, use with MX74:D0 to set If D0=0, the respective register value placed on pad (D1 for GPIO1, D0 for GPIO0) If D0=1, pad get value from slot 12 As input and sticky 0 clears this bit 1 does nothing As input and non sticky This register gives GPIO1 value from pad.

5.3. Extended Registers

5.3.1. MX6A SPDIF Output Select

Default: 0000H

Bit	Type	Function
15:2	-	Reserved
1	R/W	SPDIF Output Source Select 0 PCM data from ACLINK to SPDIF 1 ADC record data to SPDIF
0	-	Reserved

5.3.2. MX72 Antipop

Default: 0000H

Bit	Type	Function
15:8	-	Reserved
7	R/W	Internal Antipop 0 enabled 1 disabled
6:0	-	Reserved

5.3.3. MX74 EAPD Access

Default: 0800H

Bit	Type	Function
15	R/W	EAPD, Use with D11 If D11=1, EAPD data output If D11=0, EAPD data input
14:12	-	Reserved
11	R/W	EAPD Pin Enable 0 EAPD as input 1 EAPD as output
10:3	-	Reserved
2	R/W	Interrupt Disable 0 clear GPIO interrupts 1 clear GPIO interrupts with MX54
1	R/W	GPIO Access 0 ACLINK access from GPIO pad 1 ACLINK access from MX54
0	R/W	GPIOSLT12 0 GPIO0 and GPIO1 access from MX54, if GPIO is set as output, input Slot 12 will be 0h. 1 GPIO0 and GPIO1 access from Slot 12, if GPIO is set as output, input MX54 not updated.

5.3.4. MX7C VENDOR ID1

Default: FFFFH

Bit	Type	Function
15:0	R	Vendor ID: FFFFH

5.3.5. MX7E VENDOR ID2

Default: FFFFH

Bit	Type	Function
15:0	R	Vendor ID: FFFFH

6. Electrical Characteristics

6.1. DC Characteristics

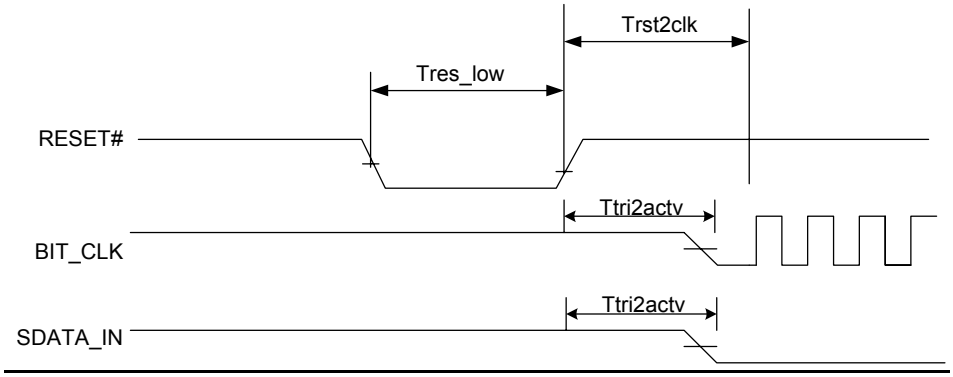
Dvdd= 3.3V ±5%, Tambient=25 0 C, with 50pF external load.-

Parameter	Symbol	Min	Typical	Max	Units
Input voltage range	Vin	-0.30	-	DVdd+0.30	V
Low level input voltage SYNC,SDATA_OUT,RESET# XTAL_IN,BIT_CLK ID1#,ID0#	VIL	- - -	1.2 / 0.7 1.7 / 1.0 2.0 / 1.2	0.30*DVdd - -	V
High level input voltage SYNC,SDATA_OUT,RESET# XTAL_IN,BIT_CLK ID1#,ID0#	VIH	0.40*DVdd - -	2.1 / 1.7 3.2 / 2.2 2.5 / 1.7	- - -	V
High level output voltage	VOH	0.90DVdd	-	-	V
Low level output voltage	VOL	-	-	0.1DVdd	V
Pull up resistance		50K	100K	200K	
Input leakage current	-	-10	-	10	uA
Output leakage current (Hi-Z)	-	-10	-	10	uA
Output buffer drive current	-	-	5	-	mA

6.2. AC Timing Characteristics

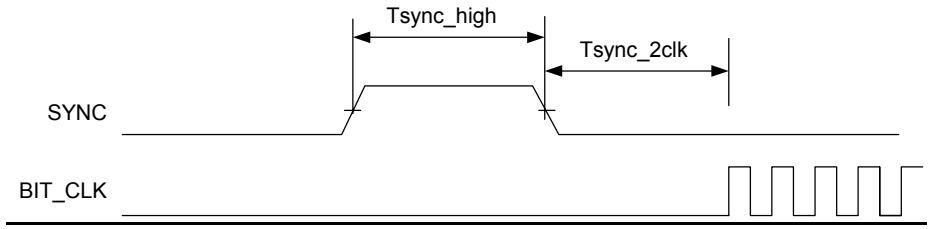
6.2.1. Cold Reset

Parameter	Symbol	Min	Typical	Max	Units
RESET# active low pulse width	Trst_low	1.0	-	-	us
RESET# inactive to BIT_CLK Startup delay	Trst2clk	162.8	-	-	ns



Cold reset timing diagram

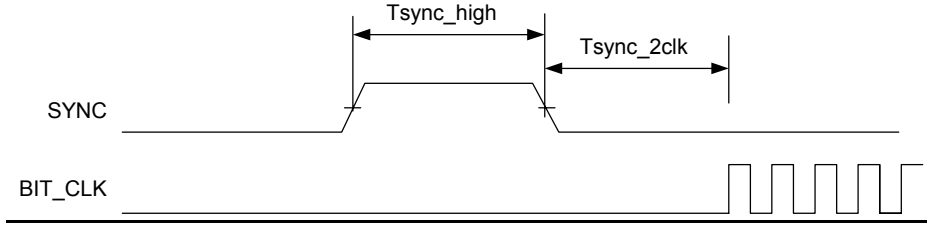
6.2.2. Warm Reset



Warm reset timing diagram

Parameter	Symbol	Min	Typical	Max	Units
SYNC active high pulse width	Tsync_high	1.0	1.3	-	us
SYNC inactive to BIT_CLK Startup delay	Tsync2clk	162.8	-	-	ns

6.2.3. AC-Link Clocks

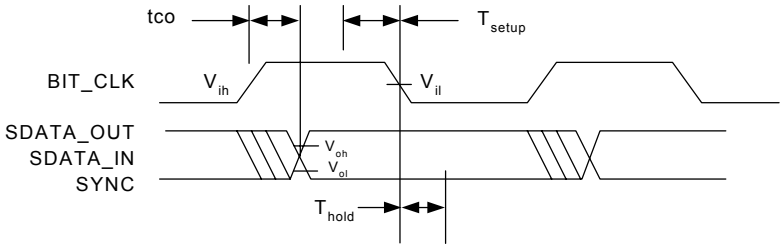


BIT_CLK and SYNC timing diagram

Parameter	Symbol	Min	Typical	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	750	750	ps
BIT_CLK high pulse width (note 1)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (note 1)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low pulse width	Tsync_low	-	19.5	-	us

Note 1: Worse case duty cycle restricted to 45/55.

6.2.4. Data Output and Input Times

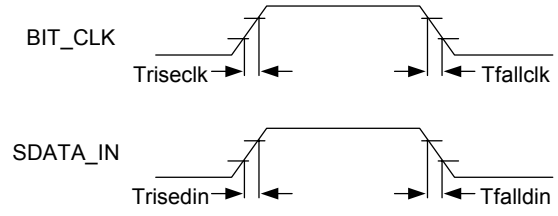


Data Output and Input timing diagram

Parameter	Symbol	Min	Typical	Max	Units
Output Valid Delay from rising edge of BIT_CLK	tco	-	-	15	ns
Input Setup to falling edge of BIT_CLK	tsetup	10	-	-	ns
Input Hold from falling edge of BIT_CLK	thold	10	-	-	ns

Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the Device driving the output.*
Note 2: 50pF external load
Note 3: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output.*

6.2.5. Signal Rise and Fall Times

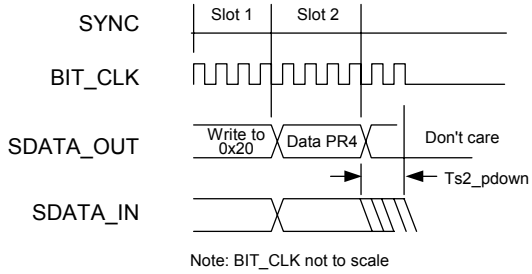


Signal Rise and Fall timing diagram

Parameter	Symbol	Min	Typical	Max	Units
BIT_CLK rise time	Triseclk	-	-	6	ns
BIT_CLK fall time	Tfallclk	-	-	6	ns
SYNC rise time	Trisesync	-	-	6	ns
SYNC fall time	Tfallsync	-	-	6	ns
SDATA_IN rise time	Trisedin	-	-	6	ns
SDATA_IN fall time	Tfalldin	-	-	6	ns
SDATA_OUT rise time	Trisedout	-	-	6	ns
SDATA_OUT fall time	Tfalldout	-	-	6	ns

Note 1: 75pF external load
Note 2: rise is from 10% to 90% of Vdd (Vol to Voh)
Note 3: fall is from 90% to 10% of Vdd (Voh to Vol)

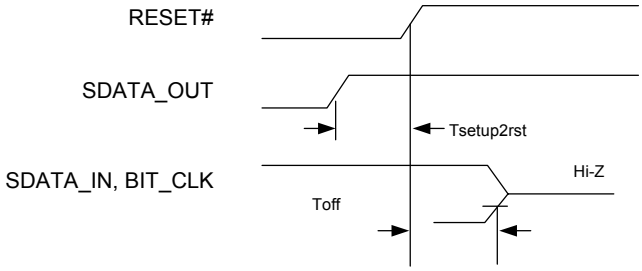
6.2.6. AC-Link Low Power Mode Timing



AC-Link low power mode timing diagram

Parameter	Symbol	Min	Typical	Max	Units
End of slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	us

6.2.7. ATE Test Mode



ATE test mode timing diagram

To meet AC'97 rev2.2 requirements, EAPD, SPDIFO, BIT_CLK and SDATA_IN should be floating in test mode.

Parameter	Symbol	Min	Typical	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

6.2.8. AC-Link IO Pin Capacitance and Loading

Output Pin	1 CODEC	2 CODEC	3 CODEC	4 CODEC
BIT_CLK (must support ≥ 2 CODECs)	47.5pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF

6.2.9. BIT-CLK and SDATA-IN State

When RESET# is active, BIT-CLK and SDATA-IN must be floating by internal pull low 100K resistors. The ac-link signals are driven by another AC'97 on CNR board. This requirement is not mentioned in AC'97 specifications Rev 2.1. Please refer to CNR (Communication Network Riser) specifications Rev. 1.0 pages 23~25 or AC'97 Rev. 2.2 for detailed information.

7. Analog Performance Characteristics

Standard test condition:

Tambient=25 0 C, Dvdd=5.0 or 3.3V ±5%,Avdd=5.0V ±5%

Input Voltage Level: Logic Low=0.35*Vdd, Logic High=0.65Vdd

1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms

10K §Ù/50pF load; Testbench Characterization BW:20Hz~20KHz

0dB attenuation; tone and 3D disabled

Parameter	Min	Typical	Max	Units
Full scale input voltage				
Mixer (except for MIC)	-	1.6	-	Vrms
Mic input (gain=0dB)	-	1.6	-	Vrms
Mic input (gain=20dB)	-	0.16	-	Vrms
ADC	-	1.0	-	Vrms
Full scale output voltage	-			
DAC		1.0	1.41	Vrms
S/N (A weighted)	-	95	-	dB FSA
CD to LINE_OUT	-	92	-	dB FSA
Other to LINE_OUT	-	85	-	dB FSA
ADC DAC	-	88	-	dB FSA
Total Harmonic Distortion + Noise				dB FS
ADC	-	-80	-	dB FS
DAC	-	-80	-	
Frequency Response				Hz
Mixers	20	-	20,000	
ADC & DAC	20	-	19,200	
Power Supply Rejection (DAC,ADC)	-	-68	-	dB
Total Out-of-Band Noise (28.8K~100KHz)	-	-63	-	dB
Mic 20dB gain is selected	18	20	22	dB
Crosstalk between inputs channels	-	-	-70	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input impedance (gain=0dB)				K
PC_BEEP only	-	32	-	
Others (PHONE,LINE,CD,AUX,VIDEO)	-	32	-	
MIC1 and MIC2	-	16	-	
Power Supply Current (normal operation)				mA
VA=5v	-	50	-	mA
VD=3.3v	-	20	-	
Power Supply Current (power down mode)				
VA=5v	-	1	mA	
VD=3.3v	-	2	mA	
VREFOUT	2.25	2.50	2.75	V
Digital Filter Characteristics				
ADC Low pass Filter				
Pass band	0	-	19.2	KHz
Stop band	28.8	-	-	KHz
Stop band Rejection	-	-76.0	-	dB
Pass band Frequency Response	-	+- 0.15	-	dB
DAC Low pass Filter				
Pass band	0	-	19.2	KHz
Stop band	28.8	-	-	KHz
Stop band Rejection	-	-78.5	-	dB
Pass band Frequency Response	-	+- 0.15	-	dB

8. Design Suggestions

8.1. Clocking

The clock source for different configurations is listed below.

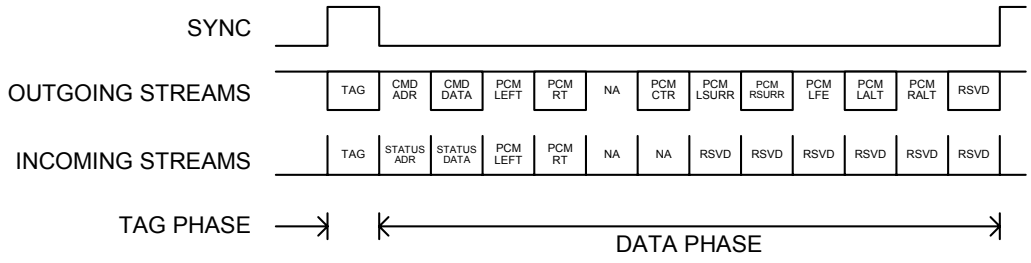
CODEC ID[1:0]	BIT-CLK	Clock source
00	Output	Crystal or external clock (XTAL-IN) BITCLK is output
01,10,11	BIT CLK	BIT CLK always an input, XTAL-IN (pin 2) ignored

8.2. AC-Link

When the EMP202 takes serial data from the AC'97 controller, it samples SDATA_OUT on the falling edge of BIT_CLK. When the EMP202 sends serial data to the AC'97 controller, it starts to drive SDATA_IN on the rising edge of BIT_CLK.

The EMP202 will return any uninstalled bits or registers with 0 for read operations. The EMP202 also stuffs the unimplemented slot or bit with 0 in SDATA-IN. Note that AC-LINK is MSB-justified.

Please refer to "Audio CODEC '97 Component Specification Revision 2.2" for details



5.1 Channel Slot Arrangement Defined in AC'97 Specification rev2.2

8.3. Reset

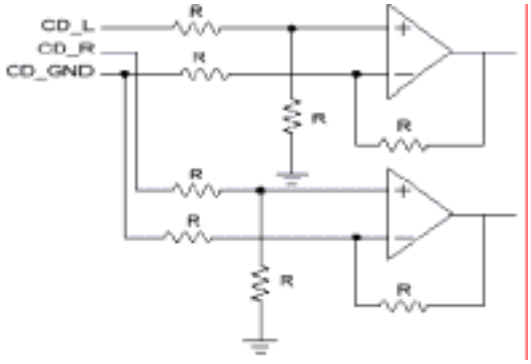
There are 3 types of reset operations: Cold, Warm and Register reset, which are listed below:

Reset Type	Trigger condition	CODEC response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to their default value.
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK, no change to register values.
Register	Write register indexed 00h	Reset all registers to their default value.

The AC'97 controller should drive SYNC and SDATA-OUT low during the period of RESET# assertion to guarantee that the EMP202 resets successfully.

8.4. CD Input

Pay attention to differential CD input. Below is an example of differential CD input.

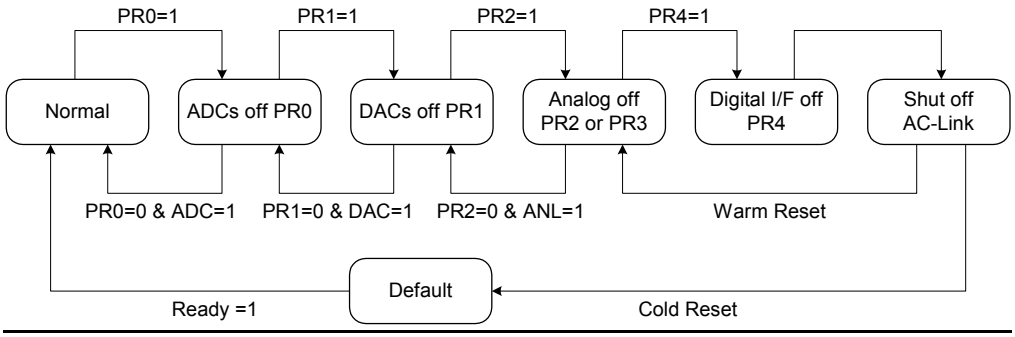


Example of differential CD input

8.5. Odd Addressed Register Access

The EMP202 will return "0000h" when odd-addressed registers and unimplemented registers are read.

8.6. Power-down Mode



Example of the EMP202 power-down/power-up flow

8.7. Test Mode

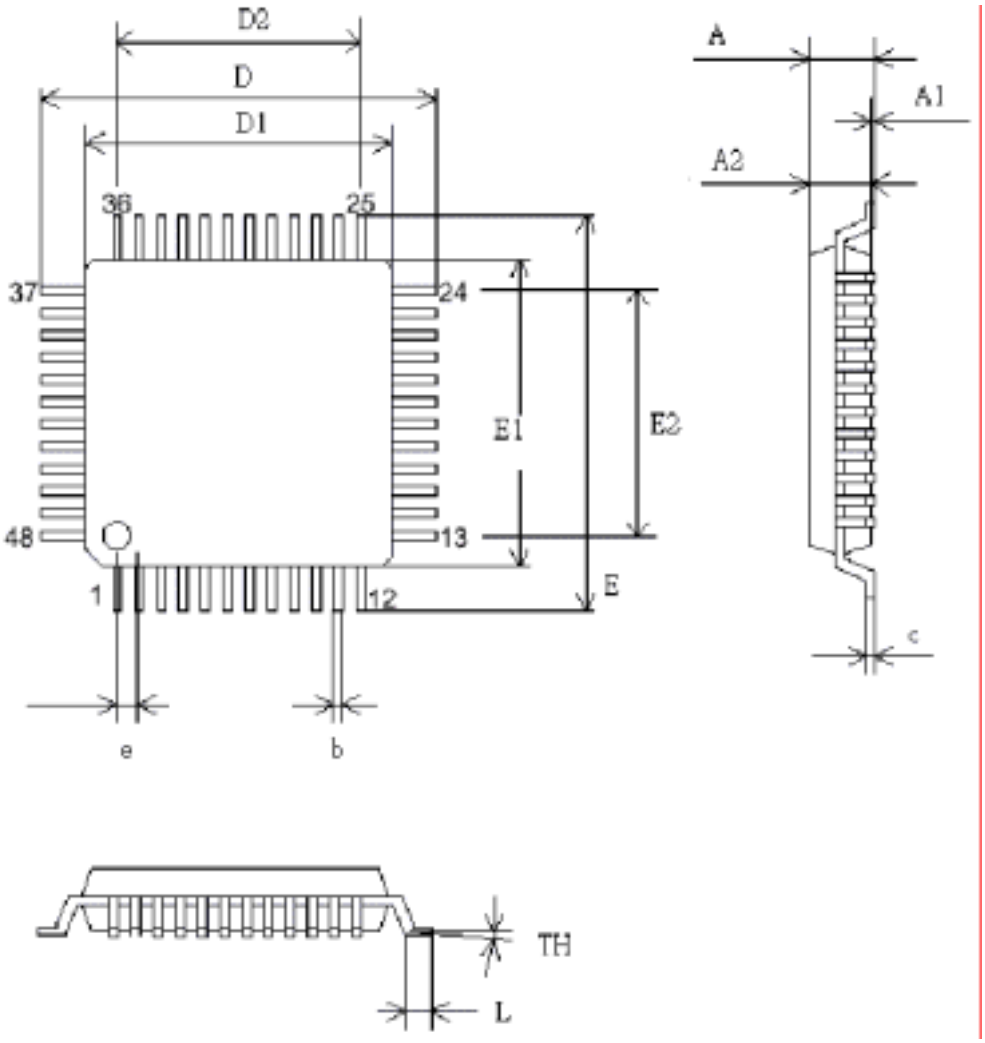
8.7.1. ATE In Circuit Test Mode

SDATA_OUT is sampled high at the trailing edge of RESET#. In this mode, the EMP202 will drive BIT_CLK, SDATA_IN, EAPD, GPIOs, IDs, and SPDIFO to high impedance.

8.7.2. Vendor Specific Test Mode

All other modes are reserved.

9. Package Dimensions



SYMBOL	MILLIMETER		
	MIN.	TYPICAL	MAX.
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
c	0.09		0.20
D		9.00 BSC	
D1		7.00 BSC	
D2		5.50	
E		9.00 BSC	
E1		7.00BSC	
E2		5.50	
b	0.17	0.20	0.27
e		0.50 BSC	
TH	0°	3.5°	7°
L	0.45	0.60	0.75