杰力科技股份有限公司
Excelliance MOS Corporation

EMP21N03HR

N-Channel Logic Level Enhancement Mode Field Effect Transistor

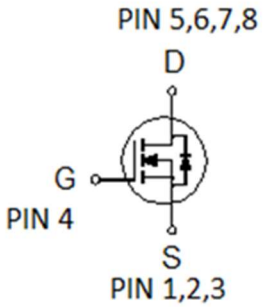
Product Summary:

BV_{DSS}	30V
$R_{DSON\ (MAX.)}$	2.3mΩ
I_D	100A

N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (Tc = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[1]	T_C = 25 °C	I_D	100	A
	T_C = 100 °C		70	
Pulsed Drain Current[2]		I_{DM}	400	
Avalanche Current		I_{AS}	65	
Avalanche Energy	L = 0.1mH	E_{AS}	211	mJ
Repetitive Avalanche Energy[3]	L = 0.05mH	E_{AR}	105	
Power Dissipation	T_C = 25 °C	P_D	50	W
	T_C = 100 °C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=40A, Rated V_{DS}=30V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient[4]	$R_{\theta JA}$		50	

[1]Package Limited.

[2]Pulse width limited by maximum junction temperature.

[3]Duty cycle ≤ 1%

[4]50°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1	1.5	3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V			1	μA
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	100			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 25A		2.0	2.3	mΩ
		V_{GS} = 4.5V, I_D = 15A		2.9	3.7	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 25A		70		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		3813		pF
Output Capacitance	C_{oss}			540		
Reverse Transfer Capacitance	C_{rss}			440		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		1.5		Ω
Total Gate Charge[1,2]	Q_g(V_{GS}=10V)	V_{DS} = 15V, V_{GS} = 10V, I_D = 25A		59		nC
	Q_g(V_{GS}=4.5V)			28		
Gate-Source Charge[1,2]	Q_{gs}			13		
Gate-Drain Charge[1,2]	Q_{gd}			11		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 15V, I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7Ω		25		nS
Rise Time[1,2]	t_r			16		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			60		
Fall Time[1,2]	t_f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current[4]	I_S				100	A
Pulsed Current[3]	I_{SM}				400	
Forward Voltage[1]	V_{SD}	I_F = 30A, V_{GS} = 0V			1.2	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / μS		35		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			200		A
Reverse Recovery Charge	Q_{rr}			25		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

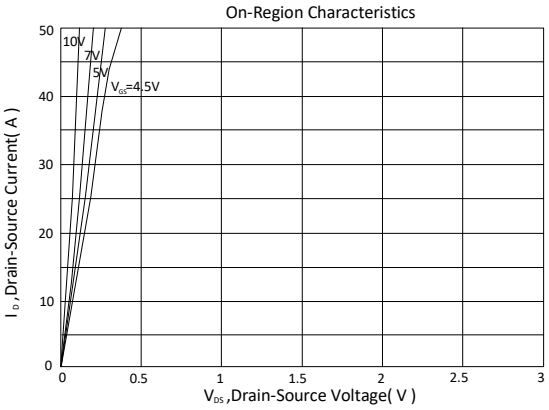
[2]Independent of operating temperature.

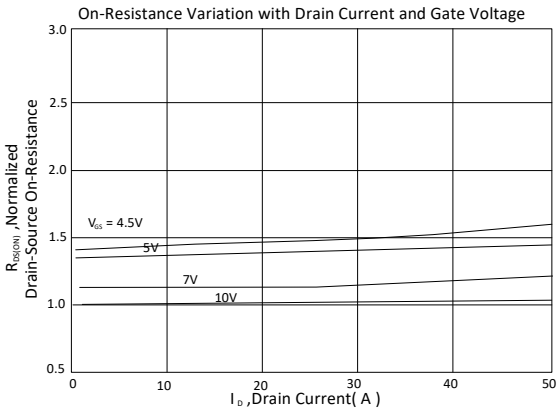
[3]Pulse width limited by maximum junction temperature.

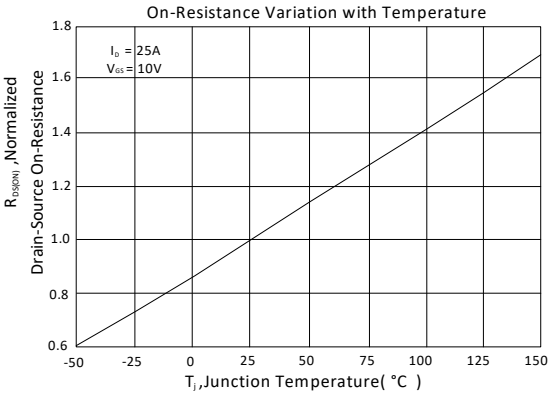
[4]Package Limited.

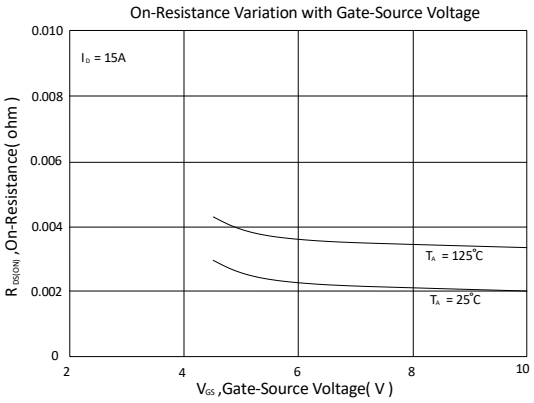
EMC will review datasheet by quarter, and update new version.

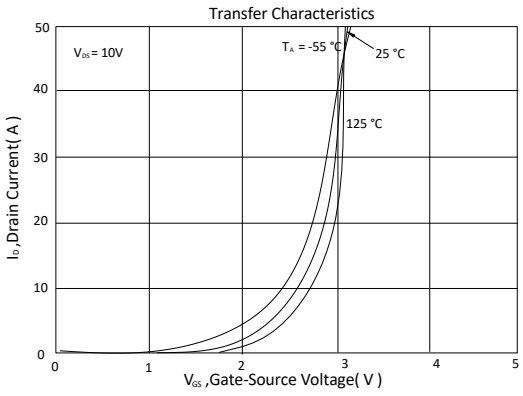
TYPICAL CHARACTERISTICS

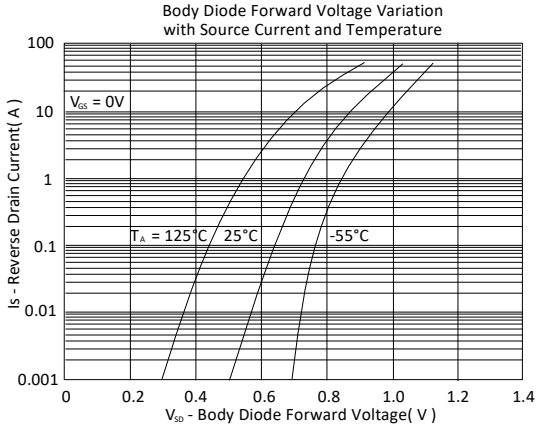


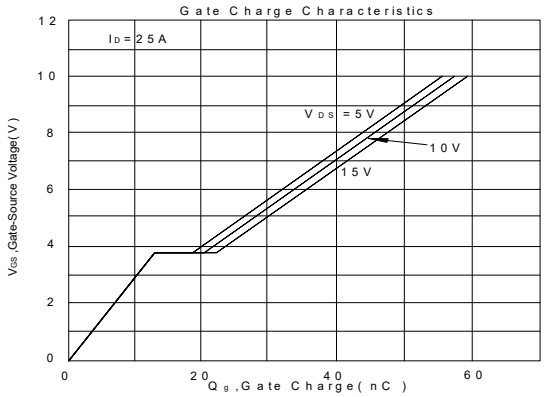


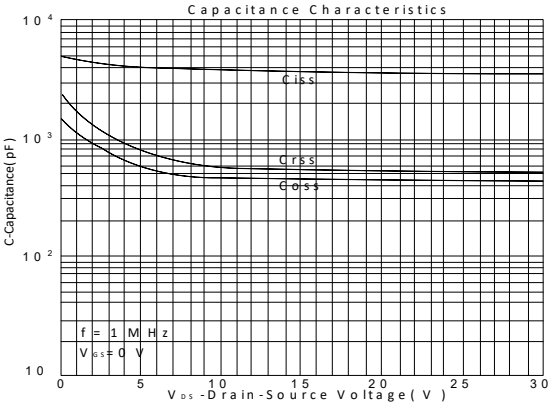


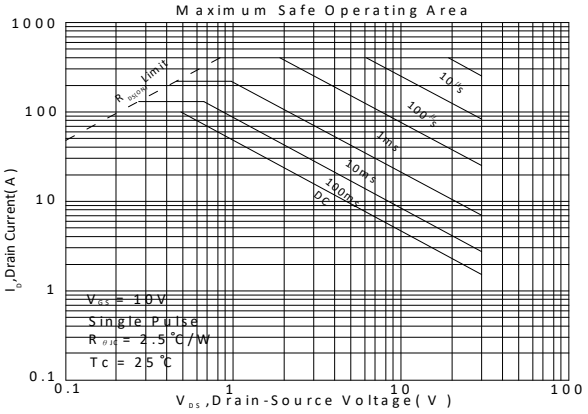


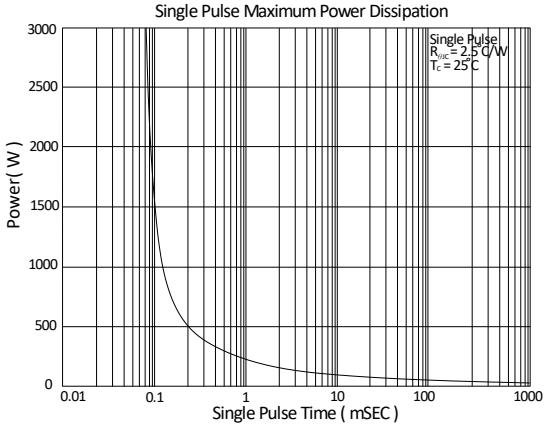


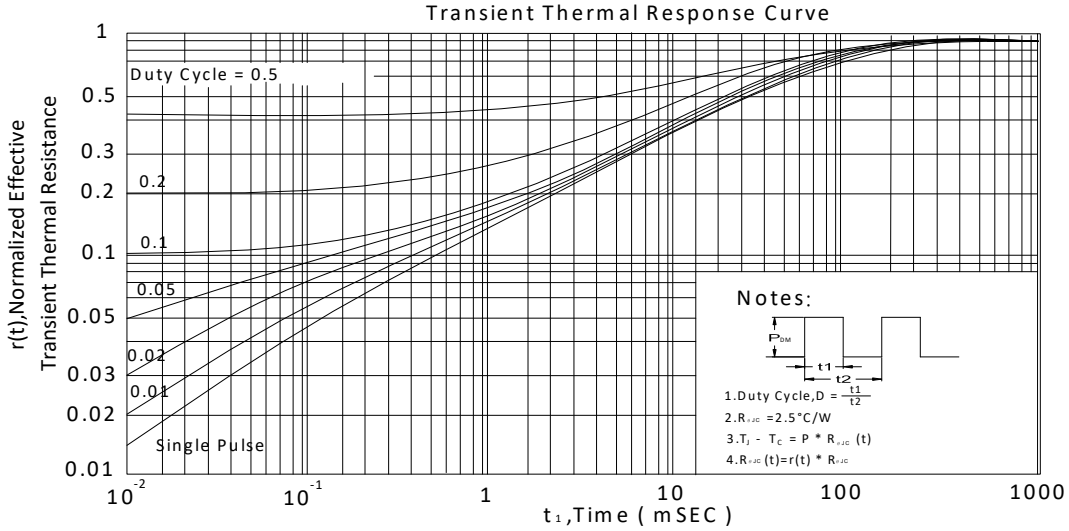



Gate Charge Characteristics
ID = 25A
VDS = 5V
10V
15V
VGS ,Gate-Source Voltage(V)
Qg ,Gate Charge(nC)


Capacitance Characteristics
Ciss
Crss
Coss
f = 1 MHz
VGS = 0 V
C-Capacitance(pF)
VDS -Drain-Source Voltage(V)

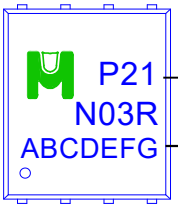

Maximum Safe Operating Area
RDS(ON) Limit
10μs
100μs
1ms
10ms
100ms
DC
VGS = 10V
Single Pulse
RθJC = 2.5°C/W
TC = 25°C
ID ,Drain Current(A)
VDS ,Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
RθJC = 2.5°C/W
TC = 25°C
Power(W)
Single Pulse Time (mSEC)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
PDM
t1
t2
1.Duty Cycle,D = t1/t2
2.RθJC =2.5°C/W
3.TJ - TC = P * RθJC (t)
4.RθJC (t)=r(t) * RθJC
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (mSEC)

Ordering & Marking Information:

Device Name: EMP21N03HR for EDFN 5 x 6



P21N03R: Device Name

ABCDEFG: Date Code

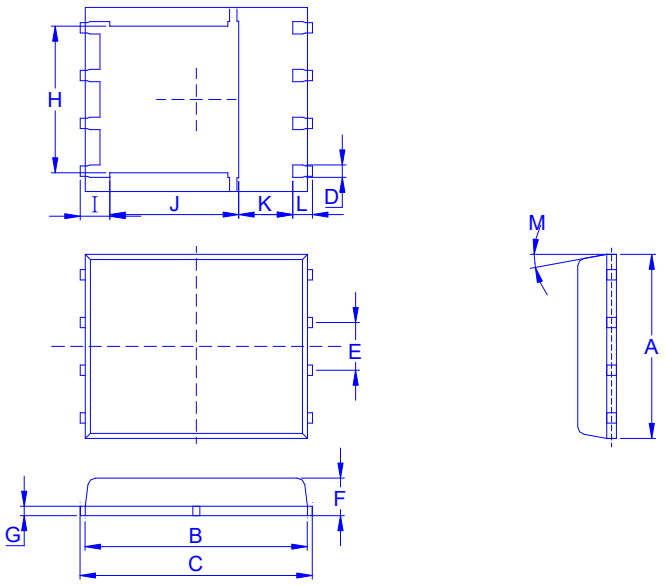
A: Assembly House

B: Year(A:2008 B:2009 C:2010….)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

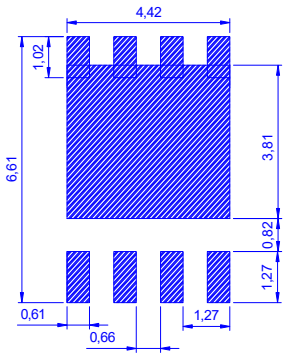
Outline Drawing



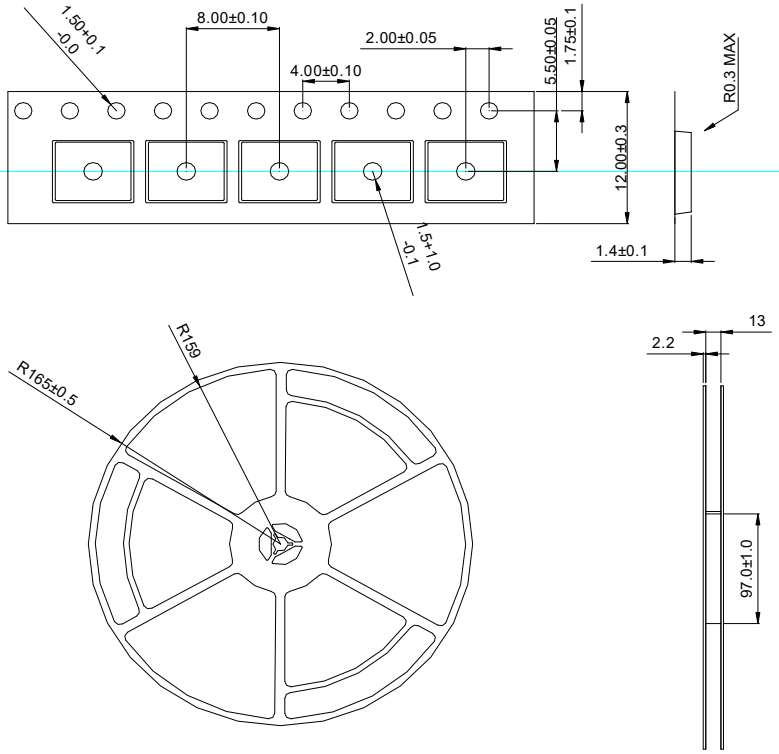
Dimension in mm

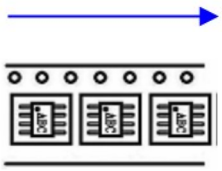
Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min	4.80	5.55	5.90	0.30	1.17	0.85	0.15	3.61	0.38	3.18	1.00	0.38	0 °
Typ.	4.90	5.70	6.00	0.40	1.27	0.95	0.20	3.87	0.40	3.44	1.20	0.40	
Max	5.40	5.85	6.15	0.51	1.37	1.17	0.34	4.31	0.71	3.78	1.39	0.71	12 °

Recommended minimum pads



◆ Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)



產品別	EDFN5X6
Reel 尺寸	13”
編帶方式	FEED DIRECTION 
前空格	25
後空格	50
裝箱數	
滿捲數量	2.5K
捲/內盒比	1：1
內盒滿箱數	2.5K
內/外箱比	10：1
外箱滿箱數	25K