Fast Ultra High-PSRR, Low-Noise, Low-Dropout, 300mA CMOS Linear Regulator

General Description

The EMP8020 low-dropout (LDO) CMOS linear regulator features an ultra-high power supply rejection ratio (78dB at 1kHz), low output voltage noise (48μV), low dropout voltage, low quiescent current (50μA), and fast transient response. It guarantees a delivery of 300mA output current, and supports preset output voltages ranging from 0.8V to 4.75V with 0.05V increments.

The EMP8020 is ideal for battery-powered applications because of its low quiescent current consumption and its 1nA shutdown mode. The regulator provides fast turn-on and start-up time by using dedicated circuitry to pre-charge an optional external bypass capacitor. This bypass capacitor is used to reduce the output voltage noise without adversely affecting the load transient response. The high power supply rejection ratio of the EMP8020 holds well for low input voltages typically encountered in battery operated systems. The regulator is stable with small ceramic capacitive loads (2.2μF typical).

Additional features include bandgap voltage reference, constant current limiting, and thermal overload protection. Both of Miniature 5-pin SC-70-5/SOT-23-5 and 4-pin SC-82-4 package options are offered to provide flexibility for different applications.

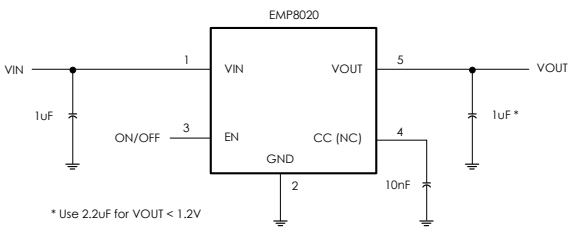
Applications

- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

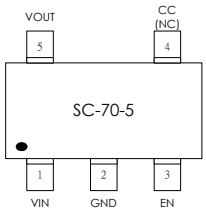
Features

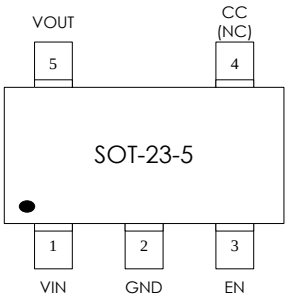
- Miniature SC-70-5,SOT-23-5 and SC-82-4 packages
- 300mA guaranteed output current
- PSRR 78dB typical at 1kHz
  70dB typical at 10kHz
- 48μV RMS output voltage noise (10Hz to 100kHz) (Vout=2.8V, Cbypass=10nF)
- 305mV typical dropout at 300mA (Vout=2.8V)
- 50μA typical quiescent current
- 1nA typical shutdown mode
- Fast line and load transient response
- 140μs typical fast turn-on time (Vout=2.8V, Cbypass=10nF)
- 2.2V to 5.5V input range
- Stable with small ceramic output capacitors
- Over-temperature and over-current protection
- ±2% output voltage tolerance

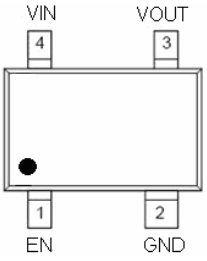
Typical Application



Connection Diagrams







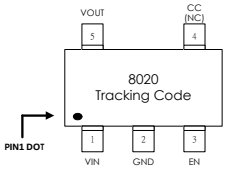
Order information

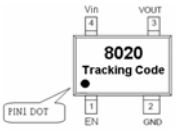
EMP8020-XXVI05NRR
XX Output voltage
VI05 SC-70-5 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

EMP8020-XXVF05NRR
XX Output voltage
VF05 SOT-23-5 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

EMP8020-XXVJ04NRR
XX Output voltage
VJ04 SC-82-4 Package
NRR RoHS & Halogen free package
Rating: -40 to 85°C
Package in Tape & Reel

Order, Marking, and Packing Information

Package	Vout	Product ID.	No. of Pin	EN	CC (NC)	Marking	Packing
SC-70-5	1.5	EMP8020-15VI05NRR	5	Y	Y		Tape & Reel 3Kpcs
	1.8	EMP8020-18VI05NRR					
	2.5	EMP8020-25VI05NRR					
	2.8	EMP8020-28VI05NRR					
	3.0	EMP8020-30VI05NRR					
	3.1	EMP8020-31VI05NRR					
	3.3	EMP8020-33VI05NRR					
SOT-23-5	1.8	EMP8020-18VF05NRR	5	Y	Y		Tape & Reel

	2.5	EMP8020-25VF05NRR					3Kpcs
	2.8	EMP8020-28VF05NRR					
	3.0	EMP8020-30VF05NRR					
	3.1	EMP8020-31VF05NRR					
	3.3	EMP8020-33VF05NRR					
SC-82-4	3.1	EMP8020-31VJ04NRR	4	Y	N		Tape & Reel 3Kpcs

Pin Functions

Name	SC-70-5	SOT-23-5	SC-82-4	Function
VOUT	5	5	3	**Output Voltage Feedback**
VIN	1	1	4	**Supply Voltage Input** Require a minimum input capacitor around 1μF to ensure stability and sufficient decoupling from the ground pin.
GND	2	2	2	**Ground Pin**
CC (NC)	4	4	N/A	**Compensation Capacitor (Soft Start)** Connect an optimum 10nF noise bypass capacitor between the CC and the ground pins to reduce noise in VOUT. **(Note. It can be floated, but don't connect the CC pin to any DC voltage.)**
EN	3	3	1	**Shutdown Input** Set the regulator into disable mode by pulling the EN pin low. To keep the regulator on during normal operation, connect the EN pin to VIN. The EN pin must not exceed VIN under all operating conditions.

Functional Block Diagram

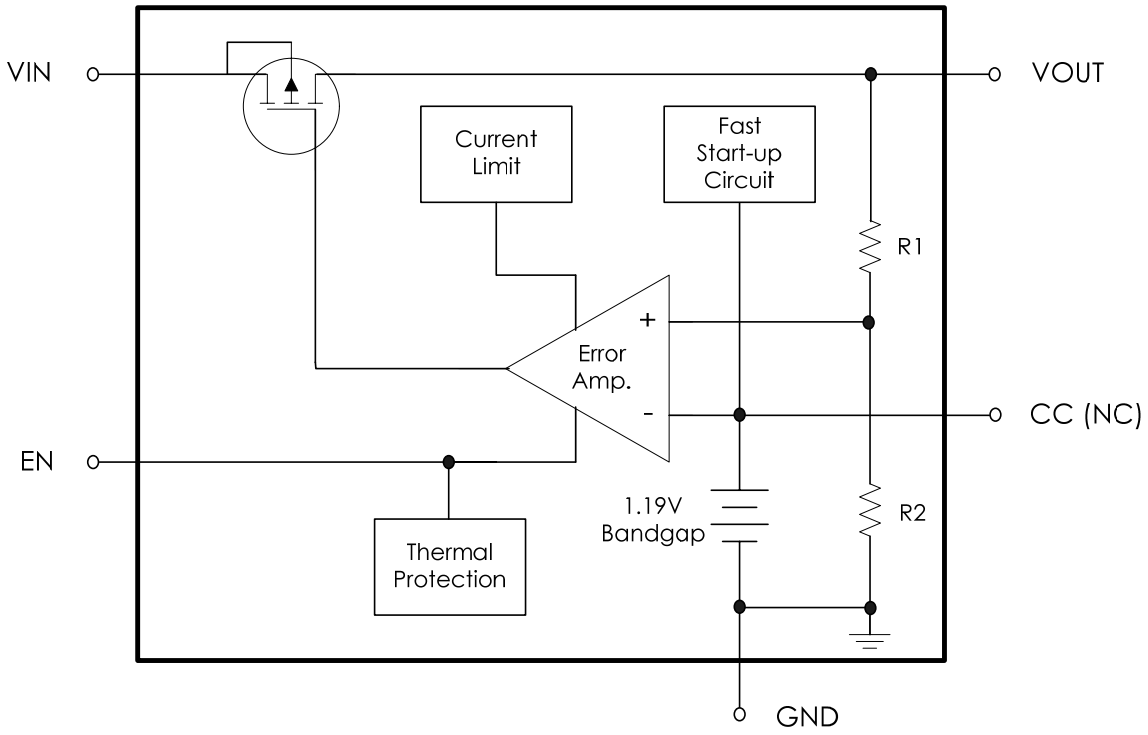


FIG.1. Functional Block Diagram of EMP8020

Absolute Maximum Ratings (Notes 1, 2)

VIN, VOUT, VEN	-0.3V to 6.0V	Lead Temperature (Soldering, 10 sec.)	260°C
Power Dissipation	(Note 4)	ESD Rating	
Storage Temperature Range	-65°C to 150°C	Human Body Model (Note 6)	2KV
Junction Temperature (T_J)	150°C	MM	200V

Operating Ratings (Note 1, 2)

Supply Voltage	2.2V to 5.5V	Thermal Resistance (θ_{JA}))	
Storage Temperature Range	-40°C to 85°C	SC-70-5	331°C /W (Note. 3)
		SOT-23-5	124°C /W (Note. 3)

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V_{IN} = V_{OUT}$ +1V (Note 7), VEN = V_{IN}, $C_{IN} = C_{OUT}$ = 2.2µF, C_{CC} = 33nF, T_J = 25°C. **Boldface** limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_{IN}	Input Voltage			**2.2**		**5.5**	V
ΔV_{OTL}	Output Voltage Tolerance	100µA ≤ I_{OUT} ≤ 300mA $V_{OUT\ (NOM)}$ +0.5V ≤ VIN ≤ 5.5V (Note 7)		-2		+2	% of $V_{OUT\ (NOM)}$
				-3		**+3**	
I_{OUT}	Maximum Output Current	Average DC Current Rating		**300**			mA
I_{LIMIT}	Output Current Limit			**358**	489	**622**	mA
I_Q	Supply Current	I_{OUT} = 0mA			50		µA
		I_{OUT} = 300mA			120		
	Shutdown Supply Current	V_{OUT} = 0V, EN = GND			0.001	1	
V_{DO}	Dropout Voltage (Note 8)	Vout=1.8V	I_{OUT} =300mA		395		mV
		Vout=2.5V			310		
		Vout=2.8V			305		
		Vout=3.0V			297		
		Vout=3.1V			274		
		Vout=3.3V			267		

ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 7)	-0.1	0.02	0.1	%/V
	Load Regulation	100μA ≤ I_{OUT} ≤ 300mA		0.001		%/mA
e_n	Output Voltage Noise	I_{OUT}=10mA,10Hz ≤ f ≤ 100kHz Cbypass = 10nF		45		μV_{RMS}
		I_{OUT}=10mA,10Hz ≤ f ≤ 100kHz Cbypass = float		145		
VEN	EN Input Threshold	V_{IH}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 7)	**1.2**			V
		V_{IL}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 7)			**0.4**	
IEN	EN Input Bias Current	EN = GND or VIN		0.1	100	nA
T_{SD}	Thermal Shutdown Temperature			167		℃
	Thermal Shutdown Hysteresis			30		
T_{ON}	Start-Up Time	C_{OUT} = 10μF, V_{OUT} at 90% of Final Value		140		μs

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: θ_{JA} is measured in the natural convection at T_A=25℃ on a high effective thermal conductivity test board (2 layers , 2S0P) of JEDEC 51-7 thermal measurement standard.

Note 4: Maximum Power dissipation for the device is calculated using the following equation:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the SOT-23-5 package θ_{JA} = 250°C/W, T_J (MAX) = 150°C and using TA = 25°C, the maximum power dissipation is found to be 500mW. The derating factor (-1/θ_{JA}) = -4.0mW/°C, thus below 25°C the power dissipation figure can be increased by 4.0mW per degree, and similarity decreased by this factor for temperatures above 25°C.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: Human body model: 1.5kΩ in series with 100pF.

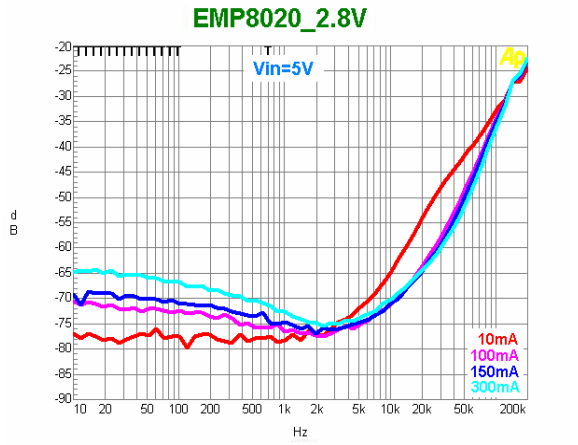
Note 7: Condition does not apply to input voltages below 2.2V since this is the minimum input operating voltage.

Note 8: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 1.8V.

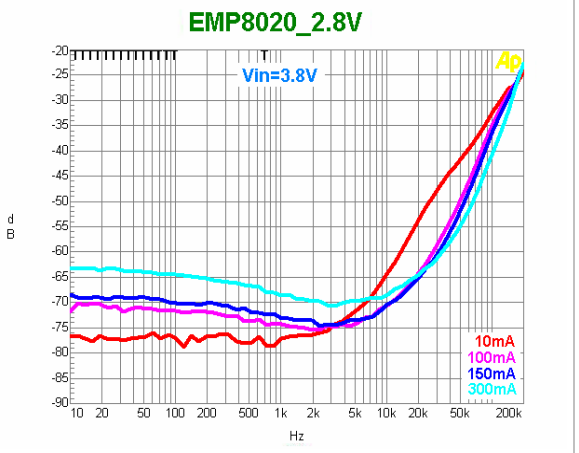
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 10nF, T_A = 25°C, VEN = VIN.

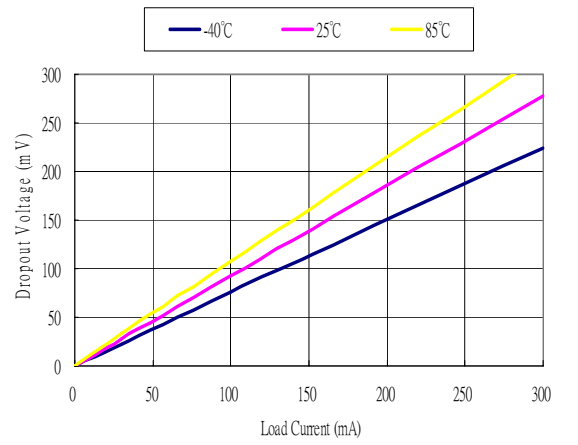
PSRR vs. Frequency (VIN=5V, VOUT=2.8V)



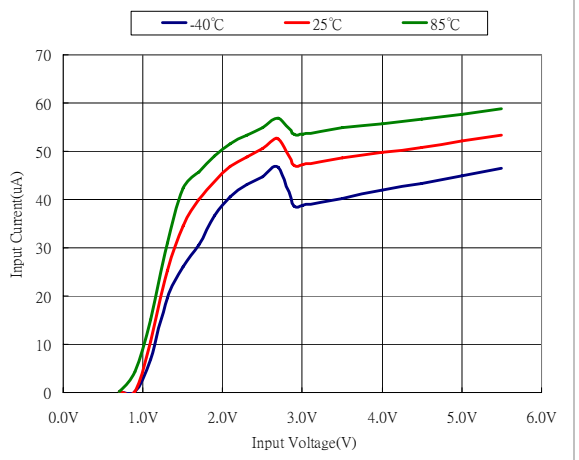
PSRR vs. Frequency (VIN=3.8V, VOUT=2.8V)



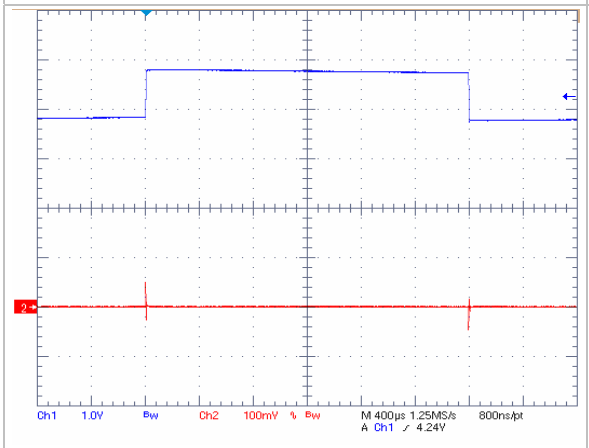
Dropout Voltage vs. Load Current (VOUT=2.8V)



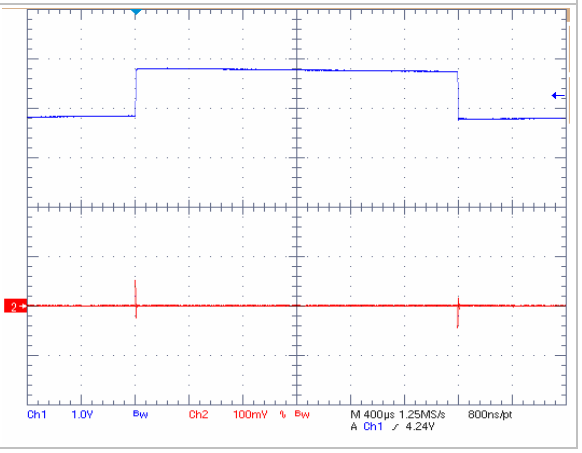
Ground Current vs. VIN (VOUT=2.8V)



Line Transient (VOUT=2.8V, IOUT=1mA)



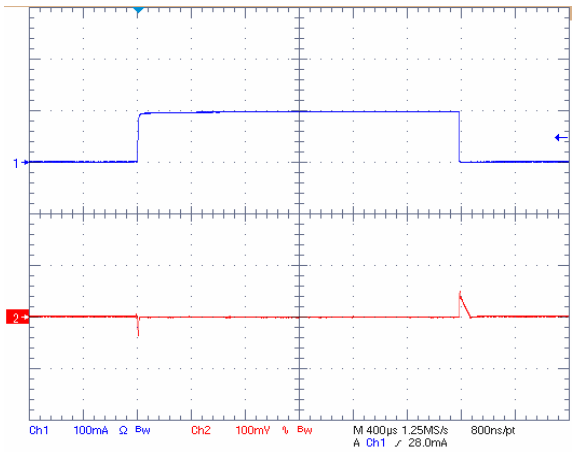
Line Transient (VOUT=2.8V, IOUT=100mA)



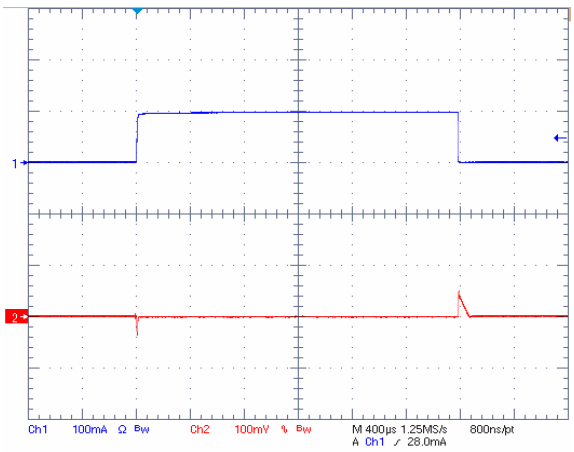
Typical Performance Characteristics (cont.)

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 10nF, T_A = 25°C, VEN = VIN.

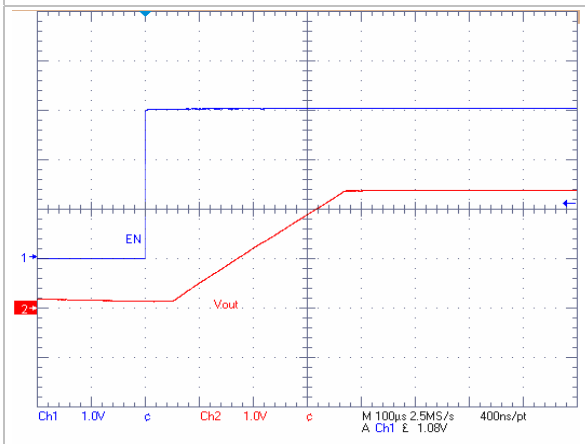
Load Transient (VOUT=2.8V, IOUT=1mA)



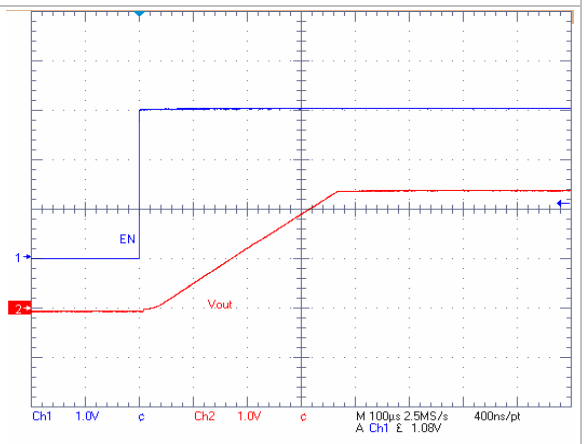
Load Transient (VOUT=2.8V, IOUT=100mA)



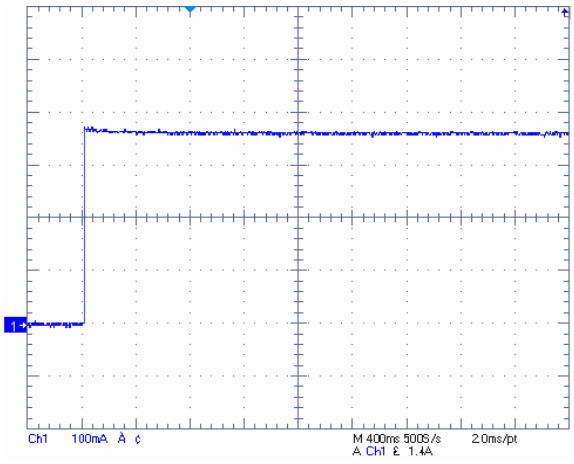
Enable Response (VOUT=2.5V, IOUT=0mA)



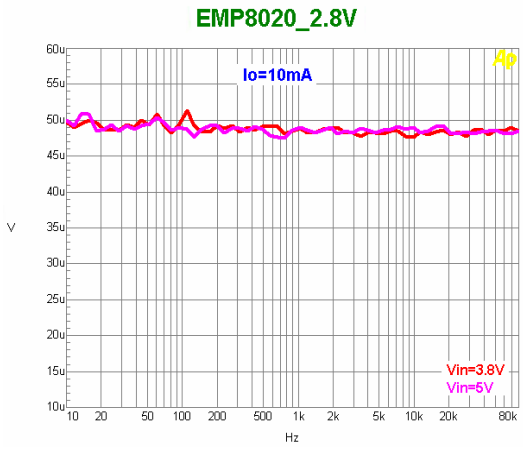
Enable Response (VOUT=2.5V, IOUT=50mA)



Current Limit (VOUT=2.8V)



Noise Level (VOUT=2.8V, IOUT=10mA)



Application Information

General Description

Referring to Fig.1as shown in the Functional Block Diagram section, the EMP8020 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. Resistors (R1, R2) form the feedback circuit which samples the output voltage for the error amplifier's non-inverting input. The inverting input is set to the bandgap reference voltage. Due to its high open-loop gain, the error amplifier ensures that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor, which controls the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register these changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. The regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Capacitor

The EMP8020 is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space, as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8020 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8020 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8020. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action due to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used sincethey are prone to fail in short-circuit operating conditions.

Compensation (Noise Bypass) Capacitor

Substantial reduction in the output voltage noise of the EMP8020 is accomplished by connecting the noise bypass capacitor CC (10nF optimum) between pin 4 and the ground. Because pin 4 connects directly to the high

impedance output of the bandgap reference circuit, the level of the DC leakage currents in the CC capacitors used will adversely reduce the regulator output voltage. This sets the DC leakage level as the key selection criterion of the CC capacitor types for use with the EMP8020. NPO and COG ceramic capacitors typically offer very low leakage. Although the use of the CC capacitors does not affect the transient response, it does affect the turn-on time of the regulator. Trade off exists between output noise level and turn-on time when selecting the CC capacitor value.

Power Dissipation and Thermal Shutdown

Thermal overload is caused by excessive power dissipation, which raises the IC junction temperature beyond a safe operating level. The EMP8020 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature TJ exceeding 167°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools down around 30°C. When continuous thermal overload conditions persist, the thermal shutdown action results in a pulsed waveform generated at the output of the regulator. An IC junction with a low thermal resistance θ_{JA} (°C/W) is preferred because the IC will be relatively effective in dissipating its thermal energy to its ambient. The relationship between θ_{JA} and T_J is as follows:

$T_J = \theta_{JA}$ (PD) + T_A

Where T_A is the ambient temperature.
P_D is the power generated by the IC and can be written as:

$P_D = I_{OUT} (V_{IN} - V_{OUT})$

As the equations show, it is desirable to work with ICs whose θ_{JA} values are small so T_J does not increase rapidly with P_D. To avoid thermal overloading do not exceed the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

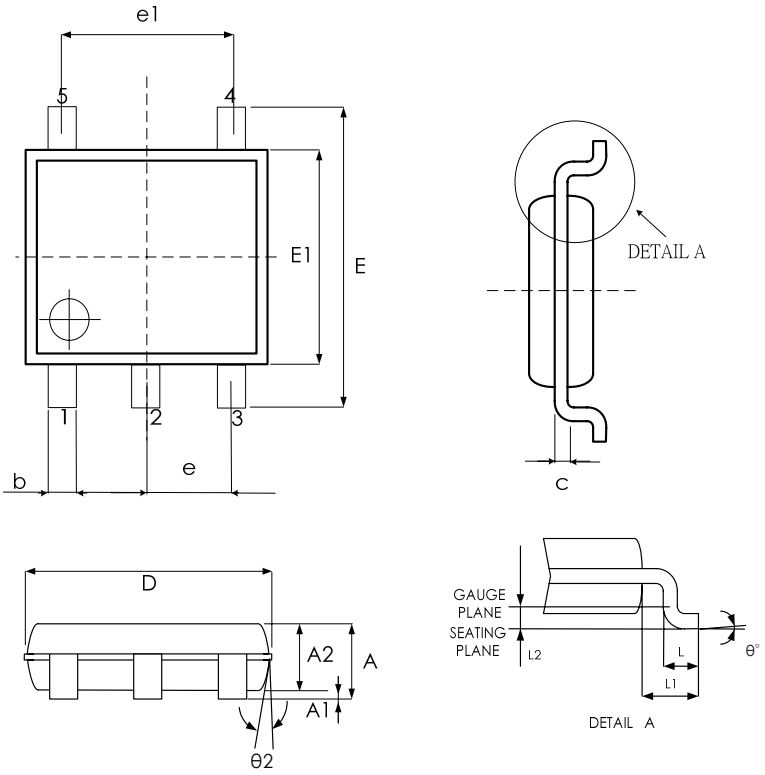
Shutdown

The EMP8020 enters sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1nA. The low supply current makes the EMP8020 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin to enter sleep mode is 0.4V. A minimum guaranteed voltage of 1.2V at the EN pin will activate the EMP8020. To constantly keep the regulator on, direct connection of the EN pin to the VIN pin is allowed.

Fast Start-Up

Fast start-up time is important for overall system efficiency improvement. The EMP8020 assures fast start-up speed when using the optional noise bypass capacitor (CC). To shorten start-up time, the EMP8020 internally supplies a current to charge up the capacitor until it reaches about 90% of its final value.

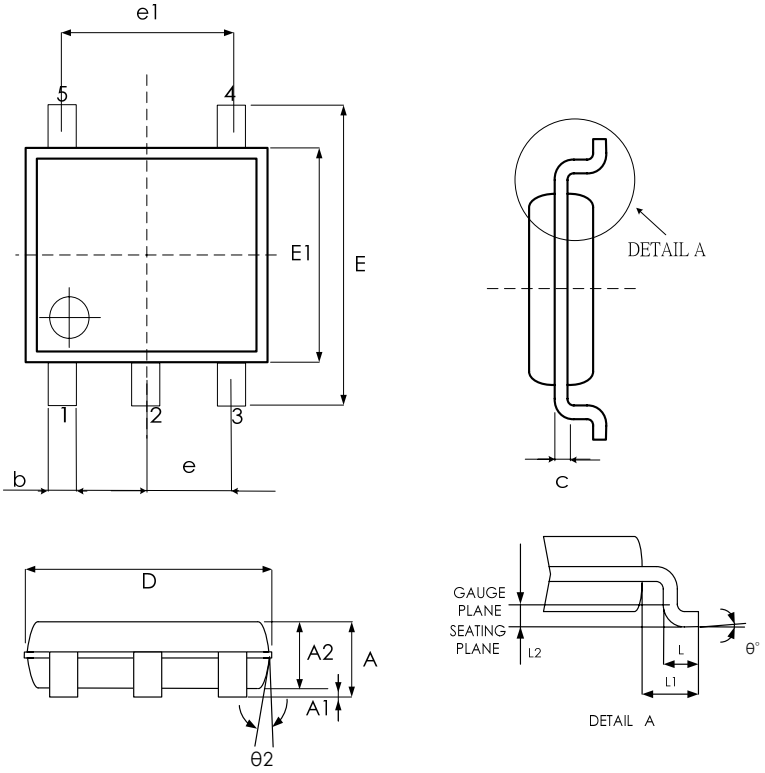
Package Outline Drawing
SC-70-5



SYMBPLS	MIN.	NOM.	MAX.
A	0.8	—	1.10
A1	0	—	0.10
A2	0.8	0.90	1.00
B	0.15	—	0.30
C	0.08	—	0.22
D	1.85	2.00	2.15
E	1.8	2.10	2.40
E1	1.10	1.25	1.40
E	0.65 BSC		
e1	1.30 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
θ°	0	4	8
θ2°	4	—	12

UNIT: MM

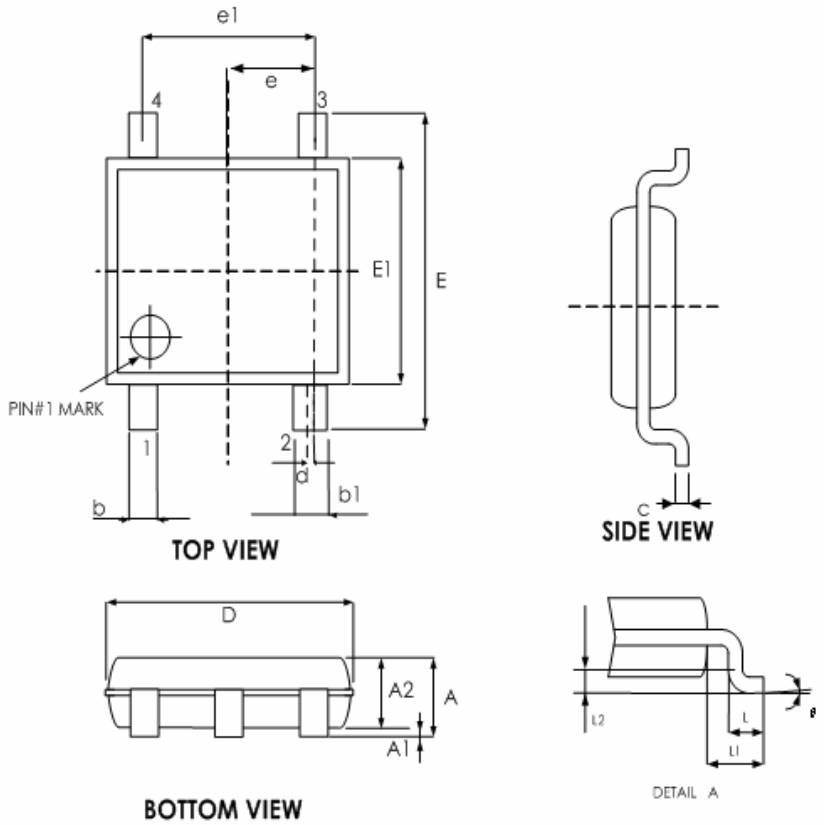
Package Outline Drawing
SOT-23-5



SYMBPLS	MIN.	NOM.	MAX.
A	1.05	1.20	1.35
A1	0.05	0.10	0.15
A2	1.00	1.10	1.20
B	0.30	—	0.50
C	0.08	—	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
E	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.55
L1	0.60 REF		
θ°	0	5	10
θ2°	6	8	10

UNIT: MM

Package Outline Drawing
SC-82-4



SYMBOL	COMMON			
	DIMENSIONS MILLIMETER		DIMENSIONS INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.250	0.400	0.010	0.016
b1	0.350	0.500	0.014	0.020
c	0.080	0.150	0.003	0.006
d	0.050 TYP.		0.002 TYP.	
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525 TYP.		0.021 TYP.	
L2	0.250 TYP.		0.010 TYP.	

Revision History

Revision	Date	Description
0.1	2009.07.09	Original
0.2	2010.03.18	1) Added 3.1V and 3.3V option. 2) Added “Soft Start” for the pin description. 3) Remove “GRR” order information
0.3	2010.07.28	1) Added 1.8V Vout version. 2) Modified SOT-25 → SOT-23-5 (let package name uniform in BU2). 3) Modified package thermal resistance (θ_{JA})) data. 4) Added Dropout voltage for Vout=3.3V, Vout=3.1V and Vout=1.8V. 5) Node. 7 item revised.
0.4	2010.08.26	1) Modified dropout voltage for Vout=2.8V 2) Added 3.0V Vout version. 3) Added Dropout voltage for Vout=3.0V
0.5	2010.10.21	1)Add 1.5V/1.8V/2.5V/3.0V/3.3V option for SC-70-5 package 2)Modified Note item number
0.6	2011.01.06	1)Added Dropout voltage for Vout=2.5V 2)Added Vout=2.5V Voltage option for SOT-25
0.7	2011.03.22	1)Add 3.1V option for SC-70-5 2)Add 3.1V option for SC-82-4

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