

# High Input Voltage, Low Quiescent Current, Low-Dropout Linear Regulator

## General Description

The EMP8041 is a high voltage, low quiescent current, low dropout regulator with 150mA output driving capacity. The EMP8041, which operates over an input range up to 40V, is stable with any capacitors, whose capacitance is larger than 1 $\mu$ F, and suitable for powering battery-management ICs because of the virtue of its low quiescent current consumption and low dropout voltage. Below the maximum power dissipation (please refer to Note. 5), It guarantees delivery of 100mA output current, and supports preset output voltages ranging from 1.3V to 6.0V with 0.1V increment.

EMP8041 features also include bandgap voltage reference, constant current limiting and thermal overload protection. Both miniature SOT-23-5 and SOT-89-3 package options are offered to provide flexibility for different applications.

## Applications

- Logic Supply for High Voltage Batteries
- Keep-Alive Supply
- 3-4 Cell Li-ion Batteries Powered systems

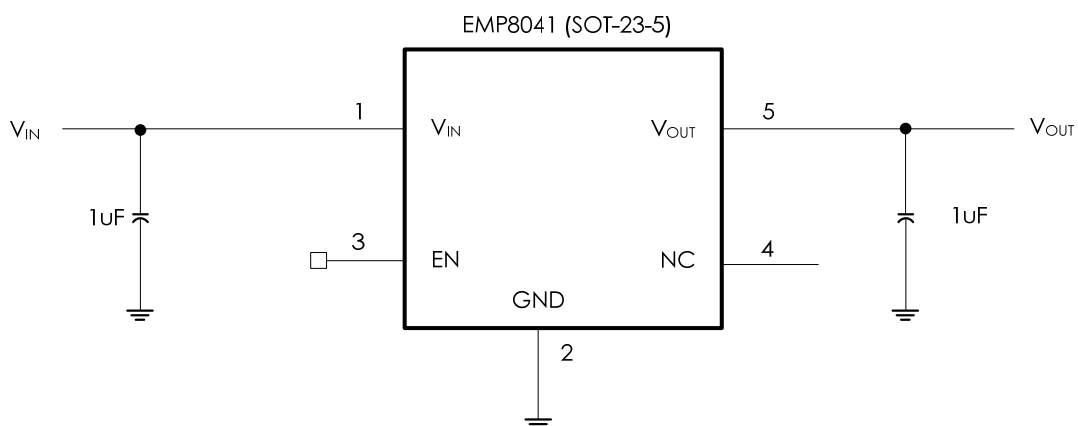
## Features

- 150mA output current driving capacity
- 780mV typical dropout at I<sub>o</sub>=150mA
- 12 $\mu$ A typical quiescent current
- 1 $\mu$ A typical shutdown mode
- Up to 40V input range
- Stable with small ceramic output capacitors (1 $\mu$ F)
- Over temperature and over current protection

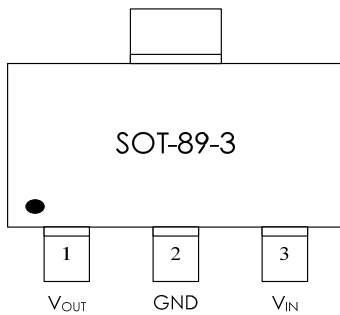
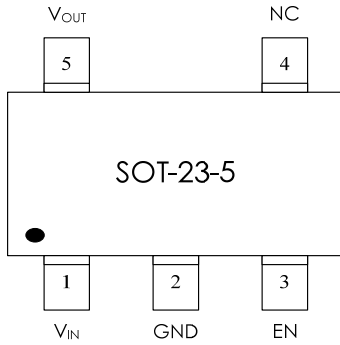
## Ordering Information

Part Number	Remark
EMP8041	±2.5% output voltage tolerance
EMP8041B	±1.0% output voltage tolerance

## Typical Application



## Connection Diagrams



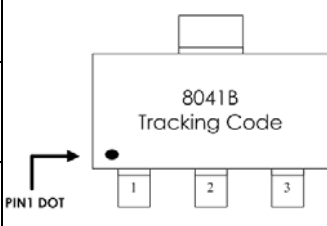
## Order information

EMP8041-XXVF05NRR/ EMP8041B-XXVF05NRR  
 XX Output voltage  
 VF05 SOT-23-5 Package  
 NRR RoHS & Halogen free package  
 Rating: -40 to 85°C  
 Package in Tape & Reel

EMP8041-XXVG03NRR/ EMP8041B-XXVG03NRR  
 XX Output voltage  
 VG03 SOT-89-3 Package  
 NRR RoHS & Halogen free package  
 Rating: -40 to 85°C  
 Package in Tape & Reel

## Order, Marking and Packing Information

Package	Vout	Product ID.	Marking	Packing
SOT-23-5	3.3V	EMP8041-33VF05NRR		Tape & Reel 3Kpcs
	5.0V	EMP8041-50VF05NRR		
SOT-89-3	3.3V	EMP8041-33VG03NRR		Tape & Reel 1Kpcs
	5.0V	EMP8041-50VG03NRR		
SOT-23-5	3.0V	EMP8041B-30VF05NRR		Tape & Reel 3Kpcs
	3.3V	EMP8041B-33VF05NRR		
	5.0V	EMP8041B-50VF05NRR		

SOT-89-3	3.0V	EMP8041B-30VG03NRR		Tape & Reel 1Kpcs
	3.3V	EMP8041B-33VG03NRR		
	5.0V	EMP8041B-50VG03NRR		

Pin Functions

Name	SOT-23-5	SOT-89-3	Function
V <sub>IN</sub>	1	3	<b>Supply Voltage Input</b> Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.
GND	2	2	<b>Ground Pin</b>
EN	3	N/A	<b>Shutdown Input</b> The EN pin is pulled "High" internally. Set the regulator into the disable mode by pulling the EN pin low.
NC	4	N/A	<b>No connection</b>
V <sub>OUT</sub>	5	1	<b>Output Voltage</b>

Functional Block Diagram

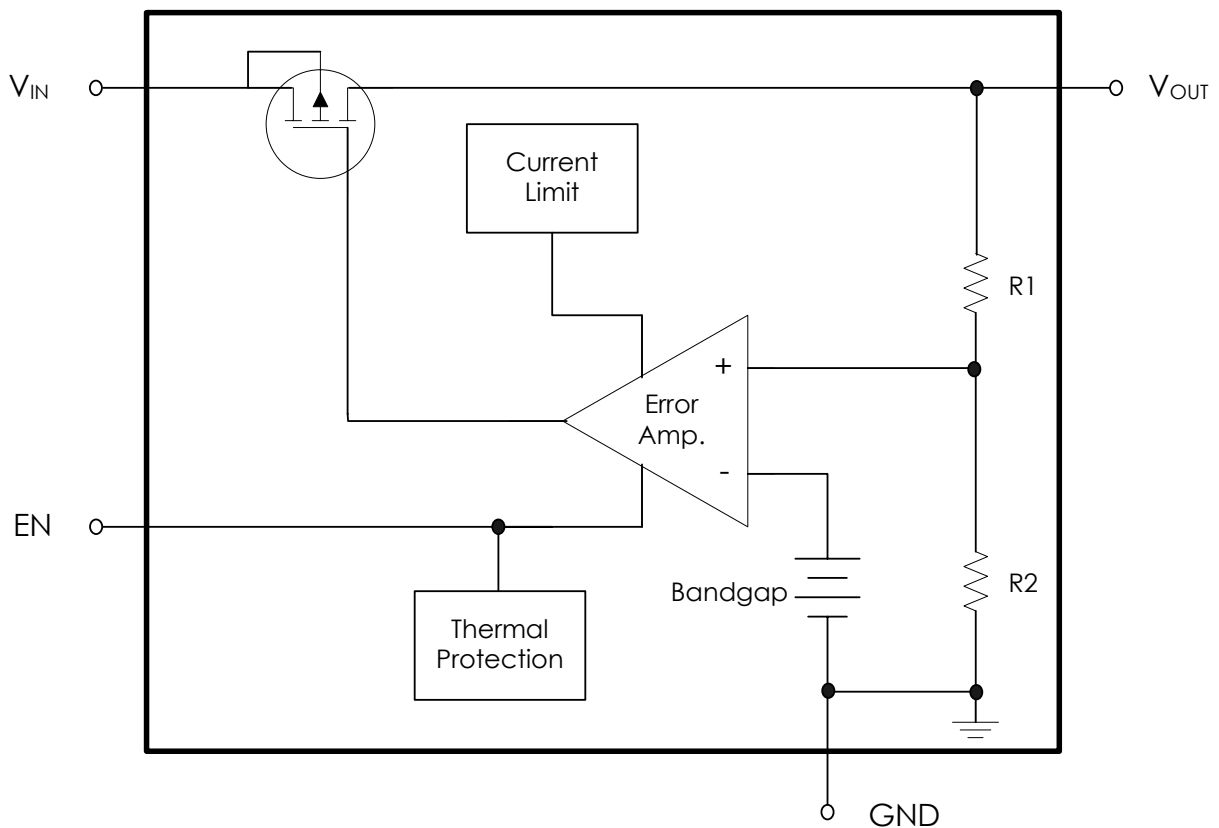


FIG.1. Functional Block Diagram of EMP8041

## Absolute Maximum Ratings (Notes 1, 2)

$V_{IN, EN}$	-0.3V to 42V	Junction Temperature ( $T_J$ )	160°C
$V_{OUT}$	-0.3V to 13.2V	Lead Temperature (Soldering, 10 sec.)	260°C
Power Dissipation	(Note 3)	ESD Rating	
Storage Temperature Range	-65°C to 150°C	Human Body Model	2KV

## Operating Ratings (Note 1, 2)

Supply Voltage (EMP8041)	3.0V to 40V	Thermal Resistance ( $\theta_{JA}$ , Note 3)	152°C/W (SOT-23-5)
<b>Supply Voltage (EMP8041B)</b>	<b>2.7V to 40V</b>		90°C/W (SOT-89-3)
Operating Temperature Range	-40°C to 85°C	Thermal Resistance ( $\theta_{JC}$ , Note 4)	81°C/W (SOT-23-5) 52°C/W (SOT-89-3)

## Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{OUT(NOM)} = 5\text{V}$ ; unless otherwise specified, all limits guaranteed for  $V_{IN} = V_{OUT} + 1\text{V}$ ,  $C_{IN} = C_{OUT} = 1\mu\text{F}$ .

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
$\Delta V_{OTL}$	Output Voltage Tolerance	$I_{OUT} = 10\text{mA}$ $V_{OUT(NOM)} + 1\text{V} \leq V_{IN} \leq 40\text{V}$	EMP8041	-2.5	+2.5	% of $V_{OUT(NOM)}$
			EMP8041B	-1	+1	
$I_{OUT}$	Maximum Output Current	Average DC Current Rating	150			mA
$I_{LIMIT}$	Output Current Limit		300			mA
$I_Q$	Supply Current	$I_{OUT} = 0.1\text{mA}$		12	30	$\mu\text{A}$
		$I_{OUT} = 100\text{mA}$		50	100	
		$I_{OUT} = 150\text{mA}$		80	130	
	Shutdown Supply Current	$V_{OUT} = 0\text{V}$ , $EN = \text{GND}$		1	5	
$V_{DO}$	Dropout Voltage $V_{OUT} = 5.0\text{V}$ (Note. 7)	$I_{OUT} = 30\text{mA}$		135		mV
		$I_{OUT} = 100\text{mA}$		500		
		$I_{OUT} = 150\text{mA}$		780		
$\Delta V_{OUT}$	Line Regulation	$I_{OUT} = 1\text{mA}$ , $(V_{OUT} + 1\text{V}) \leq V_{IN} \leq 40\text{V}$		0.1		%
	Load Regulation	$0.1\text{mA} \leq I_{OUT} \leq 100\text{mA}$		0.5		%
$e_n$	Output Voltage Noise	$I_{OUT} = 10\text{mA}$ , $10\text{Hz} \leq f \leq 100\text{kHz}$ $V_{OUT} = 5.0\text{V}$		800		$\mu\text{V}_{RMS}$
$V_{EN}$	EN Input Threshold	$V_{IH}$ , $(V_{OUT} + 1\text{V}) \leq V_{IN} \leq 40\text{V}$	1.0			V
		$V_{IL}$ , $(V_{OUT} + 1\text{V}) \leq V_{IN} \leq 40\text{V}$			0.3	
$I_{EN}$	EN Input Bias Current	$EN = \text{GND}$ or $V_{IN}$		0.1		$\mu\text{A}$
$T_{SD}$	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			30		
$t_{ON}$	Start-Up Time	$C_{OUT} = 1.0\mu\text{F}$ , $V_{OUT}$ at 90% of Final Value		500		$\mu\text{s}$

**Note 1:** Absolute maximum ratings indicate limits beyond which damage may occur.

**Note 2:** All voltages are in respect to the potential of the ground pin.

**Note 3:**  $\theta_{JA}$  is measured in the natural convection at  $T_A=25^\circ\text{C}$  on a high effectively thermal conductivity test board (2 layers, 2SOP).

**Note 4:**  $\theta_{JC}$  represents the resistance between the chip and the top of the package case.

**Note 5:** Maximum power dissipation for the device is calculated using the following equation:

$$P_D = \frac{T_{J(\text{MAX})} - T_A}{\theta_{JA}}$$

Where  $T_{J(\text{MAX})}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance. For example, for the SOT-89-3 package  $\theta_{JA}=90^\circ\text{C}/\text{W}$ ,  $T_{J(\text{MAX})}=160^\circ\text{C}$  and using  $T_A=25^\circ\text{C}$ , the maximum power dissipation is 1.5W.

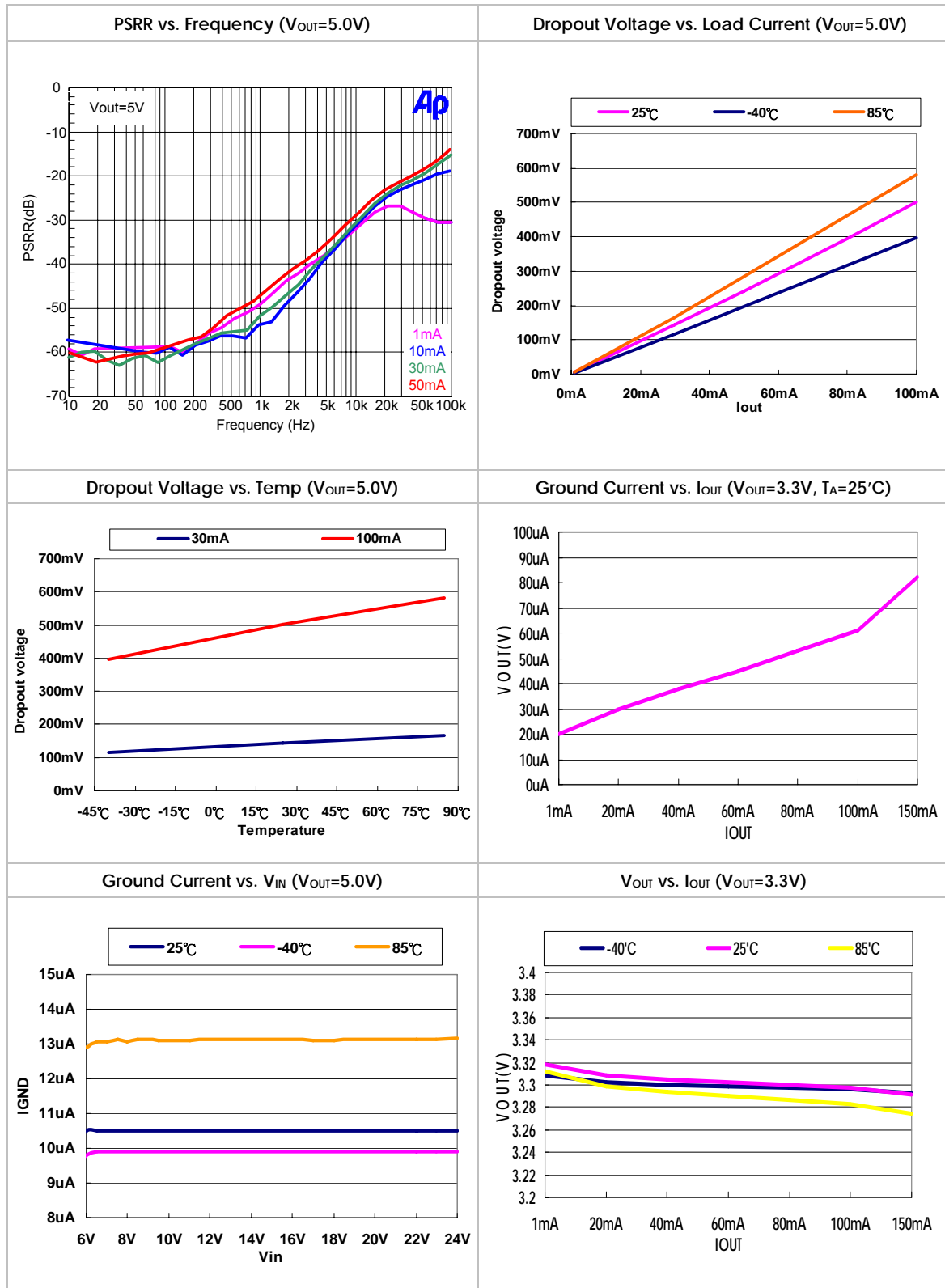
The derating factor  $(-1/\theta_{JA})=-11.1\text{mW}/^\circ\text{C}$ . Below  $25^\circ\text{C}$  the power dissipation figure can be increased by 11.1mW per degree and similarly decreased by this factor for temperatures above  $25^\circ\text{C}$ .

**Note 6:** Typical values represent the most likely parametric norm.

**Note 7:** Dropout voltage is measured by reducing  $V_{IN}$  until  $V_{OUT}$  drops to 98% its nominal value.

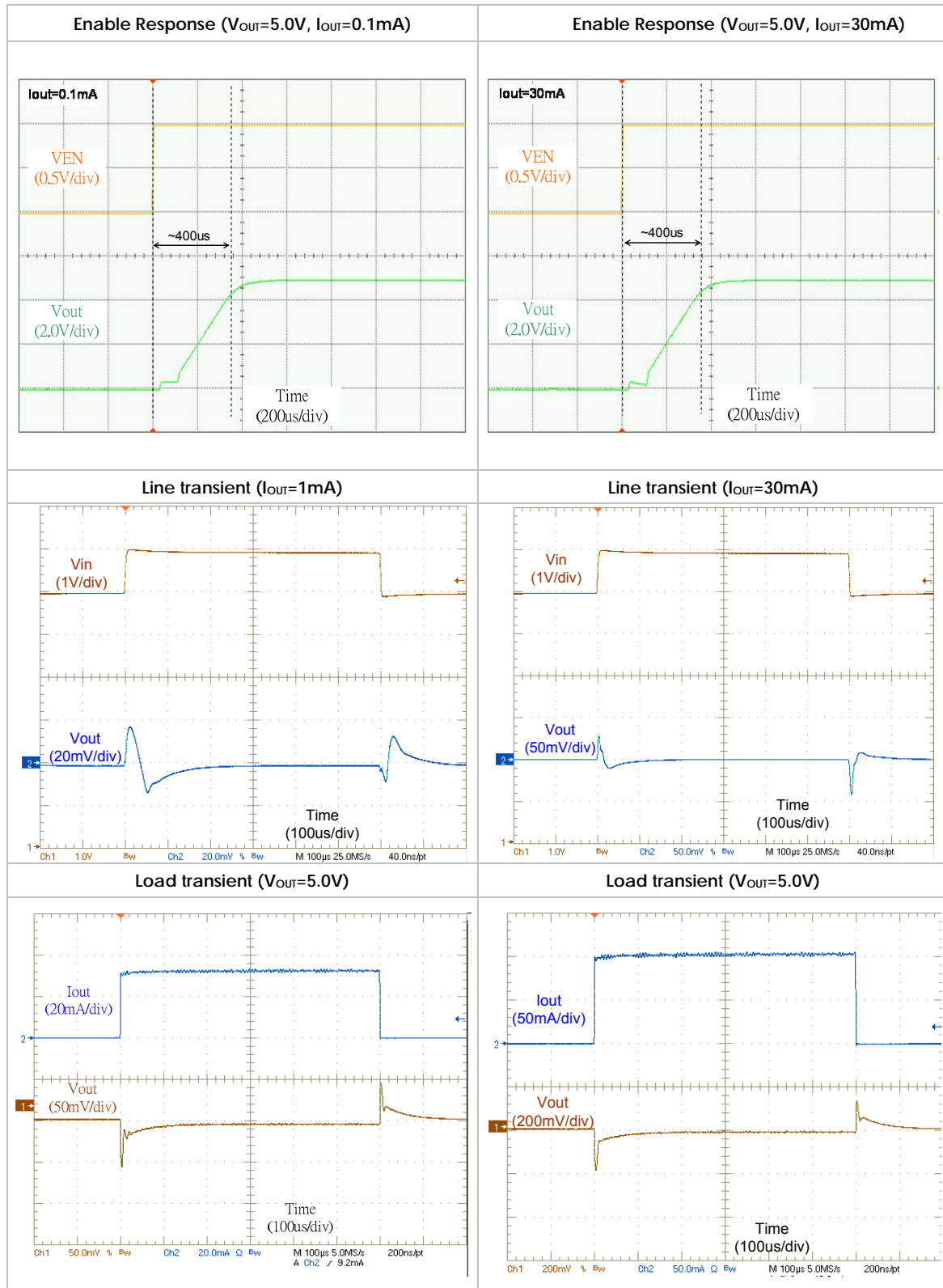
## Typical Performance Characteristics

Unless otherwise specified,  $V_{IN} = V_{OUT(NOM)} + 1V$ ,  $V_{OUT} = 5V$ ,  $C_{IN} = C_{OUT} = 1.0\mu F$ ,  $T_A = 25^\circ C$ ,  $EN = 2V$



## Typical Performance Characteristics (cont.)

Unless otherwise specified,  $V_{IN} = V_{OUT(NOM)} + 1V$ ,  $V_{OUT} = 5.0V$ ,  $C_{IN} = C_{OUT} = 1.0\mu F$ ,  $T_A = 25^\circ C$





---

## Application Information

### General Description

Referring to Fig.1 as shown in the Functional Block Diagram section, the EMP8041 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By the virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

### Output Capacitor

The EMP8041 is specially designed for use with ceramic output capacitors of as low as 1.0 $\mu$ F to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) is restricted to less than 0.5 $\Omega$ . The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8041 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within  $\pm 20\%$  and  $\pm 10\%$ , respectively, as the temperature increases.

### No-Load Stability

The EMP8041 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

### Input Capacitor

A minimum input capacitance of 1 $\mu$ F is required for EMP8041. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10 $\mu$ F tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

**Power Dissipation and Thermal Shutdown**

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The EMP8041 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature  $T_J$  exceeding 160°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance  $\theta_{JA}$  (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between  $\theta_{JA}$  and  $T_J$  is as follows:

$$T_J = \theta_{JA} \times (P_D) + T_A$$

$T_A$  is the ambient temperature, and  $P_D$  is the power generated by the IC and can be written as:

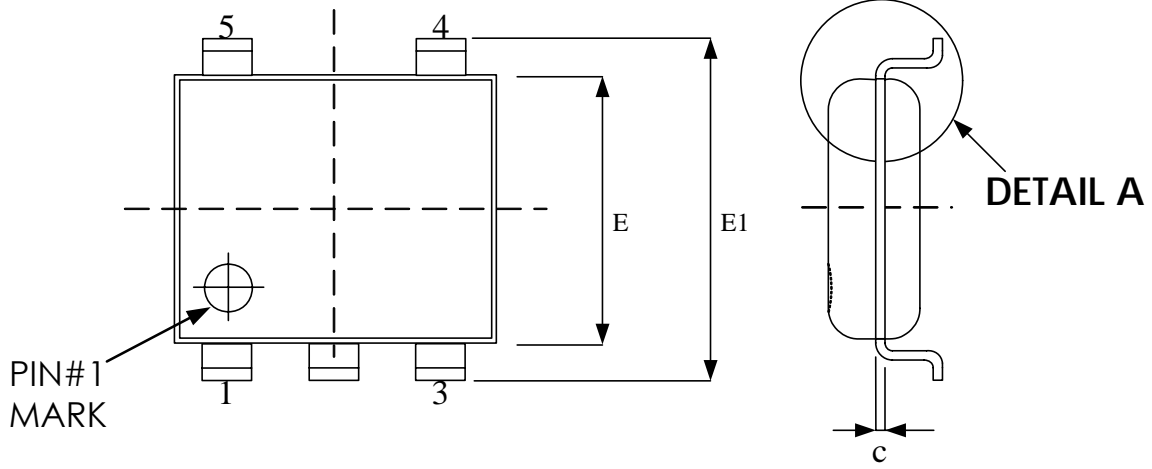
$$P_D = I_{OUT} (V_{IN} - V_{OUT})$$

As the above equations show, it is desirable to work with ICs whose  $\theta_{JA}$  values are small such that  $T_J$  does not increase strongly with  $P_D$ . To avoid thermally overloading the EMP8041, refrain from exceeding the absolute maximum junction temperature rating of 160°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

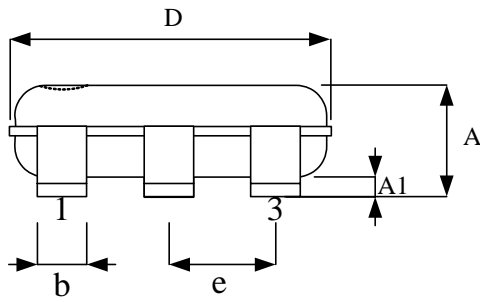
**Shutdown**

The EMP8041 enters the sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1µA. Such a low supply current makes the EMP8041 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin for the sleep mode to take effect is 0.3V. The EN pin is pulled high internally.

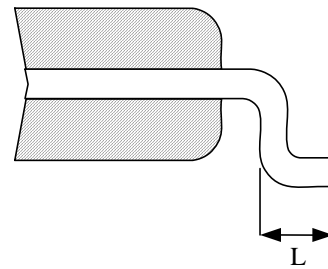
Package Outline Drawing  
SOT-23-5



TOP VIEW



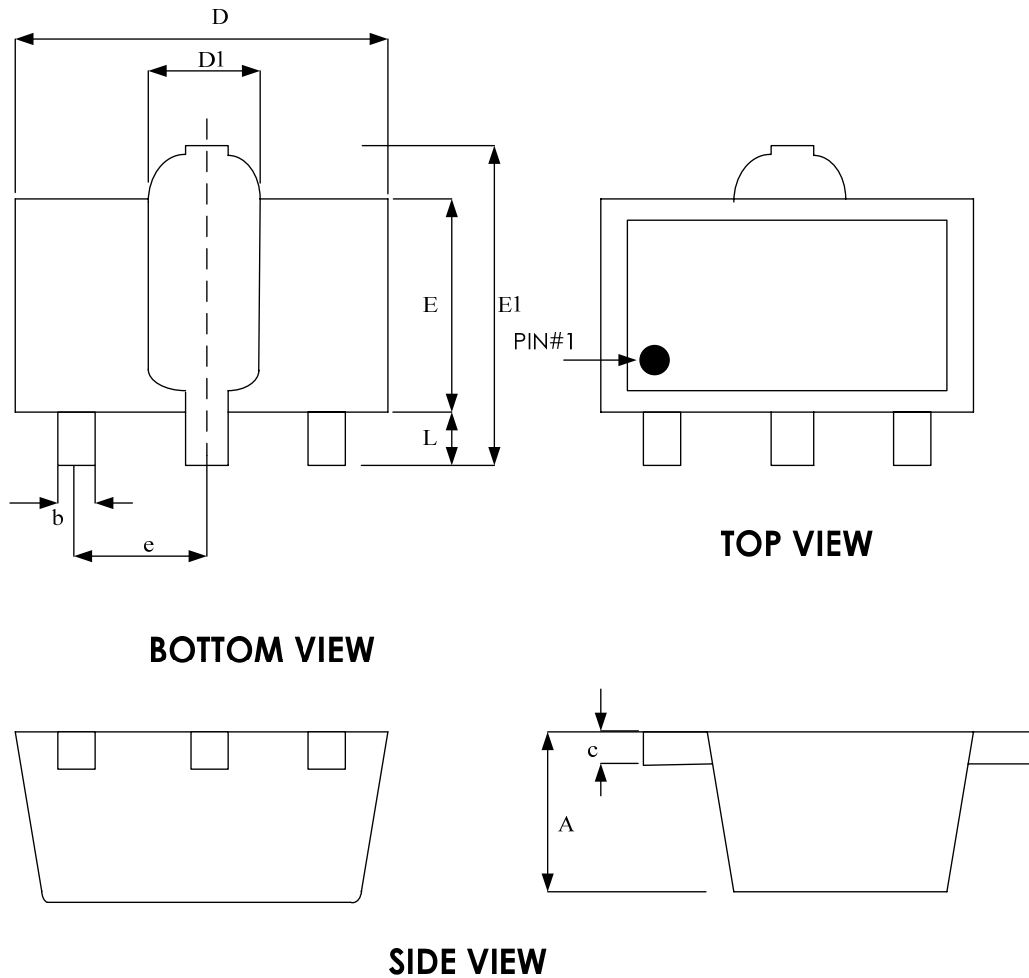
SIDE VIEW



DETAIL A

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

Package Outline Drawing  
SOT-89-3



Symbol	Dimension in mm	
	Min	Max
A	1.4	1.6
b	0.4	0.56
c	0.35	0.41
D	4.4	4.6
D1	1.5	1.83
E	2.29	2.6
E1	3.94	4.25
e	1.50 BSC	
L	0.89	1.2

## Revision History

Revision	Date	Description
0.1	2010.05.05	Original
0.2	2010.8.27	1) Updated output voltage option 2) Revised Iq spec.
1.0	2011.2.23	Skip "Preliminary"
1.1	2011.12.13	1) Modified 100mA output driving capacity to 150mA. 2) Modified the output voltage accuracy is based on Iout=10mA this condition. 3) Added Iout=150mA spec. into electrical characteristics table.
1.2	2012.03.29	1) Modified the operating voltage from 36V to 40V. 2) Modified the absolute maximum ratings VIN, EN from 40V to 42V. 3) Updated the package outline drawing.
1.3	2013.10.17	Modify package outline drawing
1.4	2017.06.26	<b>Added EMP8041B series product</b>

## Important Notice

All rights reserved.

No part of this document may be reproduced or duplicated in any form or by any means without the prior permission of ESMT.

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.