Fast Ultra High-PSRR, Low-Noise, 300mA CMOS Linear Regulator

General Description

The EMP8736 features ultra-high power supply rejection ratio, low output voltage noise, low dropout voltage, low quiescent current and fast transient response. It guarantees delivery of 300mA output current and supports adjustable output voltages by using two external resistors.

Based on its low quiescent current consumption and its less than 1μA shutdown mode of logical operation, the EMP8736 is ideal for battery-powered applications. The high power supply rejection ratio of the EMP8736 holds well for low input voltages typically encountered in battery-operated systems. The regulator is stable with small ceramic capacitive loads (1μF typical). The EMP8736 is available in miniature SOT-23-5 packages.

Features

- 300mA guaranteed output current
- 65dB typical PSRR at 1kHz
- 110μV RMS output voltage noise (10Hz to 100kHz)
- 290mV typical dropout at 300mA
- 57μA typical quiescent current
- Less than 1μA typical shutdown mode
- Fast line and load transient response
- 2.2V to 5.5V input range
- Auto-discharge during chip disable
- 80μs typical turn-on time
- Stable with small ceramic output capacitors
- Over temperature and over current protection
- ±2% output voltage tolerance

Applications

- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

Typical Application

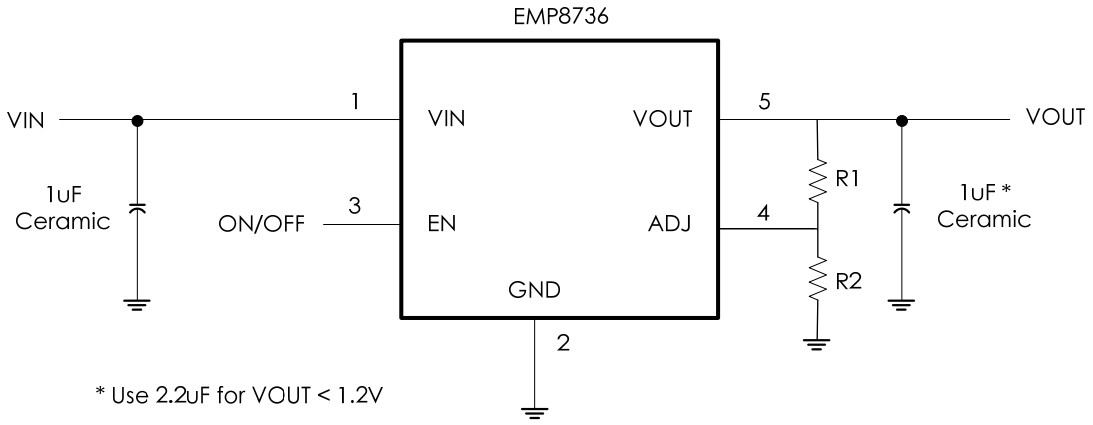
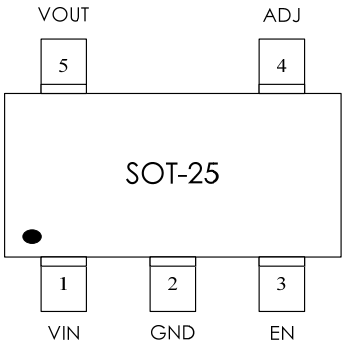


Fig 1. The typical application circuit.

Connection Diagram

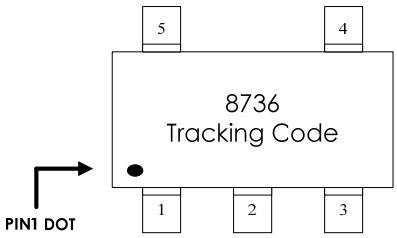


Order Information

EMP8736-XXVF05NRR

XX	Output Voltage
VF05	SOT-25 Package
NRR	RoHS & Halogen free
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Mark & Packing Information

Marking	Vout	Product ID	Packing
	Adj	EMP8736-00VF05NRR	Tape & Reel 3Kpcs

Pin Functions

Name	SOT-23-5	Function
VIN	**1**	**Supply Voltage Input** Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.
GND	**2**	**Ground Pin**
EN	**3**	**Enable Input** Enable the regulator by pulling the EN pin High. To keep the regulator on during normal operation, connect the EN pin to VIN. The EN pin must not exceed VIN under all operating conditions.
ADJ	**4**	**Adjustable Control** Use external resistors to achieve desired output voltage.
VOUT	**5**	**Output Voltage Feedback**

Functional Block Diagram

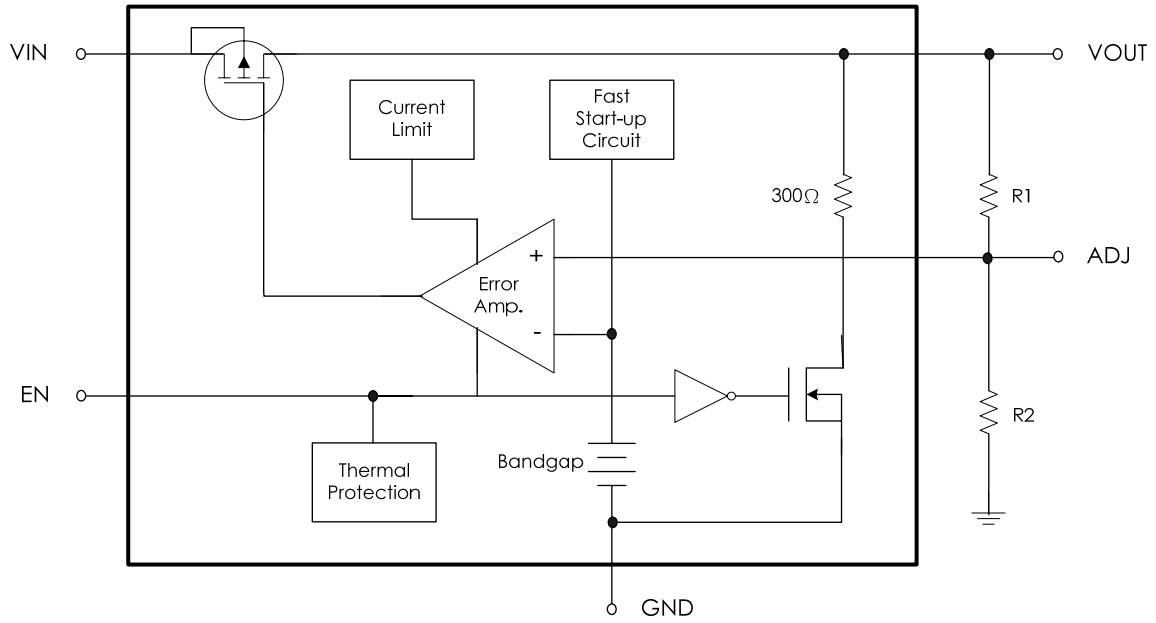


Fig 2. The EMP8736 Functional Block Diagram

Absolute Maximum Ratings (Notes 1, 2)

VIN, VOUT, VEN	-0.3V to 6.0V	ESD Rating	
Storage Temperature Range	-65°C to150°C	Human Body Model	2kV
Junction Temperature (T_J)	150°C	MM	200V
Lead Temperature (10 sec.)	260°C	Power Dissipation	(Note 6)

Operating Ratings (Note 2)

Supply Voltage	2.2V to 5.5V	Thermal Resistance (θ_{JA})	
Temperature Range	-40°C to 85°C	SOT-25	250°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V_{IN} = V_{OUT}$ +1V (Note 3), $V_{EN}=V_{IN}$, $C_{IN} = C_{OUT}$ = 2.2µF, T_A = 25°C.
Boldface limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		**2.2**		**5.5**	V
V_{OUT}	Output Voltage		**1.0**		**4.5**	V
V_{ADJ}	Feedback Voltage			0.894		V
ΔV_{OTL}	Output Voltage Tolerance	1mA ≤ I_{OUT} ≤ 300mA $V_{OUT\ (NOM)}$ +1V ≤ VIN ≤ 5.5V (Note 3)	-2		+2	% of $V_{OUT\ (NOM)}$
			-3		**+3**	
I_{OUT}	Maximum Output Current	Average DC Current Rating	**300**			mA
I_{LIMIT}	Output Current Limit		**300**	450		mA
I_Q	Supply Current	I_{OUT} = 0mA		57		µA
		I_{OUT} = 300mA		130		
	Shutdown Supply Current	V_{OUT} = 0V, EN = GND		0.001	1	
V_{DO}	Dropout Voltage (Note4)	I_{OUT} = 100mA		90		mV
		I_{OUT} = 300mA		290		
ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V (Note 3)	-0.1	0.01	0.1	%/V
	Load Regulation	1mA ≤ I_{OUT} ≤ 300mA		0.0008		%/mA
e_n	Output Voltage Noise	V_{OUT}=2.5V, I_{OUT} = 10mA, 10Hz ≤ f ≤ 100kHz		110		μV_{RMS}
T_{SD}	Thermal Shutdown Temperature			165		℃
	Thermal Shutdown Hysteresis			35		
V_{EN}	EN Input Threshold	V_{IH}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V (Note 3)	**1.2**			V
		V_{IL}, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V (Note 3)			**0.4**	
I_{EN}	EN Input Bias Current	EN = GND or VIN		0.1	100	nA
T_{ON}	Turn-On Time	V_{OUT} at 95% of Final Value		80		µs
T_{OFF}	Turn-Off Time	I_{OUT}=0mA (Note 5)		2.4		ms

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: Condition does not apply to input voltages below 2.2V since this is the minimum input operating voltage.

Note 4: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} -V_{OUT} = 1V. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 2.2V.

Note 5: Turn-off time is time measured between the enable input just decreasing below V_{IL} and the output voltage just decreasing to 10% of its nominal value.

Note 6: Maximum Power dissipation for the device is calculated using the following equations:

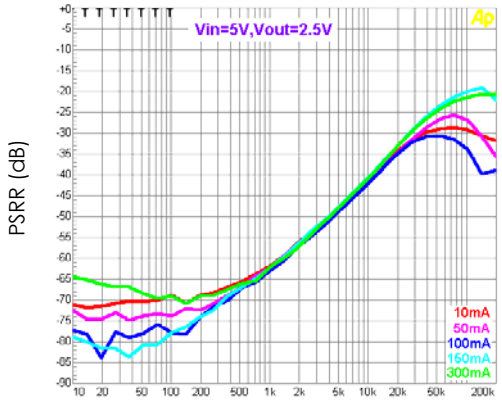
$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the SOT-25 package θ_{JA} = 250°C/W, $T_{J(MAX)}$ = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 500mW. The derating factor (-1/θ_{JA}) = -4mW/°C, thus below 25°C the power dissipation figure can be increased by 4mW per degree, and similarity decreased by this factor for temperatures above 25°C. The value of the θ_{JA} for the FBP-6 package is specifically dependent on the PCB trace area, trace material, and the number of layers and thermal vias.

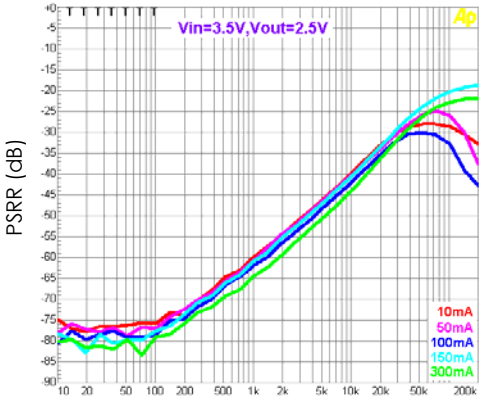
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = C_{OUT} = 2.2µF, T_A = 25°C.

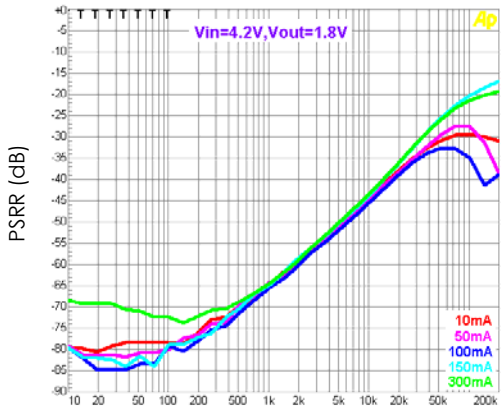
PSRR vs. Frequency



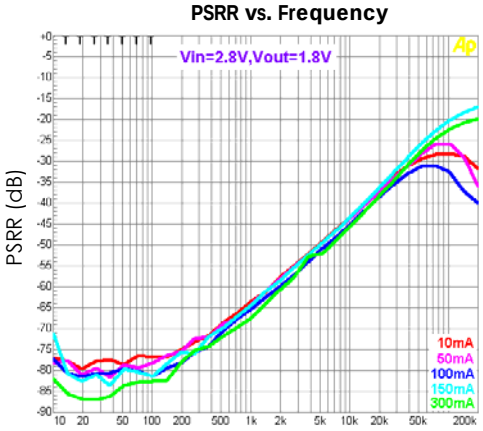
PSRR vs. Frequency



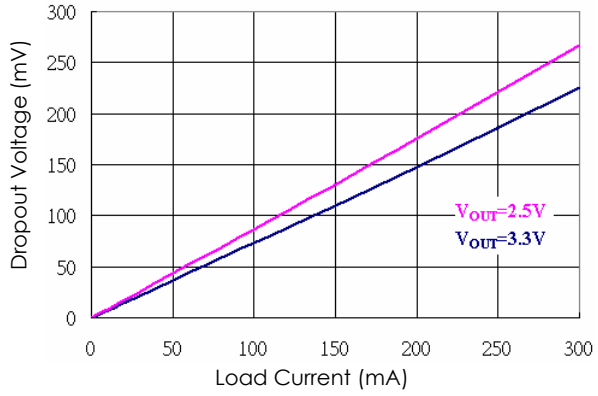
PSRR vs. Frequency



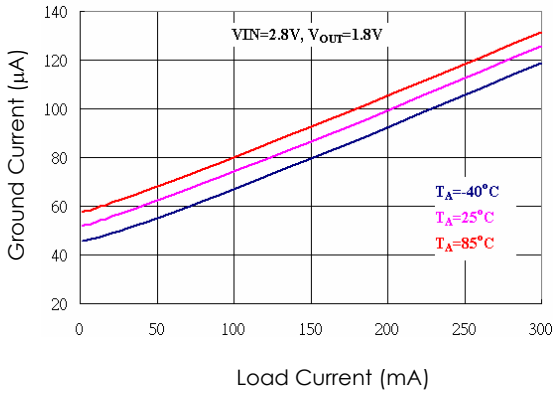
PSRR vs. Frequency



Dropout Voltage vs. Load Current



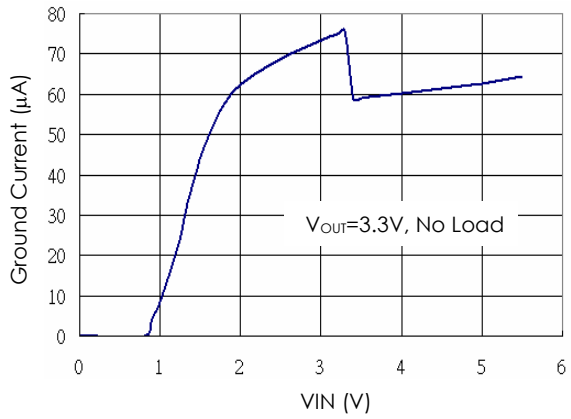
Ground Current vs. Load Current



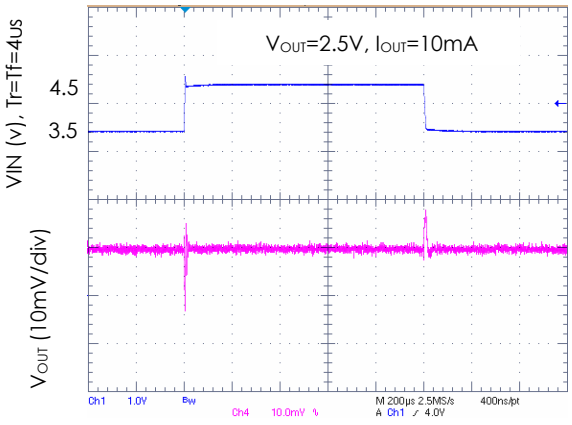
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = C_{OUT} = 2.2μF, T_A = 25°C. (Continued)

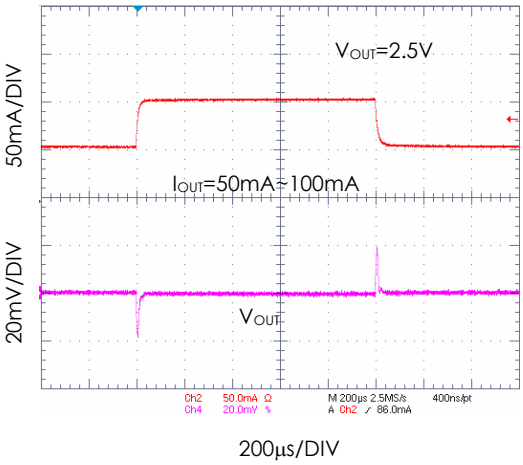
Ground Current vs. VIN



Line Transient



Load Transient



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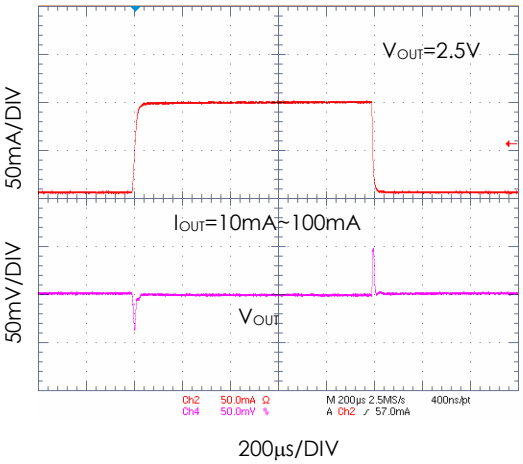
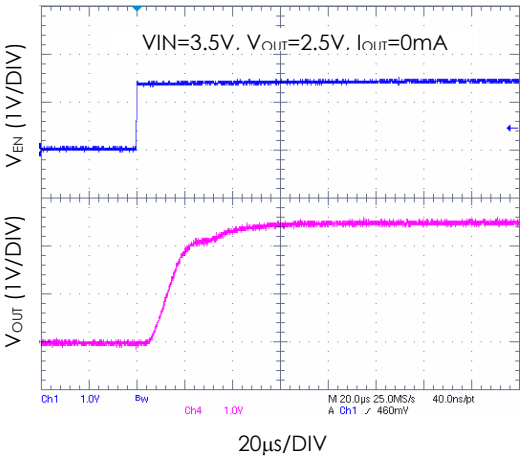


Enable Response



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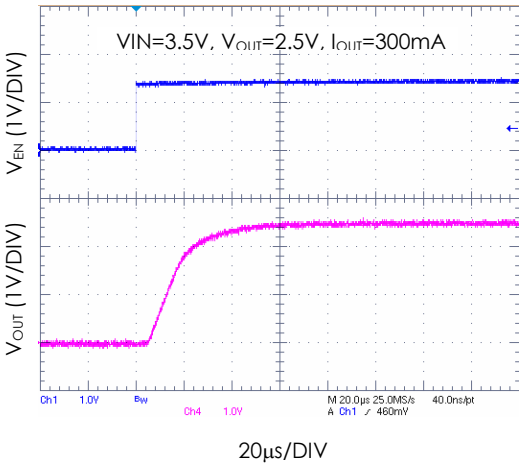
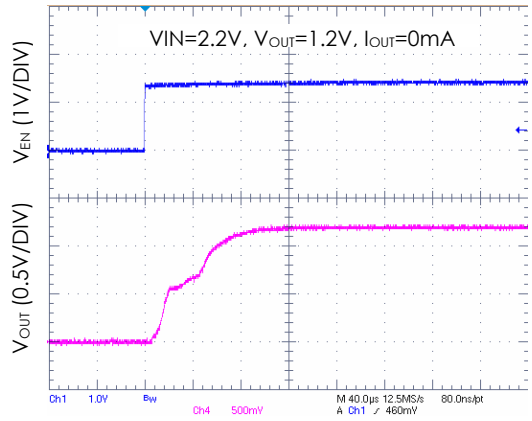


Typical Performance Characteristics

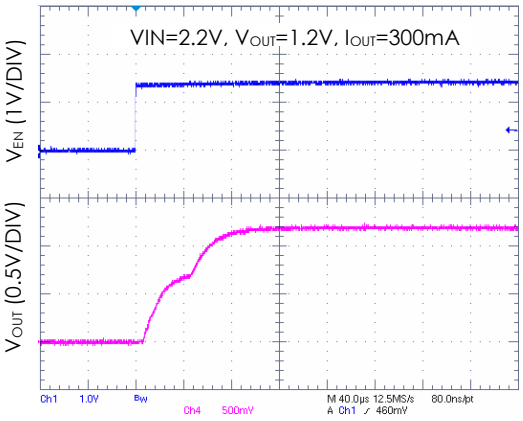
Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} = C_{OUT} = 2.2µF, T_A = 25°C. (Continued)

Enable Response



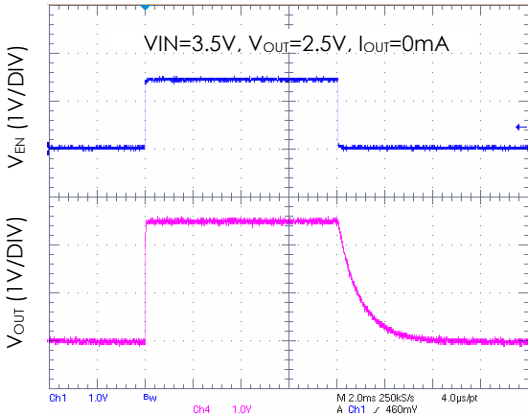
40µs/DIV

Enable Response



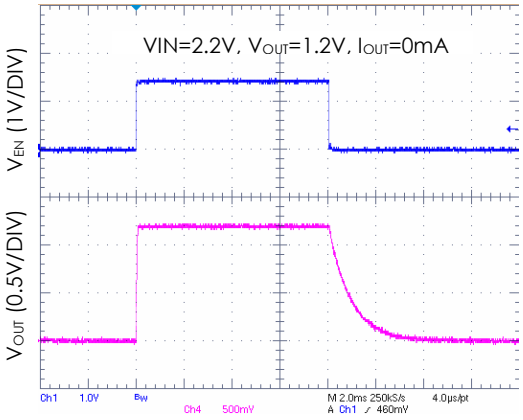
40µs/DIV

Disable Response



2ms/DIV

Disable Response



2ms/DIV

Application Information

General Description

Referring to Figure 2 as shown in the Functional Block Diagram section, the EMP8736 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage. These feedback resistors can be either internal or external to the EMP8736, depending on whether a preset or an adjustable output voltage version is being used.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Voltage Control

The EMP8736 allows direct user control of the output voltage in accordance with the amount of negative feedback present. To see the explicit relationship between the output voltage and the negative feedback, it is convenient to conceptualize the EMP8736 as an ideal non-inverting operational amplifier with a fixed DC reference voltage VREF at its non-inverting input. Such a conceptual representation of the EMP8736 in closed-loop configuration is shown in Figure 3. This ideal op amp features an ultra-high input resistance such that its inverting input voltage is virtually fixed at VREF. The output voltage is therefore given by:

$$V_{OUT} = V_{REF}\left[\frac{R_1}{R_2} + 1\right]$$

This equation can be rewritten in the following form to facilitate the determination of the resistor values for a chosen output voltage:

$$R_1 = R_2\left[\frac{V_{OUT}}{0.894V} - 1\right]$$

Set R2 equal to 100kΩ to optimize for overall accuracy, power supply rejection, noise, and power consumption.

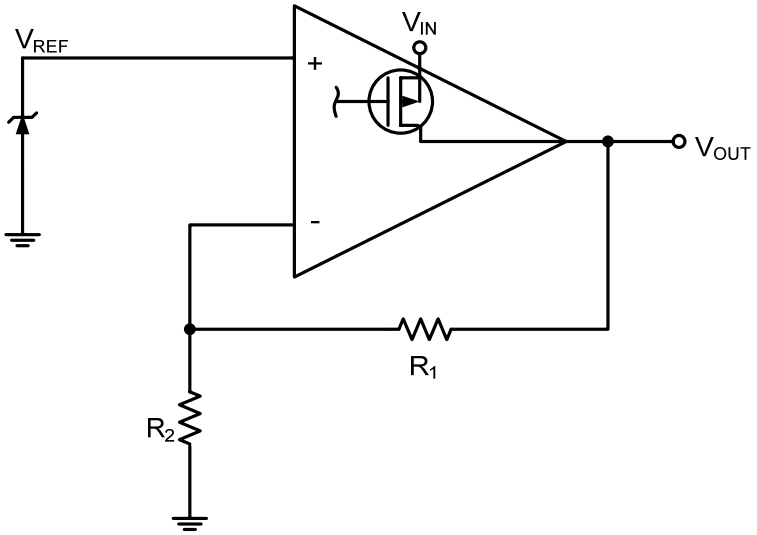


Fig 3. Simplified Regulator Topology

Output Capacitor

The EMP8736 is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8736 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8736 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8736. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The EMP8736 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature TJ exceeding 165°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$T_J = \theta_{JA} \times (PD) + T_A$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

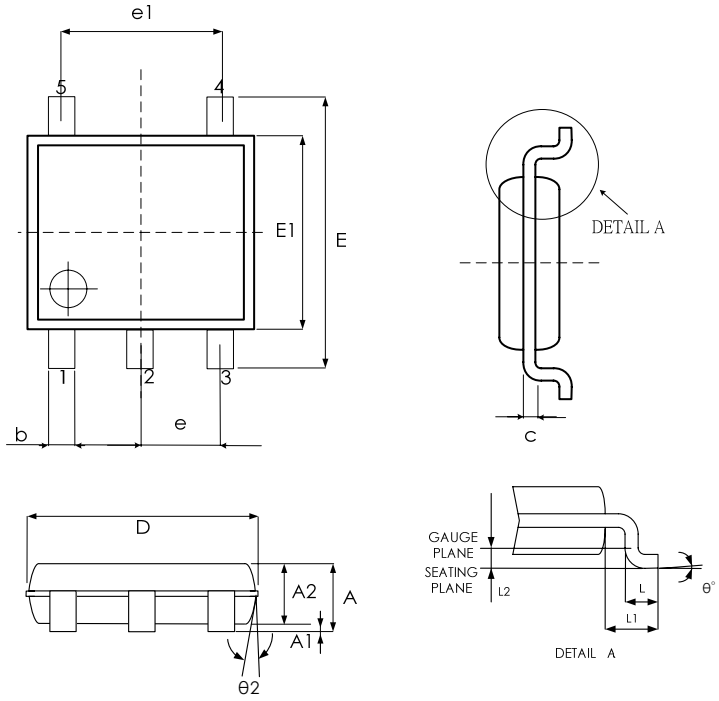
$P_D = I_{OUT} (V_{IN} - V_{OUT})$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8736, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

Shutdown

The EMP8736 enters the sleep mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1nA. Such a low supply current makes the EMP8736 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin for the sleep mode to take effect is 0.4V. A minimum guaranteed voltage of 1.2V at the EN pin will activate the EMP8736. Direct connection of the EN pin to the VIN to keep the regulator on is allowed for the EMP8736. In this case, the EN pin must not exceed the supply voltage VIN.

Package Outline drawing
SOT-23-5



SYMBPLS	MIN.	NOM.	MAX.
A	1.05	1.20	1.35
A1	0.05	0.10	0.15
A2	1.00	1.10	1.20
b	0.30	—	0.50
c	0.08	—	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.55
L1	0.60 REF		
L2	0.25 REF		
θ°	0	5	10
θ2°	6	8	10

UNIT: MM

Revision History

Revision	Date	Description
1.0	2009.11.17	Original

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