Fast Ultra High-PSRR, Low-Noise, Low-Dropout, 300mA Micropower CMOS Linear Regulator

General Description

The EMP893X series is a family of CMOS linear regulators. It is consisted of EMP8935, EMP8936 and EMP8938, featuring ultra-high power supply rejection ratio, low output voltage noise, low dropout voltage, low quiescent current and fast transient response. It guarantees delivery of 300mA output current, and supports preset 1.2V, 1.5V, 1.8V, 2.5V, 2.7V, 2.8V, 3.0V, 3.3V output voltage versions.

Based on its low quiescent current consumption and its less than 1μA shutdown mode of logical operation, the EMP893X is ideal for battery-powered applications. It provides fast turn-on and start-up time by using dedicated circuitry to pre-charge an optional external bypass capacitor. This bypass capacitor is used to reduce the output voltage noise without adversely affecting the load transient response. The high power supply rejection ratio of the EMP893X holds well for low input voltages typically encountered in battery-operated systems. The regulator is stable with small ceramic capacitive loads (2.2μF typical).

Additional features include regulation fault detection, bandgap voltage reference, constant current limiting and thermal overload protection. The EMP893X is Available in miniature SOT-23-5, SOT-23-6, TDFN-6 and MSOP-8 packages.

EMP products is RoHS compliant.

Features

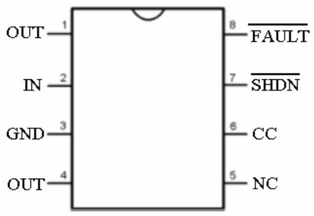
- Miniature SOT-23-5, SOT-23-6, MSOP-8 and TDFN-6 packages
- 300mA guaranteed output current
- 75dB typical PSRR at 1kHz (60dB typical at 10KHz)
- 30μV RMS output voltage noise (10Hz to 100kHz)
- 110mV typical dropout at 300mA for MSOP-8
- 106μA typical quiescent current
- less than 1μA typical shutdown mode
- Fast line and load transient response
- 80μs typical fast turn-on time
- 2.5V to 5.5V input range
- Stable with small ceramic output capacitors
- Over temperature and over current protection
- ±2% output voltage tolerance

Applications

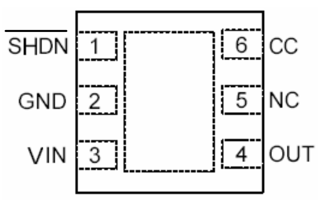
- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

Connection Diagrams

MSOP-8(TOP View)

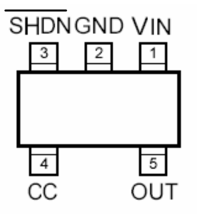


TDFN-6(TOP View)

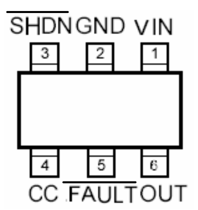


Note: Version also available for pin #1 as FAULT pin and pin #5 as SHDN pin

SOT-23-5(TOP View)



SOT-23-6(TOP View)



Order information

EMP8938-XXMA08GRR/NRR

XX	Operation Code
MA08	MSOP-8 Package
GRR	RoHS (Pb Free)
	Rating: -40 to 85°C
	Package in Tape & Reel
NRR	RoHS & Halogen free (By Request)
	Rating: -40 to 85°C
	Package in Tape & Reel

EMP8935-XXFE06NRR

XX	Operation Code
FE06	TDFN-6 Package
NRR	RoHS & Halogen free
	Rating: -40 to 85°C
	Package in Tape & Reel

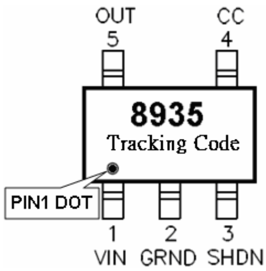
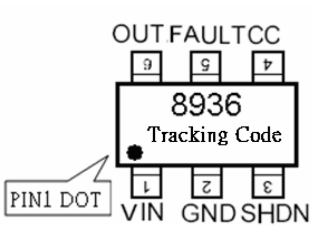
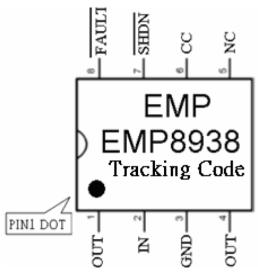
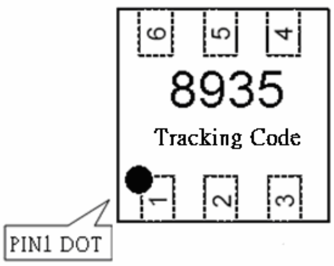
EMP8935-XXVF05GRR/NRR

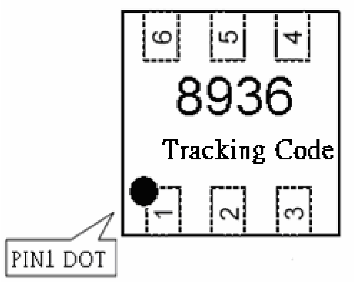
XX	Operation Code
VF05	SOT-23-5 Package
GRR	RoHS (Pb Free)
	Rating: -40 to 85°C
	Package in Tape & Reel
NRR	RoHS & Halogen free (By Request)
	Rating: -40 to 85°C
	Package in Tape & Reel

EMP8936-XXVC06GRR/NRR

XX	Operation Code
VC06	SOT-23-6 Package
GRR	RoHS (Pb Free)
	Rating: -40 to 85°C
	Package in Tape & Reel
NRR	RoHS & Halogen free (By Request)
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Mark & Packing Information

No. of PIN	EN	CC	Fault	Package	Marking	Vout	Product ID
5	Y	Y	N	SOT-23-5		1.2	EMP8935-12VF05GRR
						1.5	EMP8935-15VF05GRR
						1.8	EMP8935-18VF05GRR
						2.5	EMP8935-25VF05GRR
						2.7	EMP8935-27VF05GRR
						2.8	EMP8935-28VF05GRR
						3.0	EMP8935-30VF05GRR
						3.3	EMP8935-33VF05GRR
6	Y	Y	Y	SOT-23-6		1.2	EMP8936-12VC06GRR
						1.5	EMP8936-15VC06GRR
						1.8	EMP8936-18VC06GRR
						2.5	EMP8936-25VC06GRR
						2.7	By request
						2.8	By request
						3.0	By request
						3.3	By request
8	Y	Y	Y	MSOP-8		1.2	By request
						1.5	By request
						1.8	By request
						2.5	By request
						2.7	By request
						2.8	By request
						3.0	By request
						3.3	By request
5	Y	Y	N	TDFN-6		1.2	By request
						1.5	By request
						1.8	By request
						2.5	By request
						2.7	By request
						2.8	By request
						3.0	By request
						3.3	By request

6	Y	Y	Y	TDFN-6		1.2	By request
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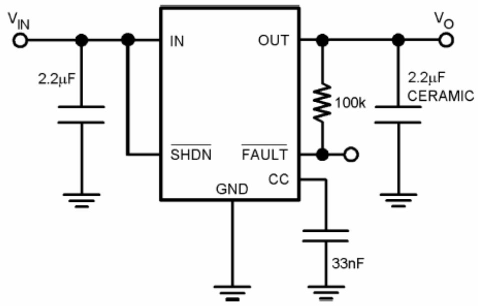
						2.5	By request
						2.7	By request
						2.8	By request
						3.0	By request
						3.3	By request

Old Marking: please see the notice(Page 20)

Package & Packing

SOT-23-5	3K units Tape & Reel
SOT-23-6	3K units Tape & Reel
MSOP-8	3K units Tape & Reel
TDFN-6	5K units Tape & Reel

Typical Application



Pin Functions

Name	MSOP-8	SOT-23-5	SOT-23-6	TDFN-6	Function
VOUT	1, 4	5	6	4	**Output Voltage Feedback**.
VIN	2	1	1	3	**Supply Voltage Input**. Require a minimum input capacitor of close to 1µF to ensure stability and sufficient decoupling from the ground pin.
GND	3	2	2	2	**Ground Pin**.
NC	5			5 or N/A	**No Connection**
CC	6	4	4	6	**Compensation Capacitor**. Connect an optimum 33nF noise bypass capacitor between the CC and the ground pins to reduce noise in VOUT.
$\overline{\text{SHDN}}$	7	3	3	1 or 5	**Shutdown Input.** Set the regulator into the disable mode by pulling the $\overline{\text{SHDN}}$ pin low. To keep the regulator on during normal operation, connect the $\overline{\text{SHDN}}$ pin to VIN. The $\overline{\text{SHDN}}$ pin must not exceed VIN under all operating conditions.
$\overline{\text{FAULT}}$	8		5	N/A or 1	**Fault Detection Output.** The $\overline{\text{FAULT}}$ pin goes low when the voltage regulating function fails. Because the $\overline{\text{FAULT}}$ pin connects to the open-drain output of a NMOS transistor, a typical 100k Ω pull-up resistor is required to provide the necessary output voltage. The $\overline{\text{FAULT}}$ pin enters the high impedance state during shutdown and it should be connected to ground if unused.

Absolute Maximum Ratings (Notes 1, 2)

VIN, VOUT, $V_{\overline{SHDN}}$, VSET, VCC, $V_{\overline{FAULT}}$	-0.3V to 6.5V
Power Dissipation	(Note 3)
Storage Temperature Range	-65°C to160°C
Junction Temperature (TJ)	150°C
Lead Temperature (10 sec.)	260°C
ESD Rating	
Human Body Model (Note 5)	2kV
Thermal Resistance (θJA)	
MSOP-8	223°C/W
TDFN-6	(Note 3)
SOT-23-5	250°C/W
SOT-23-6	250°C/W

Operating Ratings (Note 1, 2)

Temperature Range	-40°C to 85°C
Supply Voltage	2.5V to 5.5V

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V_{IN} = V_{OUT}$ +0.5V (Note 6), $V_{\overline{SHDN}} = V_{IN}$, $C_{IN} = C_{OUT}$ = 2.2µF, C_{CC} = 33nF, T_J = 25°C. **Boldface** limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units
V_{IN}	Input Voltage		**2.5**		**5.5**	V
ΔV_{OTL}	Output Voltage Tolerance	100µA ≤ I_{OUT} ≤ 300mA $V_{IN} = V_{OUT\ (NOM)}$ +0.5V ≤ V_{IN} ≤ 5.5V , (Note 6)	-2		+2	% of $V_{OUT\ (NOM)}$
			-3		**+3**	
I_{OUT}	Maximum Output Current	Average DC Current Rating	**300**			mA
I_{LIMIT}	Output Current Limit		**330**	550		mA
I_Q	Supply Current	I_{OUT} = 0mA		106	200 **270**	µA
		I_{OUT} = 300mA		180		
	Shutdown Supply Current	V_{OUT} = 0V, $\overline{SHDN}$ = GND		0.001		
V_{DO}	Dropout Voltage (MSOP-8) (Note 4), (Note 6)	I_{OUT} = 1mA		0.02		mV
		I_{OUT} = 200mA		75	190	
		I_{OUT} = 300mA		110	280	
	Dropout Voltage (SOT-23-5, SOT-23-6, DFN-6) (Note 4), (Note 6)	I_{OUT} = 1mA		0.03		
		I_{OUT} = 200mA		90	190	
		I_{OUT} = 300mA		130	280	
ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 4)	-0.1	0.02	0.1	%/V
	Load Regulation	100µA ≤ I_{OUT} ≤ 300mA		0.0003	0.005	%/mA
e_n	Output Voltage Noise	I_{OUT} = 10mA, 10Hz ≤ f ≤ 100kHz		30		$µV_{RMS}$
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Threshold	V_{IH}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 4)	**1.2**			V
		V_{IL}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 4)			**0.4**	
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ = GND or VIN		0.1	100	nA
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Detection Voltage (MSOP-8)	V_{OUT} ≥ 2.5V, I_{OUT} = 200mA (Note 8)		110	330	mV

	$\overline{FAULT}$ Detection Voltage (SOT-23-5, SOT-23-6)	V_{OUT} ≥ 2.5V, I_{OUT} = 200mA (Note 8)		125	330	
	$\overline{FAULT}$ Output Low Voltage	I_{SINK} = 2mA		0.2	**0.4**	V
$I_{\overline{FAULT}}$	$\overline{FAULT}$ Off-Leakage Current	$\overline{FAULT}$ = 3.6V, $\overline{SHDN}$ = 0V		0.1	100	nA
T_{SD}	Thermal Shutdown Temperature			165		℃
	Thermal Shutdown Hysteresis			30		
T_{ON}	Start-Up Time	C_{OUT} = 10μF, V_{OUT} at 90% of Final Value		80		μs

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications are not applicable when the device is operated outside of its rated operating conditions.

Note 2: All voltages are defined and measured with respect to the potential at the ground pin.

Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the MSOP-8 package θ_{JA} = 223°C/W, $T_{J(MAX)}$ = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 561mW. The derating factor (-1/θ_{JA}) = -4.5mW/°C, thus below 25°C the power dissipation figure can be increased by 4.5mW per degree, and similarity decreased by this factor for temperatures above 25°C. The value of the θ_{JA} for the TDFN package is specifically dependent on the PCB trace area, trace material, and the number of layers and thermal vias.

Note 4: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} -V_{OUT} = 0.5V. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 2.5V.

Note 5: Human body model: 1.5kΩ in series with 100pF.

Note 6: Condition does not apply to input voltages below 2.5V since this is the minimum input operating voltage.

Note 7: Typical Values represent the most likely parametric norm.

Note 8: The $\overline{FAULT}$ detection voltage is specified for the input to output voltage differential at which the $\overline{FAULT}$ pin goes active low.

Functional Block Diagram

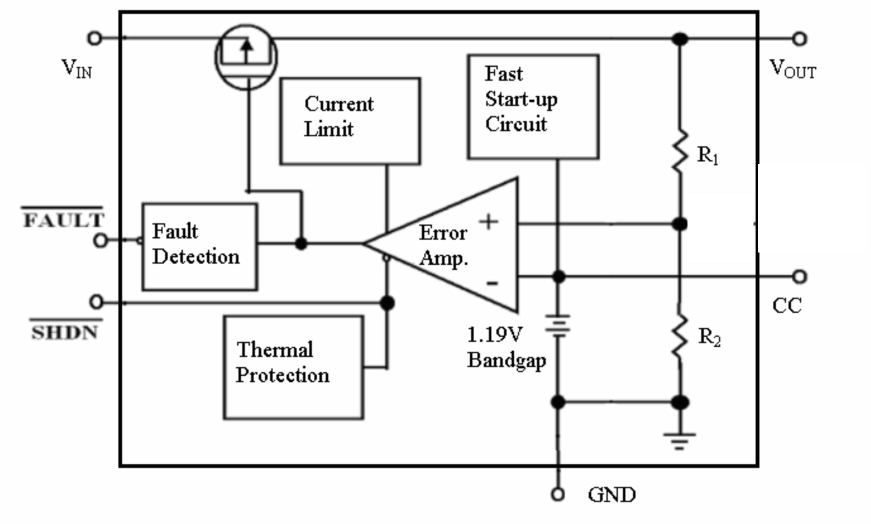
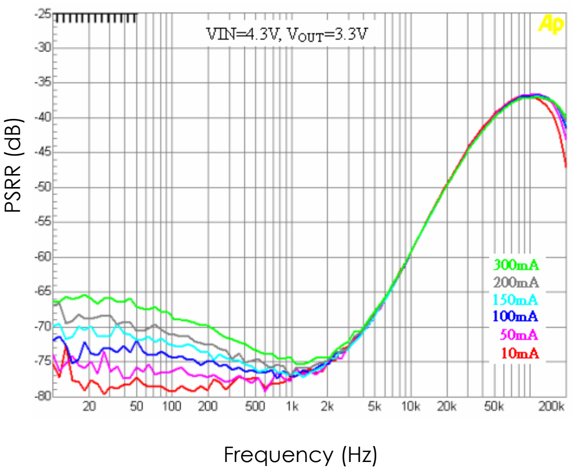


Fig.1. EMP893X Functional Block Diagram

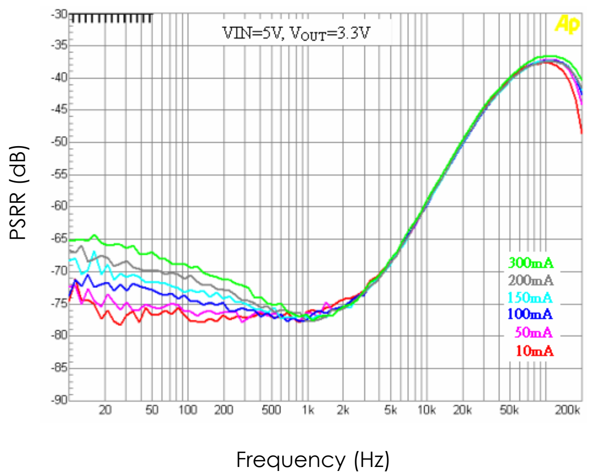
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 0.5V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 33nF, T_A = 25°C, $V_{\overline{SHDN}}$ = VIN.

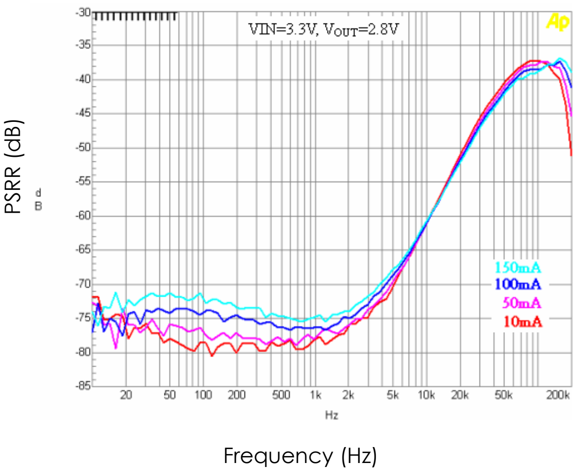
PSRR vs Frequency



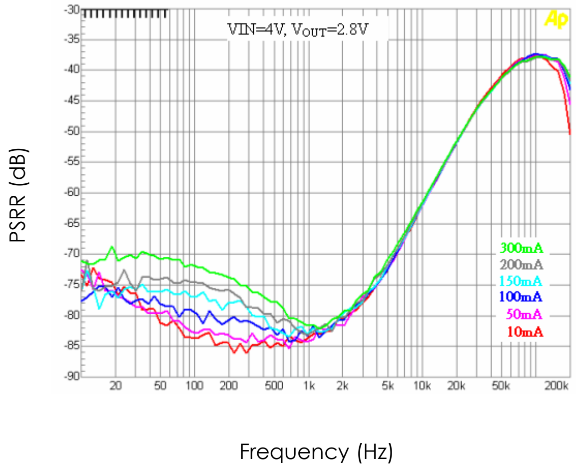
PSRR vs Frequency



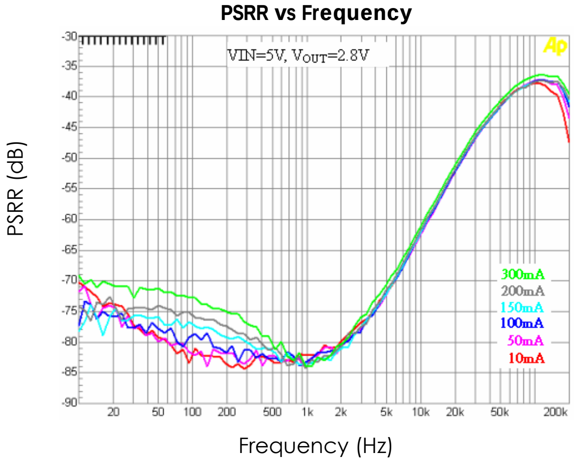
PSRR vs Frequency



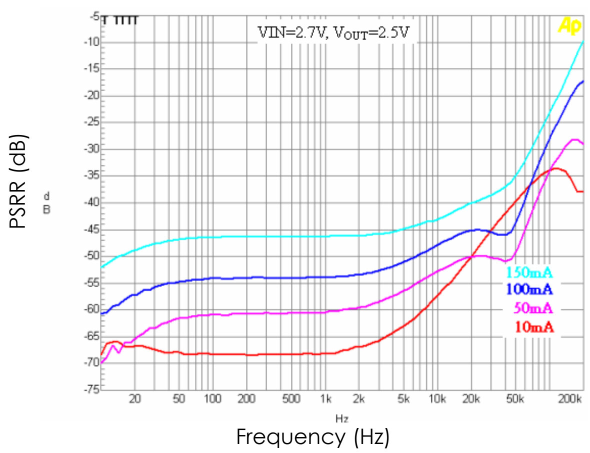
PSRR vs Frequency



PSRR vs Frequency



PSRR vs Frequency



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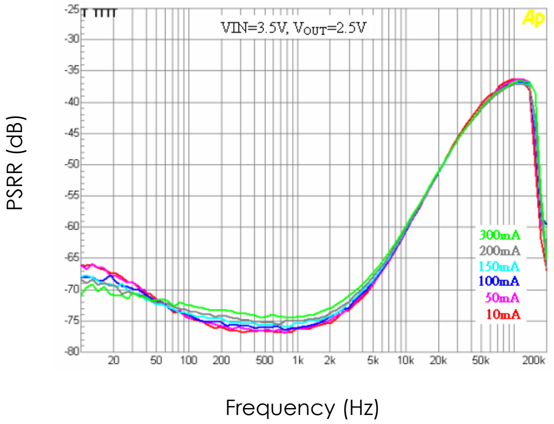
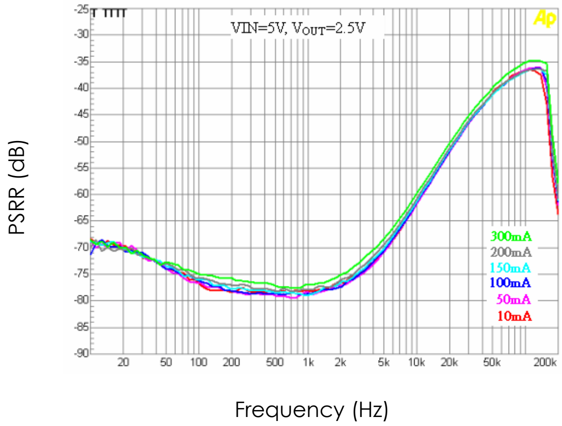
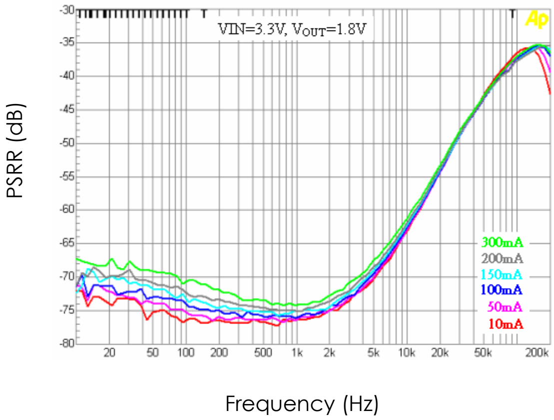
PSRR vs Frequency



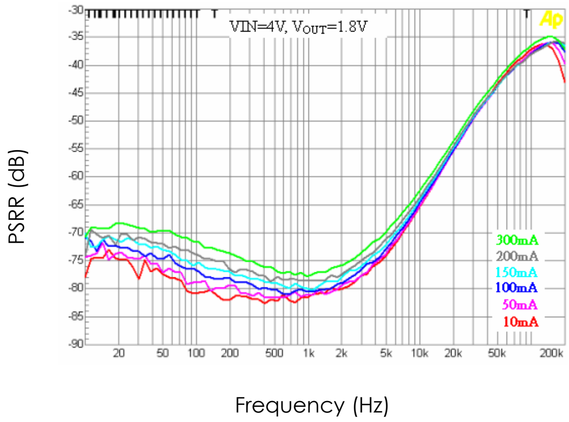
PSRR vs Frequency



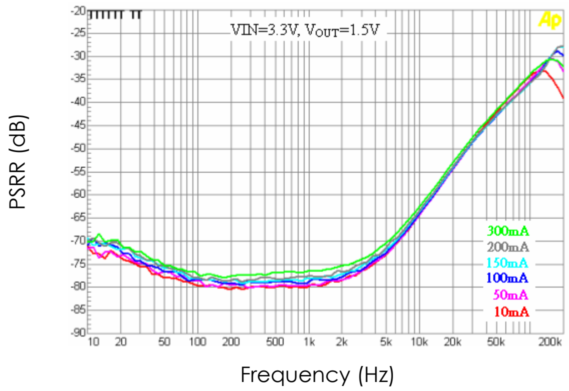
PSRR vs Frequency



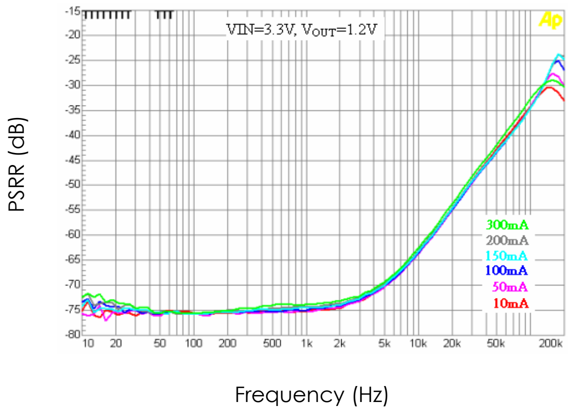
PSRR vs Frequency



PSRR vs Frequency



PSRR vs Frequency



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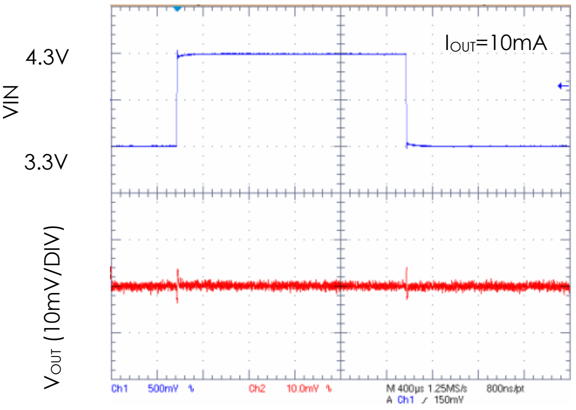
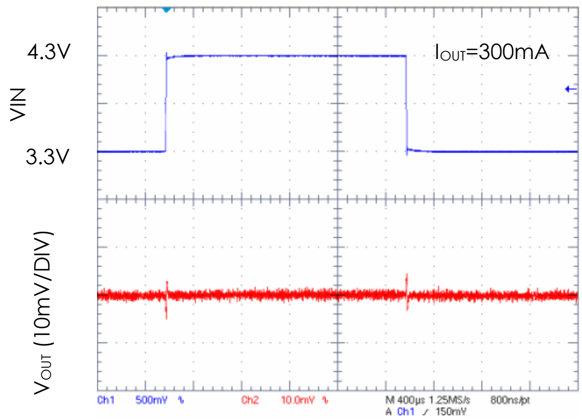
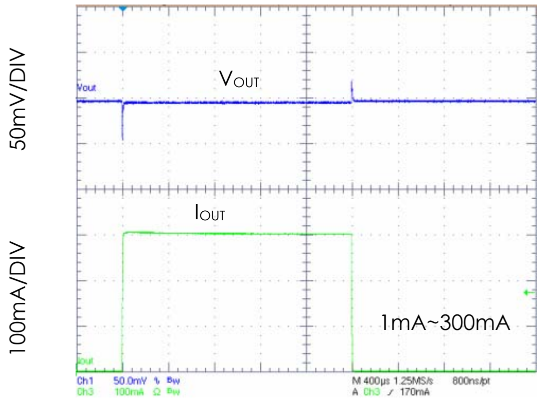
Line Transient



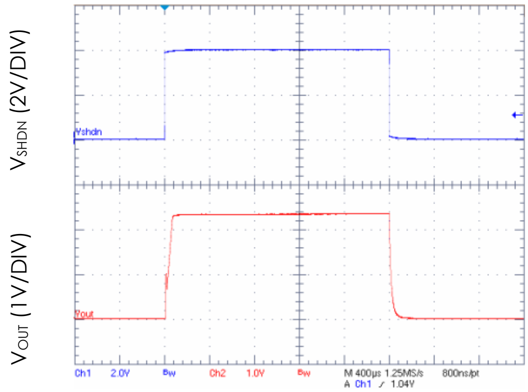
Line Transien



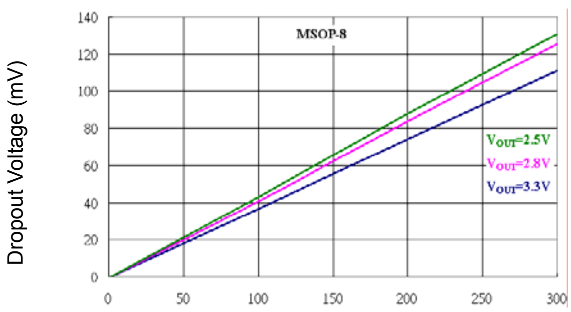
Load Transient



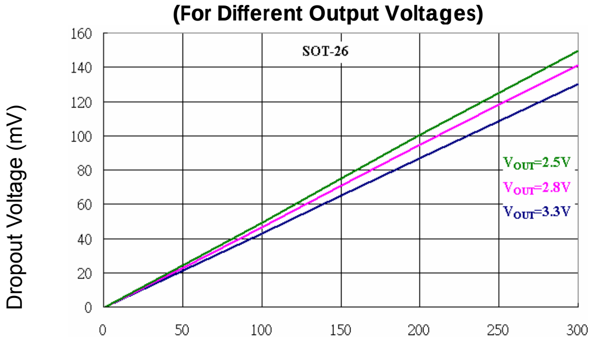
Enable and Disable



Dropout Voltage vs. Load Current (For Different Output Voltages)



Dropout Voltage vs. Load Current (For Different Output Voltages)



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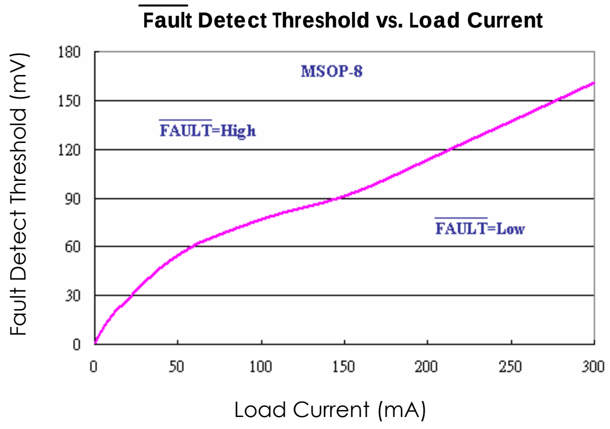
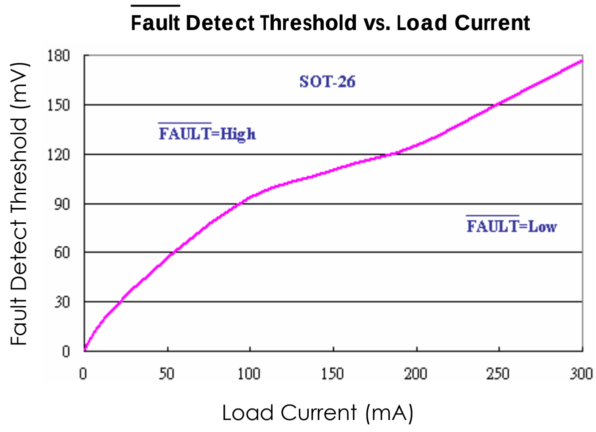
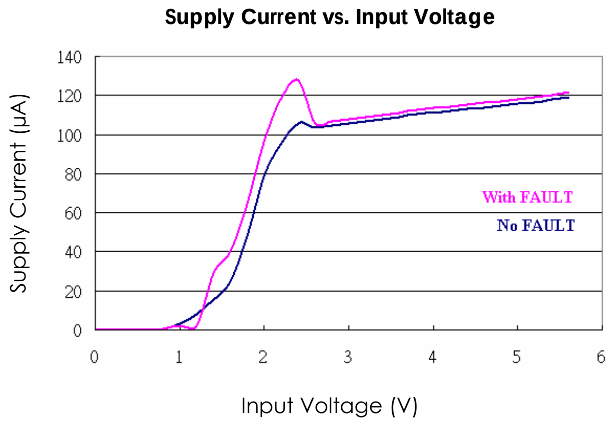
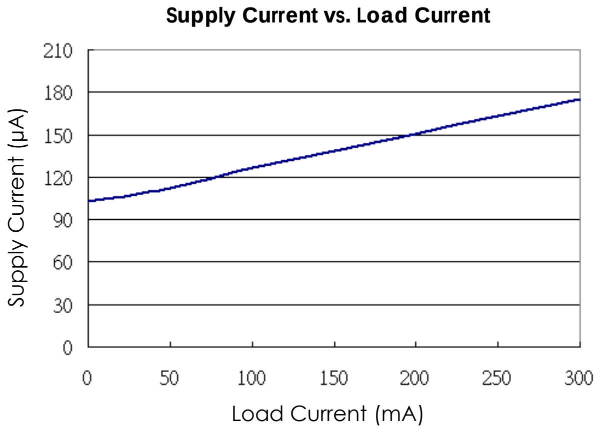
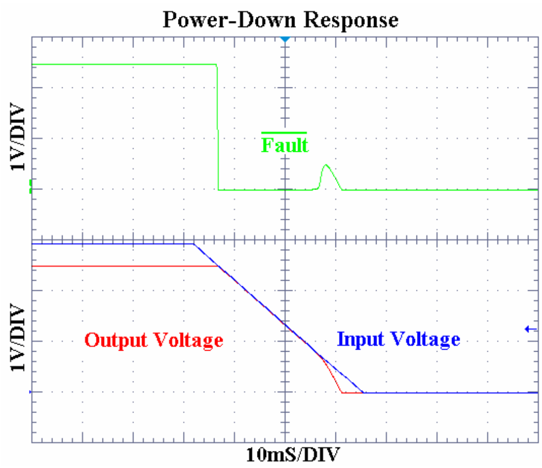
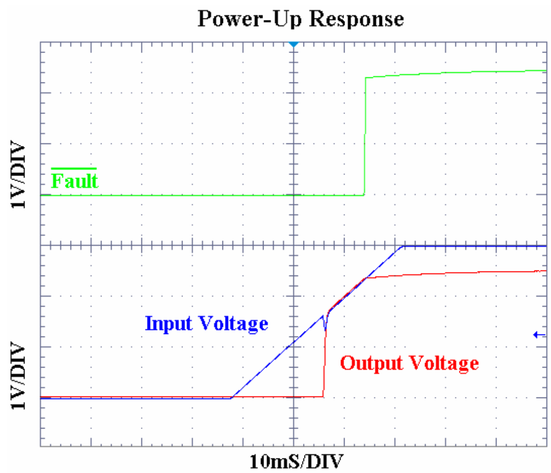












Application Information

General Description

Referring to Figure 1 of the Functional Block Diagram, the EMP893X is designed in such a way that a negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. Due to its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

To control the amount of current reaching the output, the error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. Hence, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Capacitor

To take advantage of the savings in cost and space as well as the superior filtering of high frequency noise, the EMP893X is specially designed for use with ceramic output capacitors of as low as 2.2µF. Capacitors of higher value or other types may be used, as long as its equivalent series resistance (ESR) is restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP893X are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP893X can maintain stable operation during no-load conditions, a required feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1µF is required for EMP893X. The capacitor value may be increased without limit. Caution shall be taken as the instability may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10µF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Compensation (Noise Bypass) Capacitor

To reduce the output voltage noise of the EMP893X, the bypass capacitor CC (33nF optimum) can be connected between pin 6 and the ground. Because pin 6 connects directly to the high impedance output of the bandgap reference circuit, the level of the DC leakage currents in the CC capacitors used will adversely reduce the regulator output voltage. This sets the DC leakage level as the key selection criterion of the CC capacitor types for use with the EMP893X. NPO and COG ceramic capacitors typically offer very low leakage. Although the use of the CC capacitors does

Application Information (Continued)

not affect the transient response, it does affect the turn-on time of the regulator. Tradeoff exists between output noise level and turn-on time when selecting the CC capacitor value.

Power Dissipation and Thermal Shutdown

Excessive power dissipation may cause thermal overload, and hence the increase of the IC junction temperature beyond a safe operating level. The EMP893X relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature TJ exceeding 165°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C.

When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature.

The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA} (PD) + T_A$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

$$P_D = I_{OUT} (V_{IN} - V_{OUT})$$

As the above equations indicate, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP893X, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

Fault Detection

In the event of the occurrence of various fault conditions that cause failure in the output voltage regulation, such as during thermal overload or current limit, the $\overline{\text{FAULT}}$ pin of the EMP893X becomes low. Because the $\overline{\text{FAULT}}$ pin connects to the open-drain output of a N-channel MOS transistor, a large pull-up resistor (100k Ω typical) is required to provide the necessary output voltage and yet without compromising the overall power consumption performance of the regulator. The $\overline{\text{FAULT}}$ pin also goes low when the input-to-output differential voltage becomes too small to sustain good load and line regulation at the output. This occurs typically during near dropout when the input-to-output differential voltage is less than 105mV for a load current of 200mA. The EMP893X detects near dropout conditions by comparing the differential voltage against a predefined differential threshold that is always slightly above the dropout voltage. This differential threshold is dynamical in the sense that it not only tracks the dropout voltage as the load current varies, but also scale linearly with the load current.

Shutdown

When the $\overline{\text{SHDN}}$ pin is low, the EMP893X enters the sleep mode. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the

Application Information (Continued)

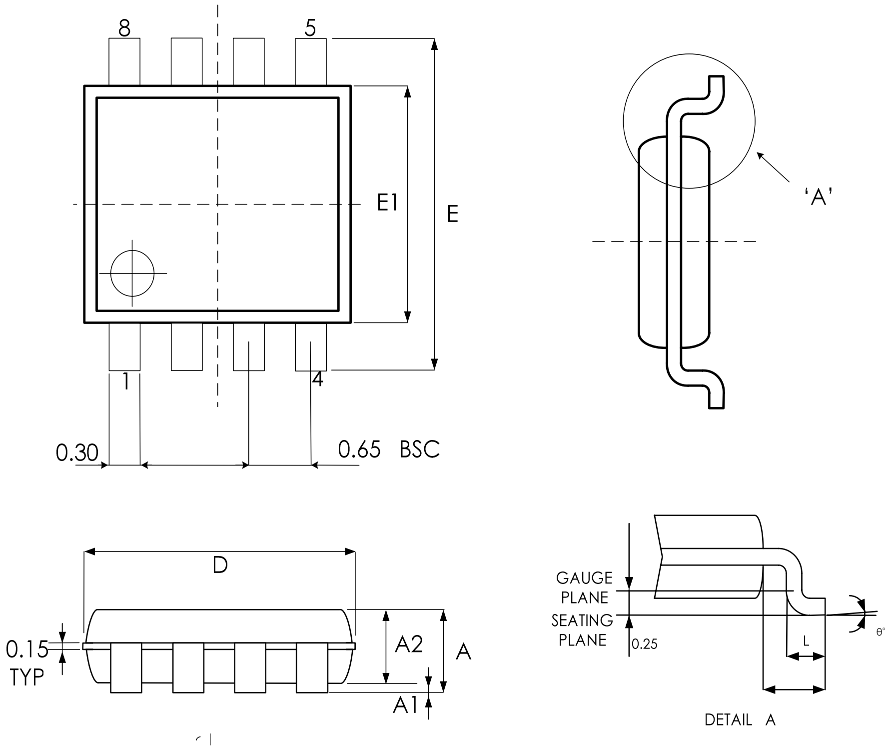
bandgap reference, are turned off, thus reducing the supply current to typically 1nA. Such a low supply current makes the EMP893X an ideal device for battery-powered applications. The maximum guaranteed voltage at the $\overline{SHDN}$ pin for the sleep mode to take effect is 0.4V. A minimum guaranteed voltage of 1.2V at the $\overline{SHDN}$ pin activates the EMP893X. Direct connection of the $\overline{SHDN}$ pin to the V_{IN} to keep the regulator on is allowed for the EMP893X. In this case, the $\overline{SHDN}$ pin must not exceed the supply voltage V_{IN}.

Fast Start-Up

Fast start-up time is one of the important factors for overall system efficiency improvement. The EMP893X has a fast start-up speed when using the optional noise bypass capacitor (CC). To shorten start-up time, the EMP893X internally supplies a 500μA current to charge up the capacitor until it reaches about 90% of its final value.

Physical Dimensions

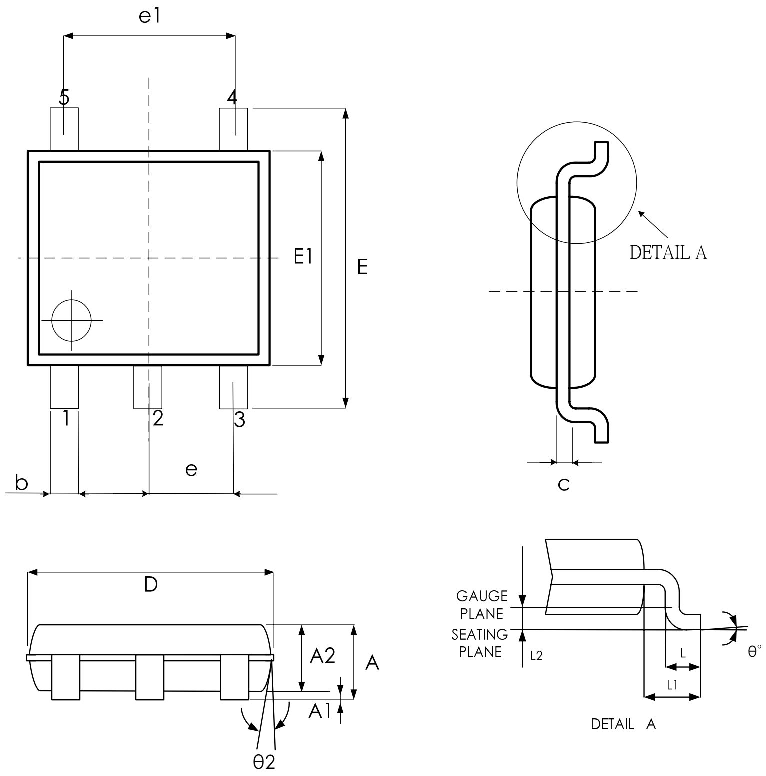
MSOP-8



SYMBPLS	MIN.	NOM.	MAX.
A	—	—	1.1
A1	0	—	0.15
A2	0.75	0.85	0.95
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
L	0.4	0.6	0.8
L1	0.95 BSC		
θ°	0	—	8

UNIT: MM

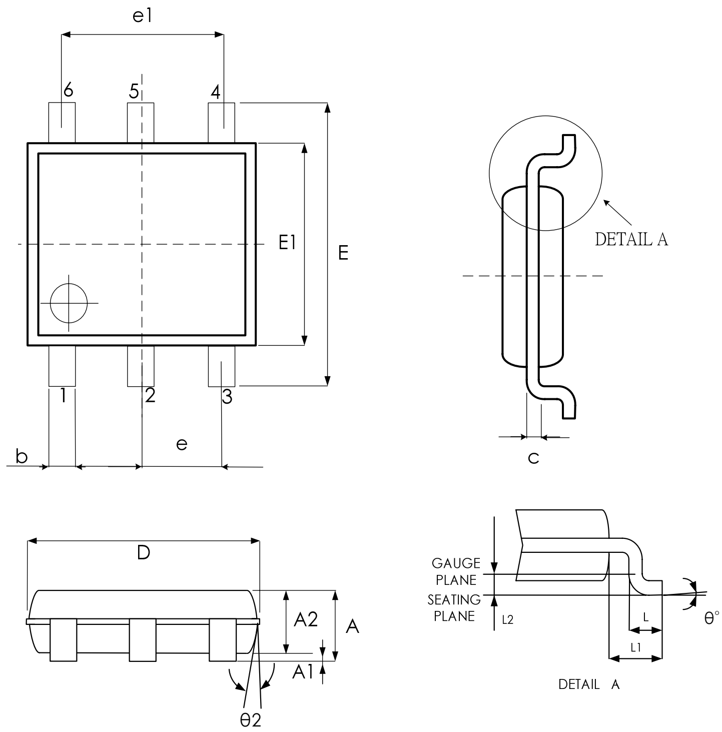
SOT-23-5



SYMBPLS	MIN.	NOM.	MAX.
A	1.05	1.20	1.35
A1	0.05	0.10	0.15
A2	1.00	1.10	1.20
b	0.30	—	0.50
c	0.08	—	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.55
L1	0.60 REF		
θ°	0	5	10
θ2°	6	8	10

UNIT: MM

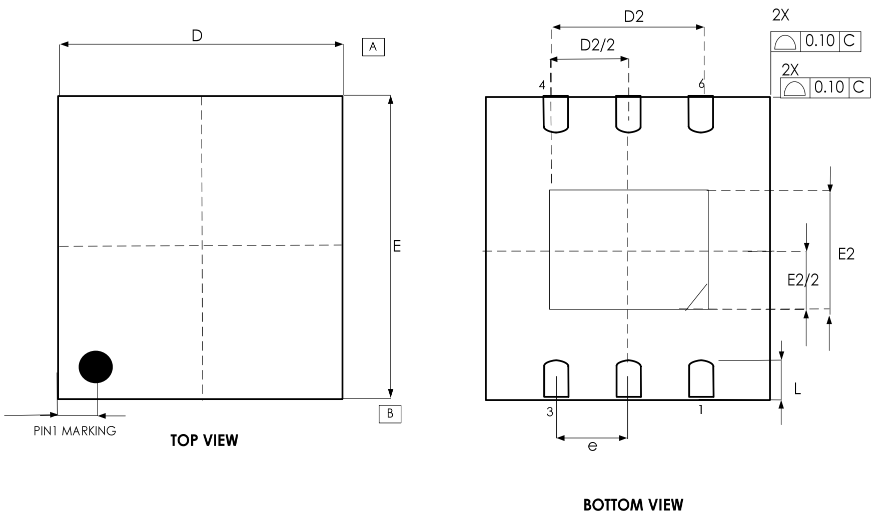
SOT-23-6

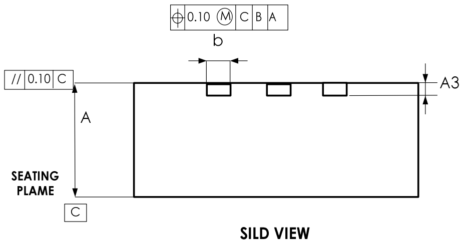


SYMBPLS	MIN.	NOM.	MAX.
A	—	—	1.45
A1	—	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC.		
E	2.80 BSC.		
E1	1.60 BSC.		
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ°	0	4	8
θ2°	5	10	15

UNIT: MM

TDFN-6





SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A3	0.200 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	2.00 BSC			0.079 BSC		
D2	1.20	1.30	1.40	0.046	0.050	0.054
E	2.00 BSC			0.079 BSC		
E2	0.50	0.60	0.70	0.022	0.024	0.026
e	0.650 BSC			0.026 BSC		
L	0.25	0.30	0.35	0.009	0.011	0.013

Notice:
Order, Mark & Packing Information

Product ID	No. of PIN	Package	Old Marking		Vout Code (XX)	Vout	Order Information
EMP8935	5	SOT-23-5	P621	P621 Date Code	12	1.2	EMP8935-12VF05GRR
			P624	P624 Date Code	15	1.5	EMP8935-15VF05GRR
			P627	P627 Date Code	18	1.8	EMP8935-18VF05GRR
			P62E	P62E Date Code	25	2.5	EMP8935-25VF05GRR
			P62G	P62G Date Code	27	2.7	EMP8935-27VF05GRR
			P62H	P62H Date Code	28	2.8	EMP8935-28VF05GRR
			P62J	P62J Date Code	30	3.0	EMP8935-30VF05GRR
			P62M	P62M Date Code	33	3.3	EMP8935-33VF05GRR

Package & Packing

SOT-23-5	3K units Tape & Reel

Revision History

Revision	Date	Description
7.0	2009.05.08	EMP transferred from version 6.3

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