1A CMOS Linear Regulator

General Description

The EMP8995 low-dropout (LDO) CMOS linear regulators feature low dropout voltage (510mV@1A), low quiescent current (120μA), and fast transient response. It guarantees delivery of 1A output current and supports preset 3.3V output voltages.

The regulator is stable with small ceramic capacitive loads (2.2μF typical). The EMP8995 is available in miniature SOT-223 packages.

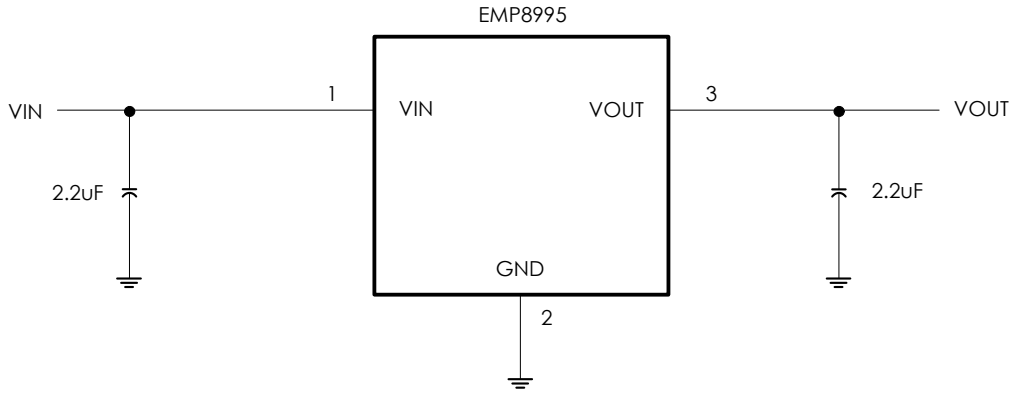
Applications

- SMPS Post Regulator
- DSP, FPGA and Microprocessor Power
- Wireless Devices
- PC Peripherals
- LCD TV / Monitors
- Portable handheld Devices

Features

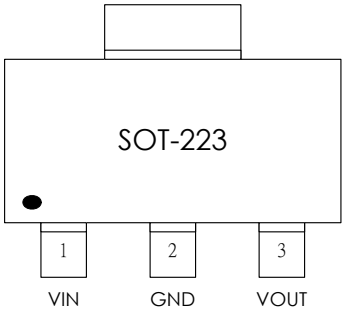
- 1A guaranteed output current
- 53dB PSRR @1kHz, Vout=3.3V, Vin=4.3V, Iload=1A
- 30μV RMS output voltage noise @10mA
- 510mV typical dropout at 1A
- 120μA typical quiescent current
- Less than 1nA (typical) @ shutdown mode
- Fast line and load transient response
- Stable with small ceramic output capacitors
- Over temperature and over current protection
- ±2% output voltage tolerance

Typical Application



Connection Diagram

SOT-223 (TOP View)



Order Information

EMP8995-XXVE03NRR

XX Output voltage

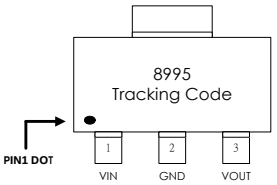
VE03 SOT-223 Package

NRR RoHS & Halogen free package

Rating: -40 to 85°C

Package in Tape & Reel

Order, Mark & Packing Information

Package	Vout	Product ID.	Marking	Packing
SOT-223	3.3V	EMP8995-XXVE03NRR		Tape & Reel 3kpcs

Pin Functions

Name	SOT-223	Function
VIN	1	**Supply Voltage Input.** Require a minimum input capacitor of close to 2.2μF to ensure stability and sufficient decoupling from the ground pin.
GND	2	**Ground Pin.**
VOUT	3	**Output Voltage Feedback.**

Absolute Maximum Ratings (Notes 1, 2)

VIN, VOUT	-0.3V to 6.0V	Lead Temperature (Soldering, 10 sec.)	260°C
Power Dissipation	(Note 3)	ESD Rating	
Storage Temperature Range	-65°C to150°C	HBM	2kV
Junction Temperature (T_J)	150°C	MM	200V

Operating Ratings (Note 1), (Note 2)

Temperature Range	-40°C to 85°C	Thermal Resistance (θ_{JA}) (Note 3)	
Supply Voltage	Vout+1V to 5.5V	SOT-223	115°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} +1V, C_{IN} = C_{OUT} = 2.2µF, Ta = 25°C.
Boldface limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		**4.0**		**5.5**	V
ΔV_{OTL}	Output Voltage Tolerance	100µA ≤ I_{OUT} ≤ 1000mA $V_{OUT\ (NOM)}$ +1V ≤ VIN ≤ 5.5V	-2		+2	% of $V_{OUT\ (NOM)}$
			-3		**+3**	
I_{OUT}	Maximum Output Current	Average DC Current Rating	1000			mA
I_{LIMIT}	Output Current Limit		1000	1300		mA
I_Q	Supply Current	I_{OUT} = 0mA		120		µA
		I_{OUT} = 1000mA		350		
V_{DO}	Dropout Voltage	I_{OUT} = 50mA		22		mV
		I_{OUT} = 300mA		130		
		I_{OUT} = 600mA		270		
		I_{OUT} = 1000mA		510		
ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V	-0.15	0.1	0.15	%/V
	Load Regulation	1mA ≤ I_{OUT} ≤ 1000mA		0.001		%/mA
e_n	Output Voltage Noise	I_{OUT} = 10mA, 10Hz ≤ f ≤ 100kHz		130		μV_{RMS}
T_{SD}	Thermal Shutdown Temperature			165		℃
	Thermal Shutdown Hysteresis			30		

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
Note 2: All voltages are with respect to the potential at the ground pin.
Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

Functional Block Diagram

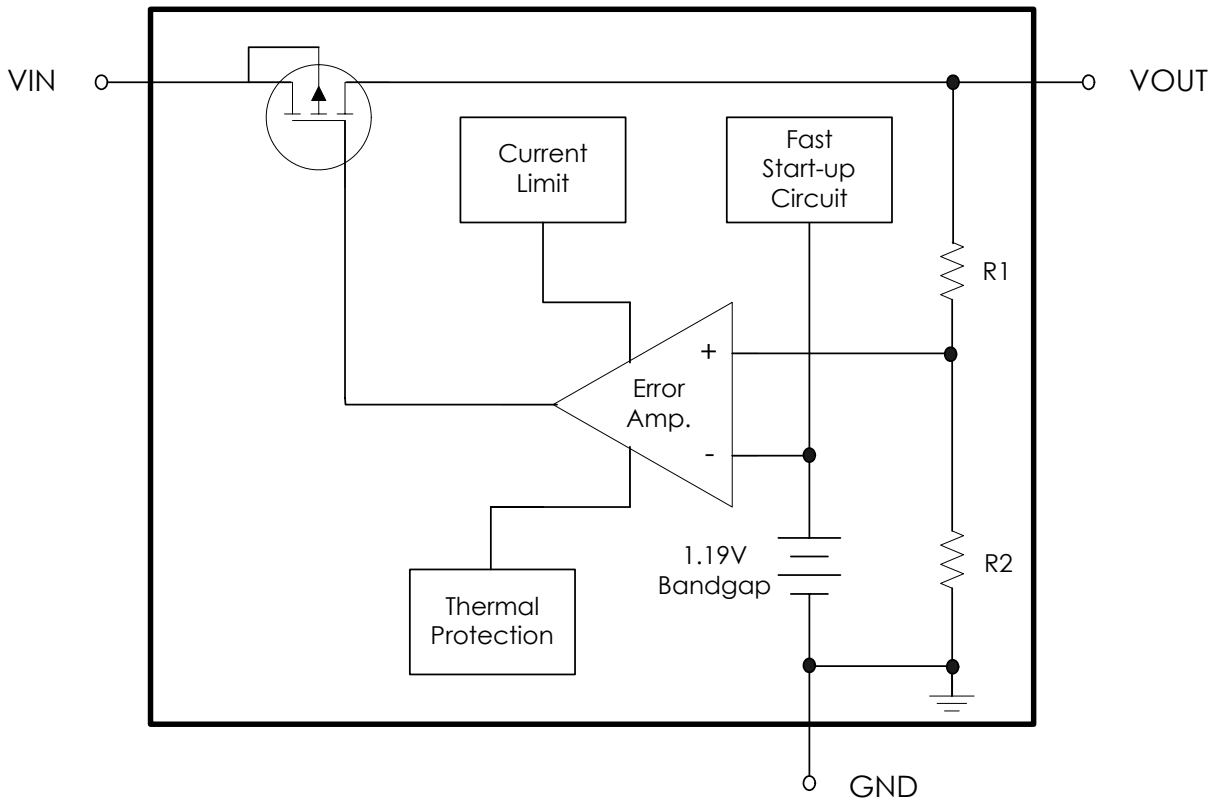
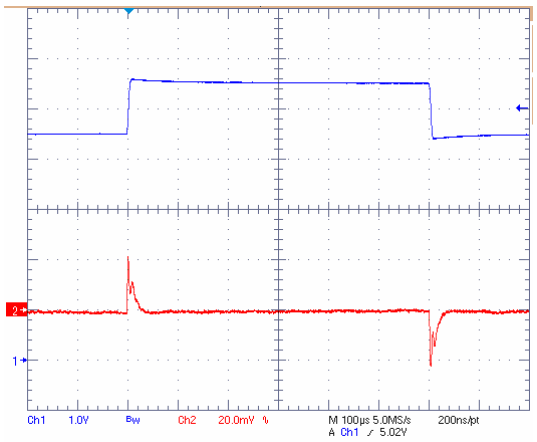


Fig.1 Functional Block Diagram of EMP8995

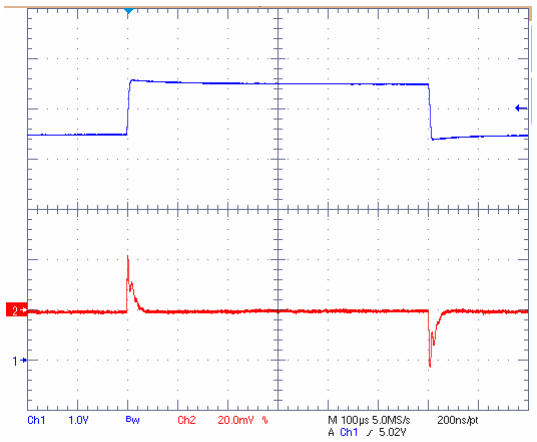
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, T_A = 25°C.

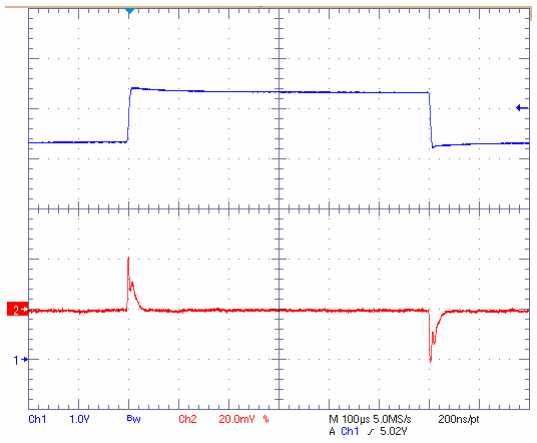
Line Transient (VOUT=3.3V, IOUT=10mA)



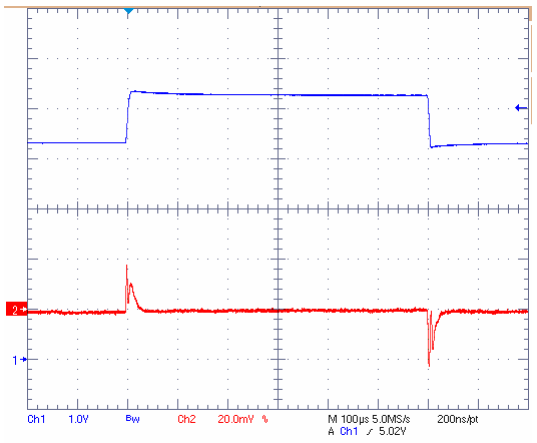
Line Transient (VOUT=3.3V, IOUT=100mA)



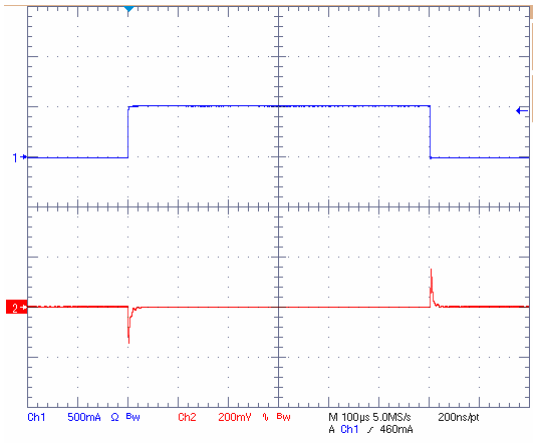
Line Transient (VOUT=3.3V, IOUT=500mA)



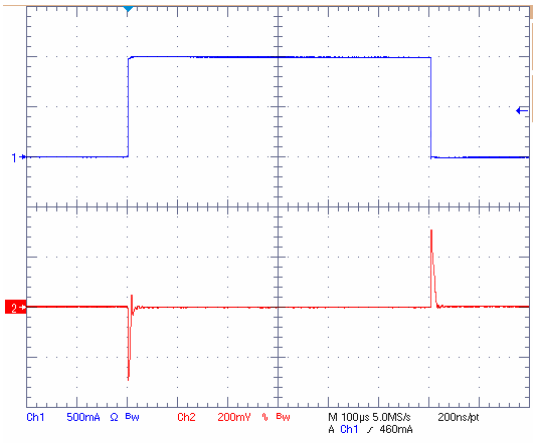
Line Transient (VOUT=3.3V, IOUT=1000mA)



Load Transient (VOUT=3.3V, IOUT=50mA to 500mA)



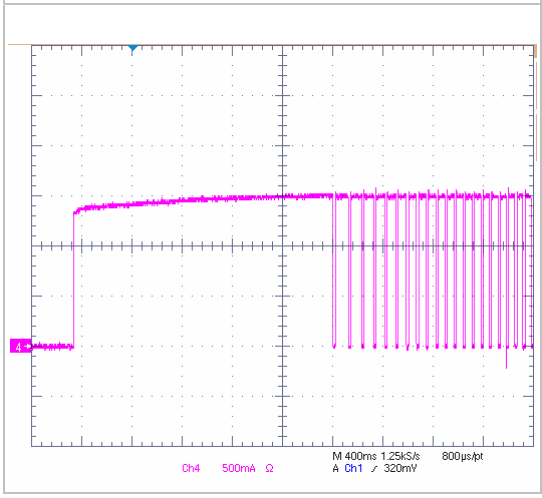
Load Transient (VOUT=3.3V, IOUT=50mA to 1000mA)



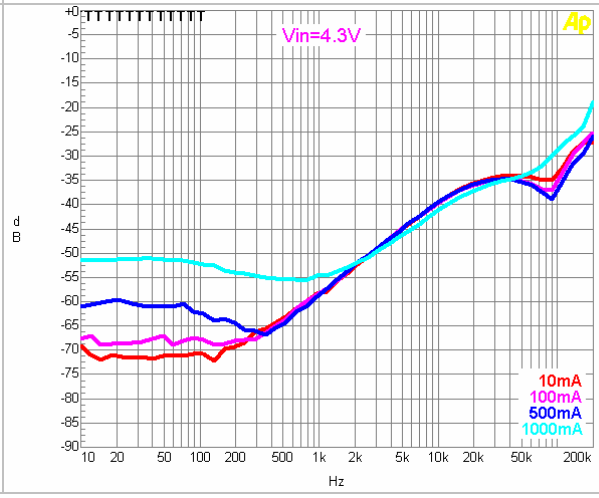
Typical Performance Characteristics (cont.)

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, T_A = 25°C.

Current Limit (VOUT=3.3V)



PSRR vs. Frequency



Application Information

General Description

Referring to Fig.1as shown in the Functional Block Diagram section, the EMP8995 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Capacitor

The EMP8995 is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8995 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8995 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 2.2μF is required for EMP8995. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The EMP8995 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature TJ exceeding 165°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and TJ is as follows:

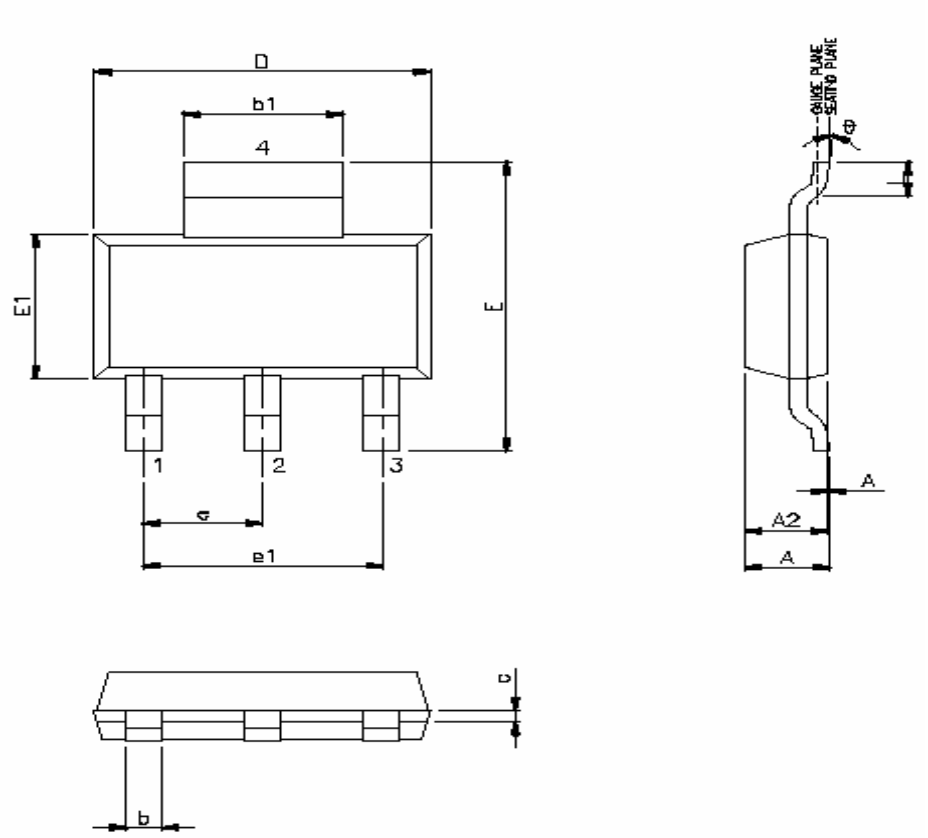
$T_J = \theta_{JA}$ (PD) + T_A

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

$P_D = I_{OUT} (V_{IN} - V_{OUT})$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8995, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

Package Outline drawing
SOT-223



SYMBPLS	MIN.	NOM.	MAX.
A	—	—	1.80
A1	0.02		0.10
A2	1.50	1.60	1.70
b	0.66	0.70	0.84
b1	2.90	3.00	3.10
c	0.23	0.30	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
e1	4.60 BSC		
L	0.75	—	—
θ°	0	—	10

UNIT: MM

Revision History

Revision	Date	Description
0.1	2009.12.23	Original

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