4 Channel Power Management IC For Portable Devices

GENERAL DESCRIPTION

The EMQ9904 is a high efficiency, 4-channel power management IC for battery-powered, portable devices application. It integrates a high efficiency step-up DC/DC converter, a linear regulator and two high efficiency step-down DC/DC converters.

The step-up DC/DC converter (CH1) can start up 0.9V typically with operating voltage down to 0.6V and up to 500mA loading capability. It features with extreme low 26µA quiescent current with no load, which is the best fit for extending battery life during the standby mode.

The linear regulator (CH2) features ultra-high power supply rejection ratio (75dB at 1kHz), low output voltage noise (30µV), low dropout voltage (270mV), low quiescent current (110µA) and fast transient response. It operates from 2.5V to 5.5V input voltage, up to 600mA loading capability and regulates adjustable output voltage from 1.2V to 5.0V.

The two Synchronous Buck converters (CH3, CH4) operate from 2.5V to 5.5V input voltage, up to 600mA loading capability and regulate adjustable output voltage from 0.6V to 5.5V. It features low quiescent current, 1.5MHz internal frequency operation.

The EMQ9904 is available in TQFN24 4x4 package,
It is **Green compliant** (RoHS and Halogen-free).

FEATURES

- **Battery powered Synchronous boost Converter**
  - 1.8V to 5.5V Output Voltage
  - Up to 93% Efficiency
  - Output Current up to 500mA
  - Typical Iq 26µA with No Load
  - 1.1V to 5.5V operating Voltage
  - 0.9V start-up input voltage
- **Linear Regulator**
  - 1.2V to 5.0V Output Voltage
  - 75dB Typical PSRR at 1kHz
  - 30µV RMS Output Voltage Noise (10Hz to 100kHz)
  - 270mV Typical Dropout at 600mA
- **Two Synchronous Buck Converters**
  - 0.6V to 5.5V Output Voltage
  - Up to 95% Efficiency
  - Low Dropout Operation: 100% Duty Cycle

- No Schottky Diode Needed for Above Converters
- Shutdown Current < 1µA(CH1-CH4)
- Independent Enable PIN (CH1-CH4)
- Independent Input Voltage PIN(CH1-CH4)
- No External Compensation Network is needed
- Excellent Line and Load Transient Response (CH1-CH4)
- Over Current Protection(CH1-CH4)
- Over Temperature Protection(CH2, CH3, CH4)

APPLICATIONS

- Hand-held Instruments
- Battery-powered systems
- Portable information applications
- Wireless Networking
- Digital Still Cameras

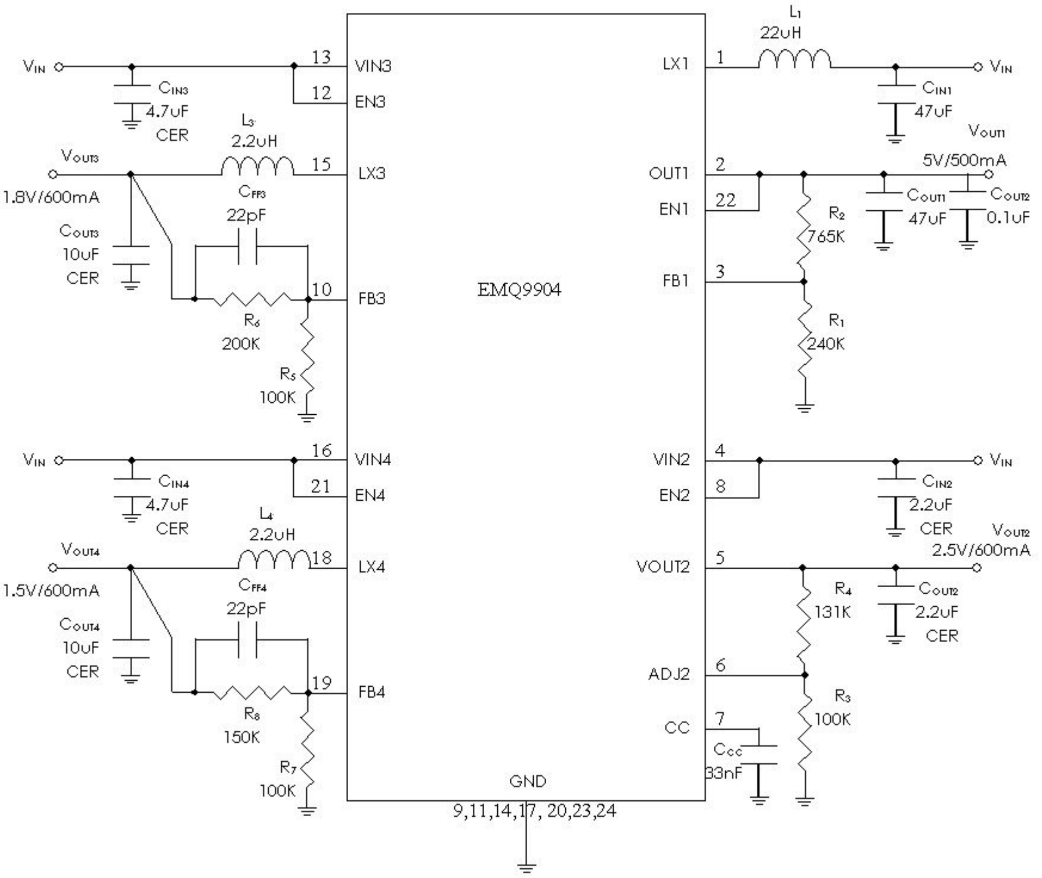
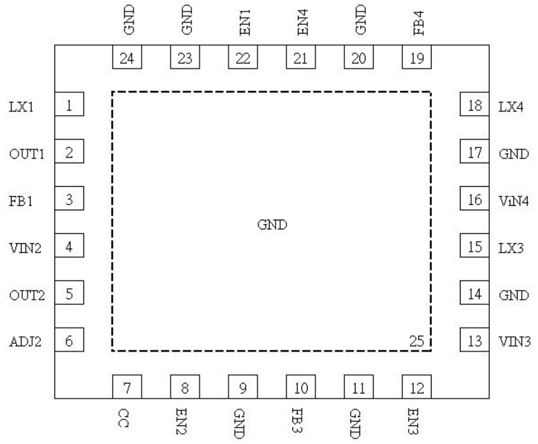


Figure 1. Typical Application

CONNECTION DIAGRAM

TQFN24 4x4

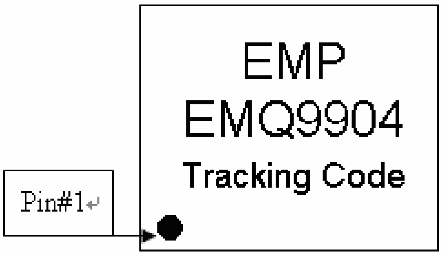


ORDER INFORMATION

EMQ9904-00HC24NRR

00	Adjustable output voltage
HC24	TQFN-24 Package
NRR	RoHS & Halogen free
	Rating: -40 to 85°C
	Package in Tape & Reel

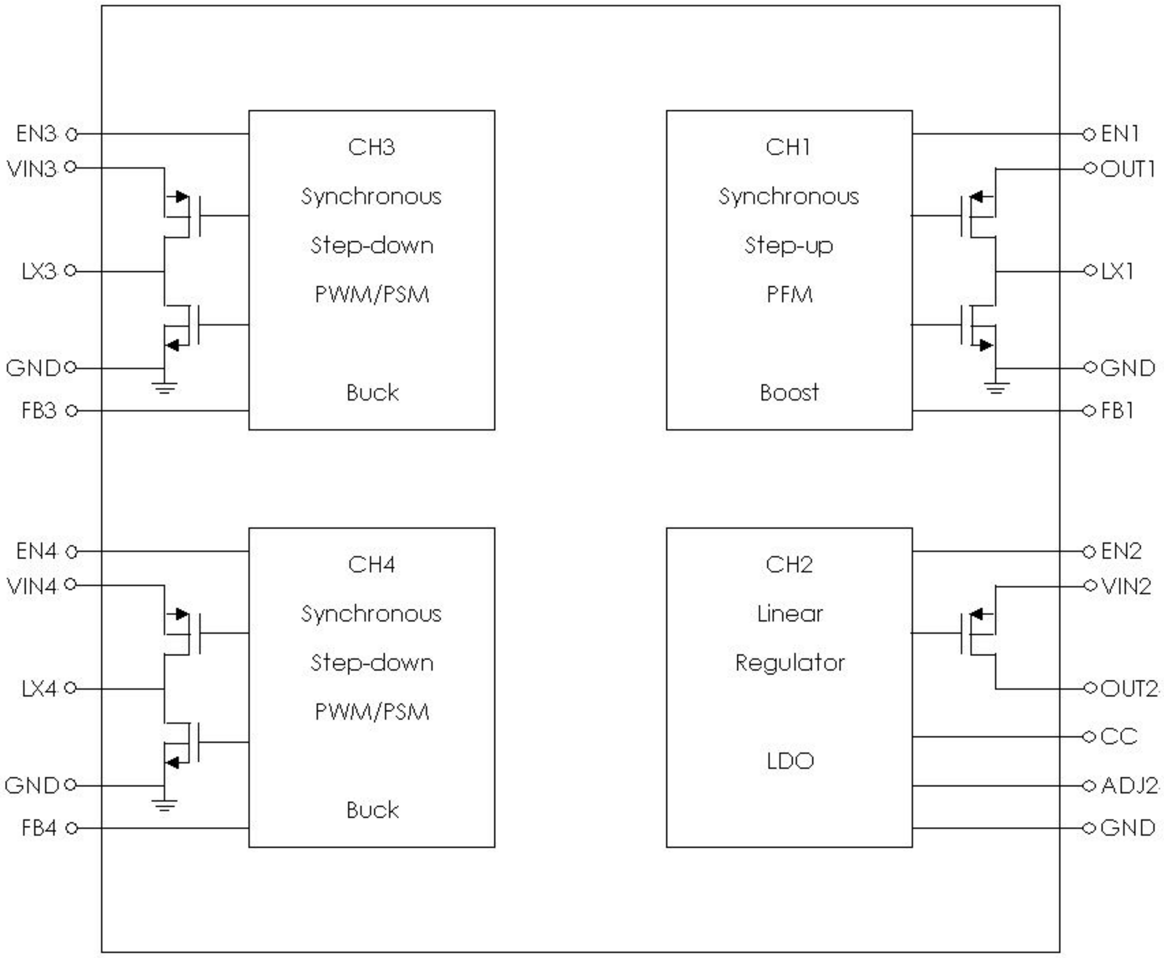
Order, Mark & Packing Information

Package	Product ID	Marking	Packing
TQFN24	EMQ9904-00HC24NRR		3K units Tape & Reel

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
LX1	1	I	CH1 Switch PIN. Must be connected to Inductor.
OUT1	2	B	CH1 Output Voltage PIN. This PIN also provides bootstrap power to IC.
FB1	3	I	CH1 Voltage Feedback PIN. Connecting to OUT1 to get +3.3V output on OUT1, Connecting to GND to get +5.0V output on OUT1, Using resistor network to set OUT1 from +1.8V to +5.5V.
EN1	22	I	CH1 Enable Input.
GND	9,11,14,17,20,23,24	-	Ground.
VIN2	4	I	CH2 Input Voltage.
OUT2	5	O	CH2 Output Voltage Feedback.
ADJ2	6	I	CH2 Adjustable Negative Feedback Control.
CC	7	I	CH2 Compensation Capacitor.
EN2	8	I	CH2 Enable Input.
FB3	10	I	CH3 Voltage Feedback PIN.
EN3	12	I	CH3 Enable Input.
VIN3	13	I	CH3 Input Voltage.
LX3	15	O	CH3 Switch PIN. Must be connected to Inductor.
VIN4	16	I	CH4 Input Voltage.
LX4	18	O	CH4 Switch PIN. Must be connected to Inductor.
FB4	19	I	CH4 Voltage Feedback PIN.
EN4	21	I	CH4 Enable Input.

FUNCTION BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (VIN2, VIN3, VIN4)	-0.3V to 6.0V
LX1 Switch PIN Voltage	-0.3V to 6.0V
OUT2 Voltage	-0.3V to 6.0V
LX3 Switch PIN Voltage	-0.3V to (VIN3+0.3V)
LX4 Switch PIN Voltage	-0.3V to (VIN3+0.3V)
Other I/O PIN Voltage	-0.3V to (VIN3+0.3V)
Storage Temperature	-65°C to +150°C
Power Dissipation	1.85W

ESD Susceptibility	**TBD**
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (TQFN24 4x4)	45°C/W
Operating Ratings	
Temperature Range	-40°C ≦ T_A ≦ 85°C
Supply Voltage (VIN2, VIN3, VIN4)	2.5V ≦ V_{DD} ≦ 5.5V

ELECTRICAL CHARACTERISTICS

Apply for V_{IN1}=2.0V, V_{OUT1}=3.3V, FB1=V_{OUT}, V_{IN2} = V_{OUT2} +1V (Note 6), V_{EN2} = V_{IN2}, C_{IN2} = C_{OUT2} = 2.2µF, C_{CC2} = 33nF, V_{IN3} = 3.6V, V_{IN4} = 3.6V and T_A = 25°C (unless otherwise noted), Boldface limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	EMQ9904			Units
			Min	Typ	Max	
CH1 (Note 4)						
V_{IN1_MIN}	Minimum input voltage			0.7		V
V_{IN1}	Operating Voltage		1.1		5.5	V
V_{START_UP}	Start-up Voltage (Note 5)	R_L=3K		0.9	1.00	V
T_{VSTART_UP}	Start-up Voltage Temp-co.			-2		mV/°C
V_{OUT1}	Output Voltage	V_{IN}<V_{OUT}	1.8		5.5	V
		FB=V_{OUT}	3.17	3.3	3.43	
		FB=GND	4.80	5.0	5.20	
I_{OUT1}	Steady State Output Current (Note 6)	FB=V_{OUT}	200	245		mA
		FB=GND	120	190		
V_{REF1}	Reference Voltage	I_{REF}=0	1.16	1.195	1.225	V
T_{VREF1}	Reference Voltage Temp-co.	Temp=-40℃ to 85℃		0.015		mV/°C
ΔV_{REF1}	Reference Load Regulation	I_{REF}=0 to 100µA		1	30	mV
	Reference Line Regulation	V_{OUT1}=1.8V to 5.5V		0.3	5	mV/V
V_{FB1}	FB1 Input Threshold		1.16	1.195	1.225	V
R_{FET1}	Internal switch On-Resistance	I_{LX1}=100mA		0.4		Ω
I_{LX_LIM1}	LX1 switch Current Limit			1		A
I_{LX_LEAK1}	LX1 Leakage Current	VLX=0V~4V;Vout=5.5V		0.05	1	µA
I_{Q1}	Operating Current into OUT1 (Note 7)	VFB=1.4V,Vout=3.3V		26	40	µA
I_{SD_OUT1}	Shutdown Current into OUT1	EN1=GND		0.1	1	µA
Effi1	Efficiency	Vout=3.3V, Iload=200mA		90		%

		Vout=2V, Iload=1mA		85		
T_{ON_LX1}	LX1 Switch On-Time	VFB=1V,Vout=3.3V	2	4	7	μs
T_{OFF_LX1}	LX1 Switch Off-Time	VFB=1V,Vout=3.3V	0.6	0.9	1.4	μs
I_{FB}	FB1 Input Current	VFB=1.4V		0.03	50	nA
I_{EN}	EN1 Input Current	EN1=GND or VOUT1		0.07	50	nA
V_{EN}	EN1 Input Voltage	VIL			0.2V_{OUT1}	V
		VIH	0.8V_{OUT1}			
CH2						
V_{IN2}	Input Voltage		**2.5**		**5.5**	V
ΔV_{OTL2}	Output Voltage Tolerance	100μA ≤ I_{OUT2} ≤ 300mA $V_{OUT2\ (NOM)}$ +0.5V ≤ VIN2 ≤ 5.5V (Note 8) ADJ2=V_{OUT2}	-2		+2	% of $V_{OUT\ (NOM)}$
			-3		**+3**	
V_{OUT2}	Output Adjust Range		**1.20**		**5.0**	V
I_{OUT2}	Maximum Output Current	Average DC Current Rating	**600**			mA
I_{LIMIT2}	Output Current Limit		**600**	950		mA
I_{Q2}	Supply Current	I_{OUT2} = 0mA		110		μA
		I_{OUT2} = 600mA		255		
	Shutdown Supply Current	V_{OUT2} = 0V, EN2 = GND		0.001	1	
V_{DO2}	Dropout Voltage (Note 8)	I_{OUT2} = 50mA		19		mV
		I_{OUT2} = 300mA		110		
		I_{OUT2} = 600mA		230		
ΔV_{OU2T}	Line Regulation	I_{OUT2} = 1mA, (V_{OUT2} + 0.5V) ≤ V_{IN2} ≤ 5.5V (Note 9)	-0.1	0.02	0.1	%/V
	Load Regulation	100μA ≤ I_{OUT2} ≤ 600mA		0.001		%/mA
e_{n2}	Output Voltage Noise	I_{OUT2} = 10mA, 10Hz ≤ f ≤ 100kHz		30		μV_{RMS}
VEN2	EN2 Input Threshold	V_{IH}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 8)	**1.2**			V
		V_{IL}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 8)			**0.4**	
I_{EN2}	EN2 Input Bias Current	EN2 = GND or VIN		0.1	100	nA
I_{ADJ2}	ADJ2 Input Leakage	ADJ2=1.3V (Note 10)		0.1	3	nA
T_{SD}	Thermal Shutdown Temperature	(Note 11)		165		℃

T_{SD_HYST}	Thermal Shutdown Hysteresis			30		℃
T_{ON2}	Start-Up Time	C_{OUT2} = 10µF, V_{OUT2} at 90% of Final Value		80		µs
CH3 (Note 11)						
I_{VFB3}	Feedback Current				±30	nA
V_{FB3}	Regulated Feedback Voltage	T_A = 25°C	0.588	0.600	0.612	V
		–40°C ≤ T_A ≤ 85°C	**0.585**	**0.600**	**0.615**	
ΔV_{FB3}	Reference Voltage Line Regulation	V_{IN3} = 2.5V to 5.5V			**0.4**	%/V
ΔV_{OVL3}	Output Over-voltage Lockout	$\Delta V_{OVL3} = V_{OVL3} - V_{FB3}$	20	50	80	mV
ΔV_{OUT3}	Output Voltage Line Regulation	V_{IN3} = 2.5V to 5.5V			**0.4**	%/V
	Output Voltage Load Regulation			0.5		%
I_{PK3}	Peak Inductor Current	V_{IN3} = 3V, V_{FB3} = 0.5V or V_{OUT3} = 90%, Duty Cycle < 35%		1.0		A
I_{Q3}	Quiescent Current (Note 12)	V_{FB3} = 0.5V or V_{OUT3} = 90%		200	340	µA
	Shutdown	V_{EN3} = 0V, V_{IN3} = 4.2V		0.1	1	µA
f_{OSC3}	Oscillator Frequency	V_{FB3} = 0.6V or V_{OUT3} = 100%	**1.2**	**1.5**	**1.8**	MHz
		V_{FB3} = 0V or V_{OUT3} = 0V		**290**		kHz
R_{PFET3}	$R_{DS(ON)}$ of PMOS	I_{LX3} = 100mA		0.45	0.55	Ω
R_{NFET3}	$R_{DS(ON)}$ of NMOS	I_{LX3} = –100mA		0.40	0.5	Ω
I_{LX3}	LX3 Leakage	V_{EN3} = 0V, V_{LX3} = 0V or 5V, V_{IN3} = 5V			±1	µA
V_{EN3}	EN3 Threshold		0.5		1.3	V
I_{EN3}	EN3 Leakage Current				**±1**	µA
CH4 (Note11)						
I_{VFB4}	Feedback Current				±30	nA
V_{FB4}	Regulated Feedback Voltage	T_A = 25°C	0.588	0.600	0.612	V
		–40°C ≤ T_A ≤ 85°C	**0.585**	**0.600**	**0.615**	
ΔV_{FB4}	Reference Voltage Line Regulation	V_{IN4} = 2.5V to 5.5V			**0.4**	%/V
ΔV_{OVL4}	Output Over-voltage Lockout	$\Delta V_{OVL4} = V_{OVL4} - V_{FB4}$	20	50	80	mV
ΔV_{OUT4}	Output Voltage Line Regulation	V_{IN4} = 2.5V to 5.5V			**0.4**	%/V
	Output Voltage Load Regulation			0.5		%

I_{PK4}	Peak Inductor Current	V_{IN4} = 3V, V_{FB4} = 0.5V or V_{OUT4} = 90%, Duty Cycle < 35%		1.0		A
I_{Q4}	Quiescent Current (Note 12)	V_{FB4} = 0.5V or V_{OUT4} = 90%		200	340	μA
	Shutdown	V_{EN4} = 0V, V_{IN4} = 4.2V		0.1	1	μA
f_{OSC4}	Oscillator Frequency	V_{FB4} = 0.6V or V_{OUT4} = 100%	**1.2**	**1.5**	**1.8**	MHz
		V_{FB4} = 0V or V_{OUT4} = 0V		**290**		kHz
R_{PFET4}	$R_{DS(ON)}$ of PMOS	I_{LX4} = 100mA		0.45	0.55	Ω
R_{NFET4}	$R_{DS(ON)}$ of NMOS	I_{LX4} = –100mA		0.40	0.5	Ω
I_{LX4}	LX4 Leakage	V_{EN4} = 0V, V_{LX4} = 0V or 5V, V_{IN4} = 5V			±1	μA
V_{EN4}	EN4 Threshold		0.5		1.3	V
I_{EN4}	EN4 Leakage Current				**±1**	μA

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

Note 4: CH1 Specifications are tested at T_A=25°C. Specifications over all operation temperature range are guarantee by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 5: CH1 Start-up voltage operation is guaranteed without external Schottky diode

Note 6: CH1 Steady-state output current indicates that the device maintains regulation under load.

Note 7: CH1 Device is bootstrapped (power to the IC comes from OUT). This correlates directly with the actual battery supply.

Note 8: CH2 Condition does not apply to input voltages below 2.5V since this is the minimum input operating voltage.

Note 9: CH2 Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} -V_{OUT} = 0.5V. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 2.5V.

Note 10: CH2 The ADJ2 pin is disconnected internally for the preset versions.

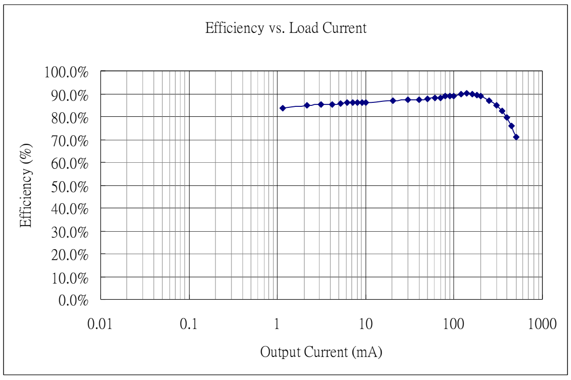
Note 11: CH2, CH3 and CH4 build-in internal over-temperature protection to prevent over-load condition.

Note 12: Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.

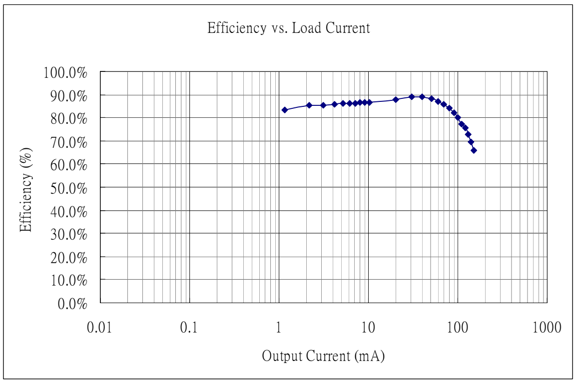
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1}=2.4V, V_{OUT1}=3.3V, C_{IN1}=47μF, L_1=22μH, C_{OUT1}=47μF, V_{EN1} = 3.3V, V_{IN2} = $V_{OUT2\ (NOM)}$ + 1V, C_{IN2} = C_{OUT2} = 2.2μF, C_{CC} = 33nF, V_{EN2} = V_{IN2}, V_{EN3} = V_{IN3}, C_{IN3}=4.7μF, L_3=2.2μH, C_{OUT3}=4.7μF, C_{IN4}=4.7μF, L_4=2.2μH, C_{OUT4}=4.7μF, V_{EN4} = V_{IN4} T_A = 25°C, unless otherwise specified

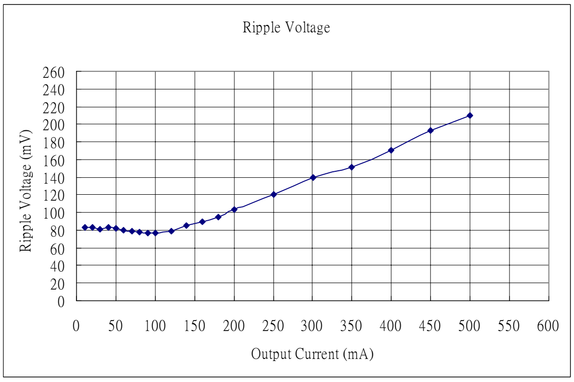
CH1 **Efficiency vs Output Current**



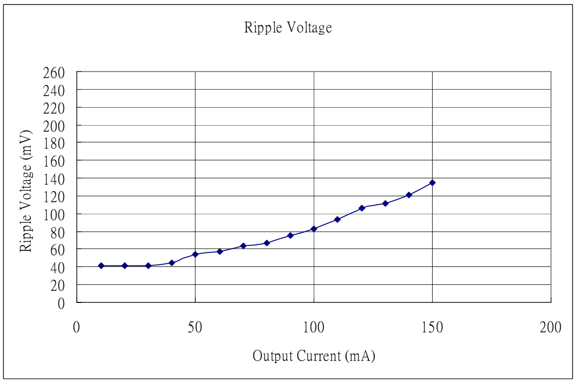
CH1 **Efficiency vs Output Current @V_{IN}=1.2V**



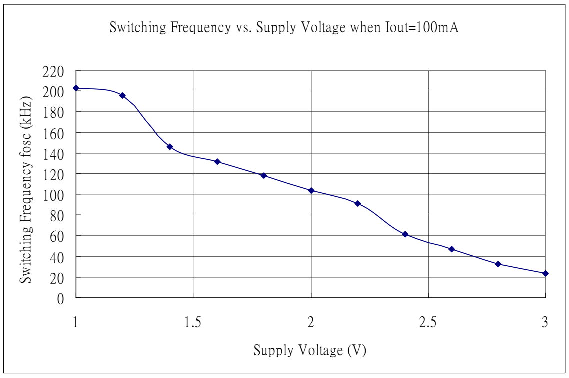
CH1 Ripple Voltage vs Output Current



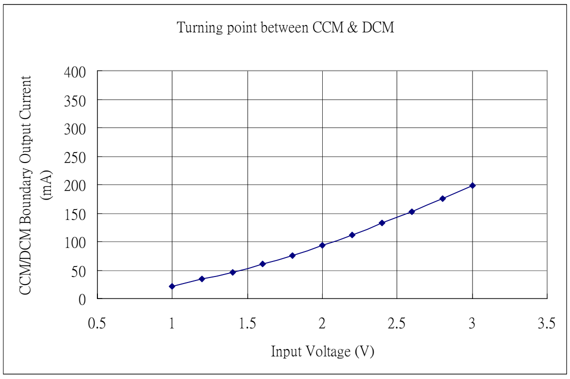
CH1 Ripple Voltage vs Output Current when Vin=1.2V



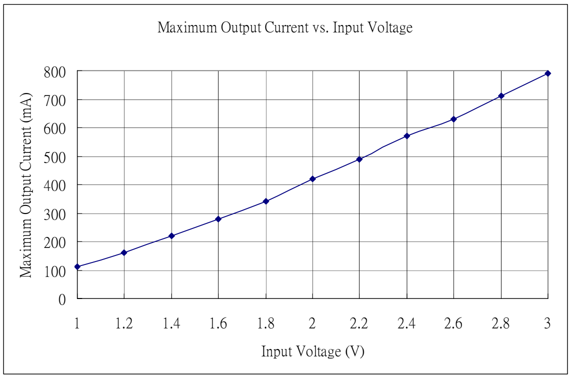
CH1 Switching Frequency vs input voltage



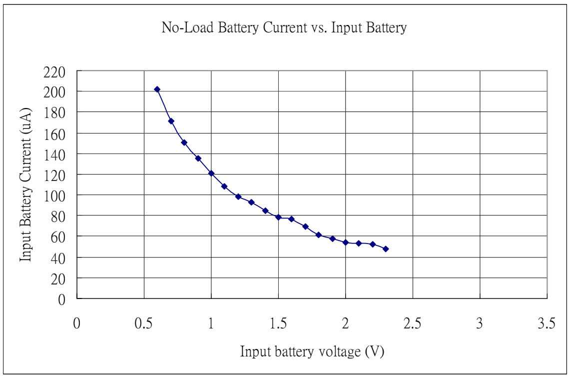
CH1 Turning point between CCM and DCM



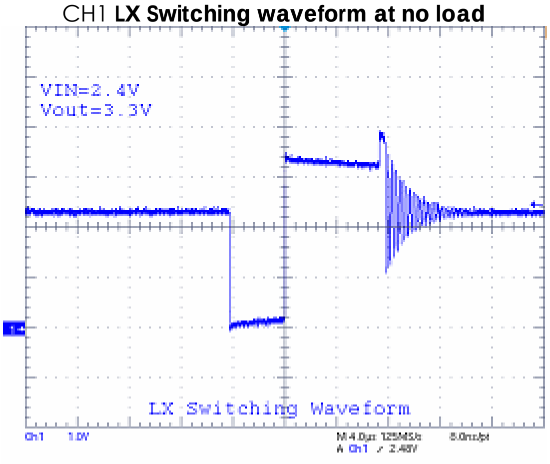
CH1 Maximum output current vs input voltage



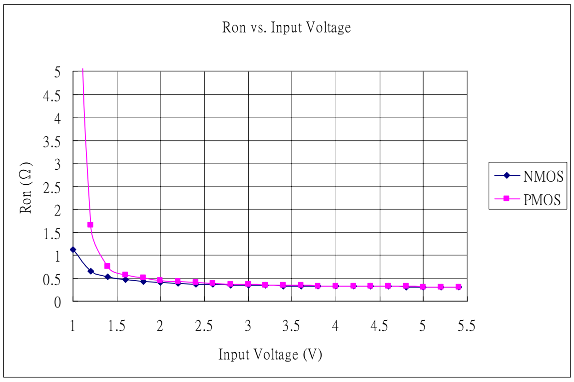
CH1 No Load battery current vs input voltage



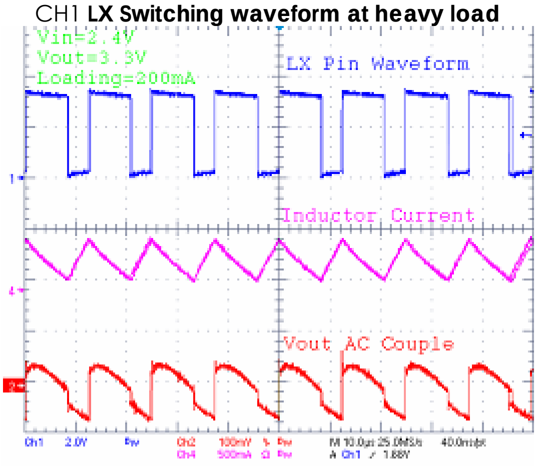
CH1 **LX Switching waveform at no load**



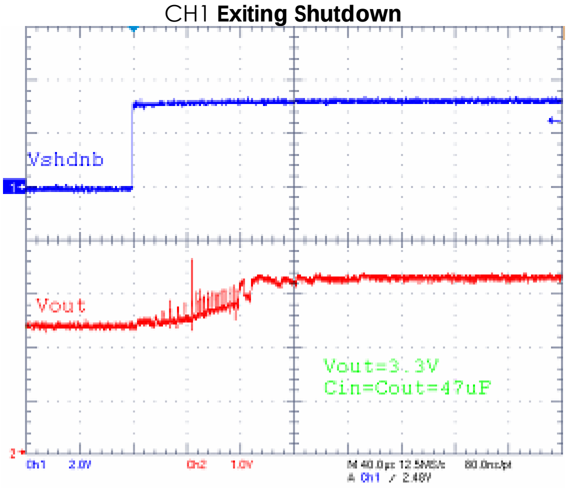
CH1 $R_{DS(ON)}$ vs Input Voltage



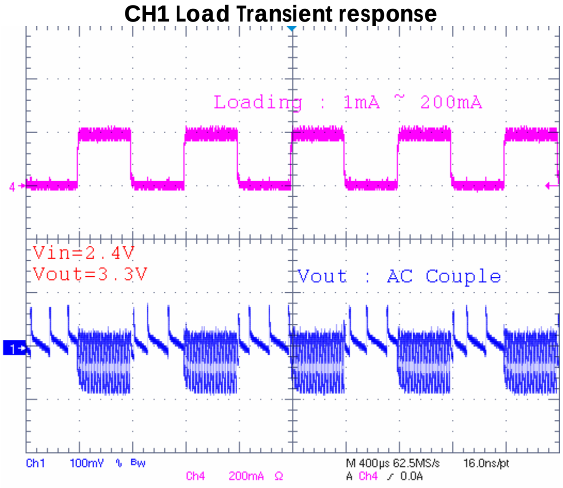
CH1 **LX Switching waveform at heavy load**



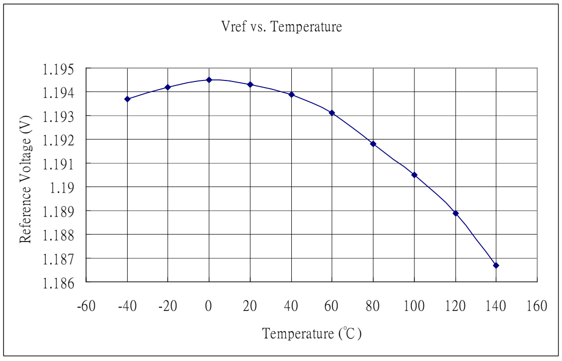
CH1 **Exiting Shutdown**



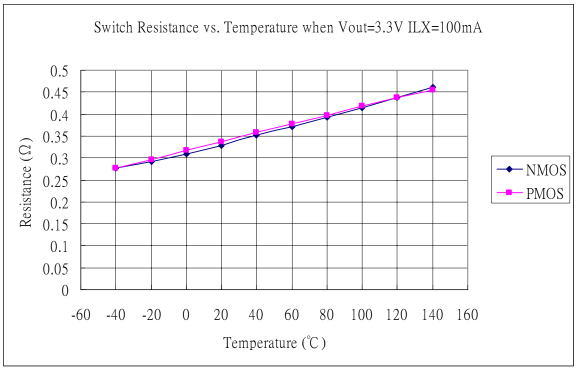
CH1 Load Transient response



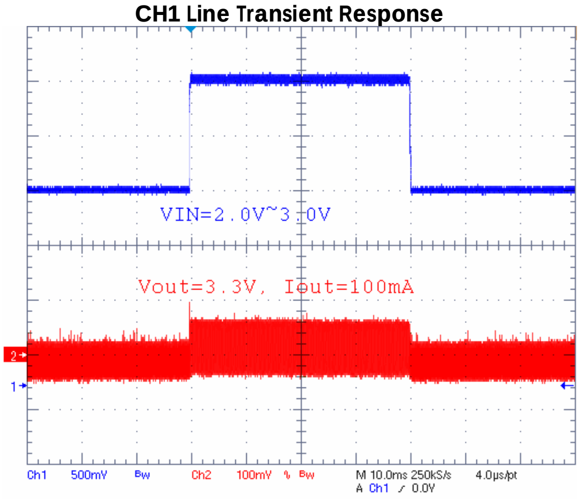
CH1 Vref voltage vs temperature



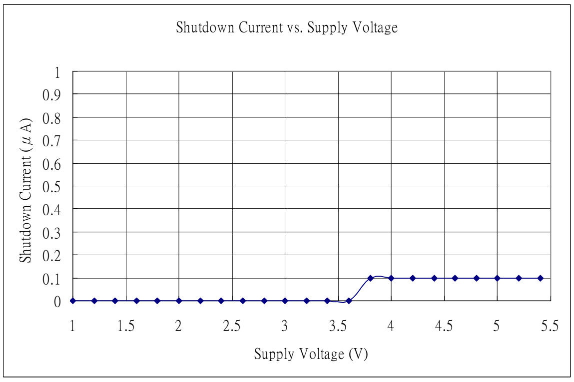
CH1 Switch Ron vs Temperature



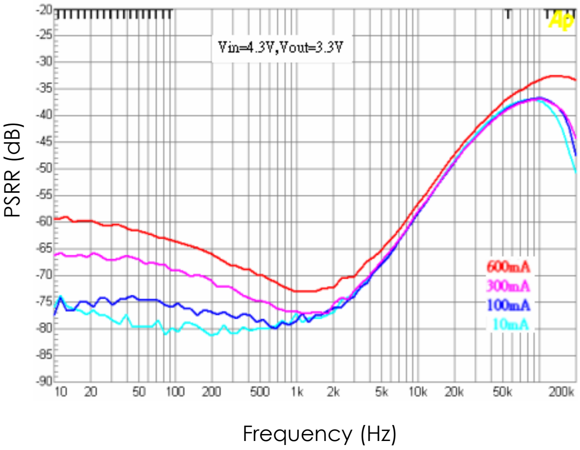
CH1 Line Transient Response

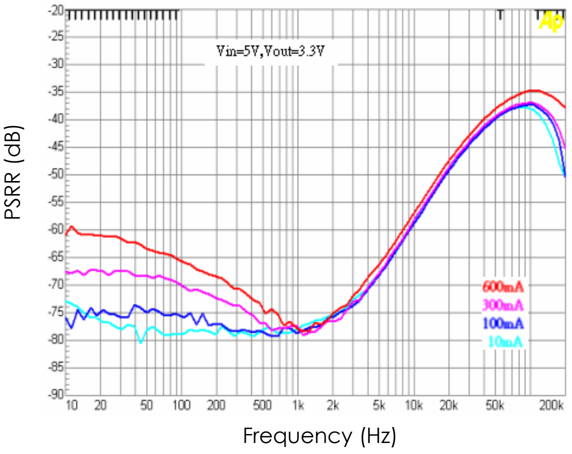


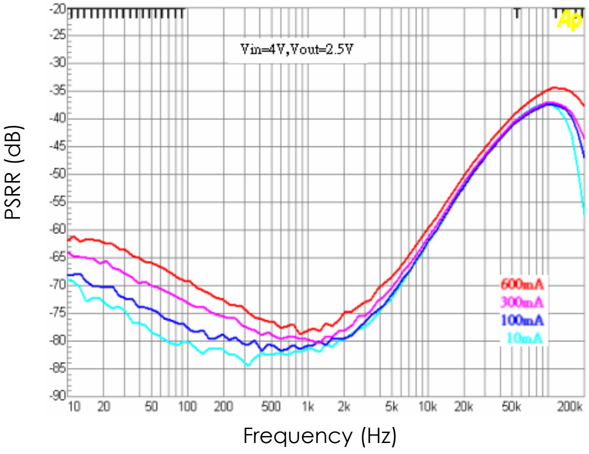
CH1 Shutdown current vs input voltage

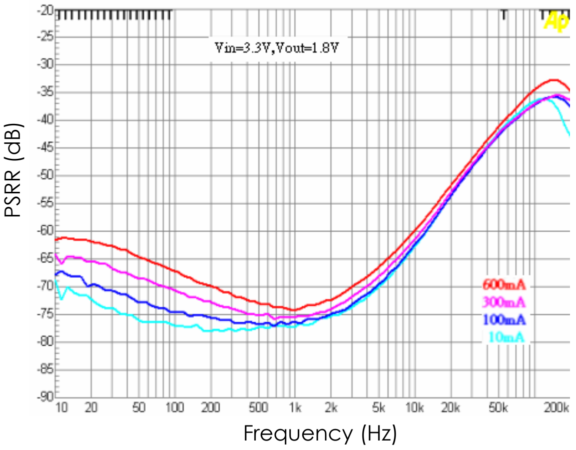


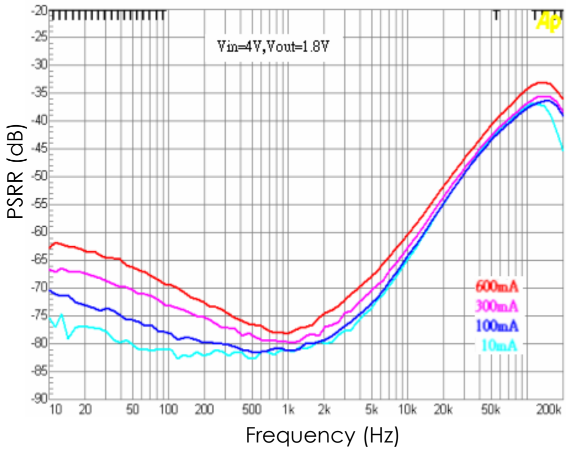
CH2 PSRR vs. Frequency

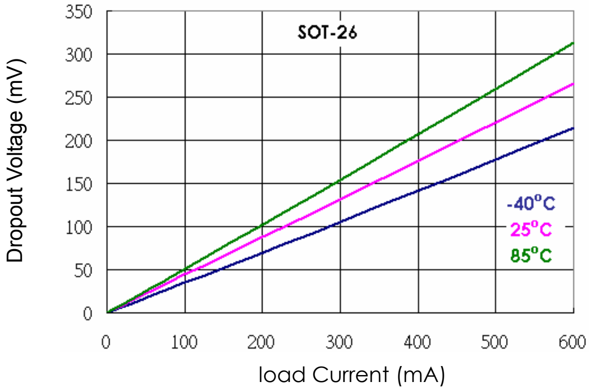


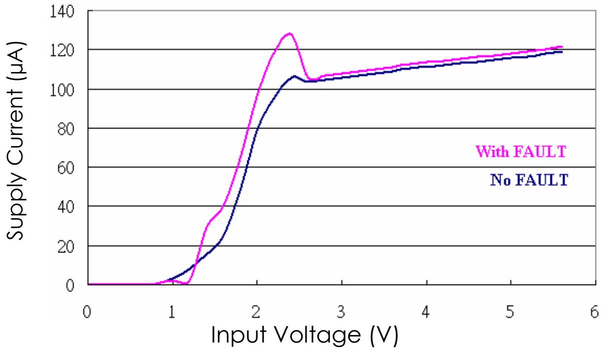

CH2 PSRR vs. Frequency

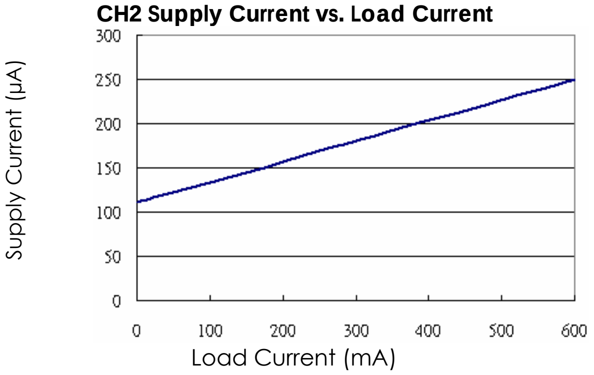

CH2 PSRR vs. Frequency

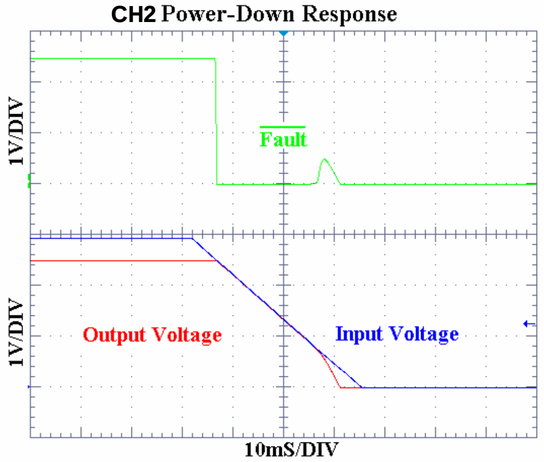

CH2 PSRR vs. Frequency

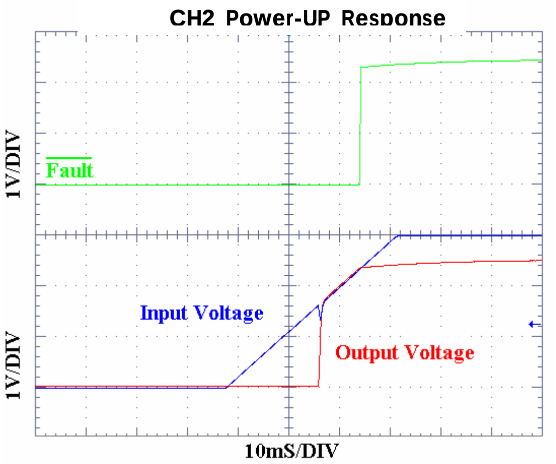

CH2 PSRR vs. Frequency

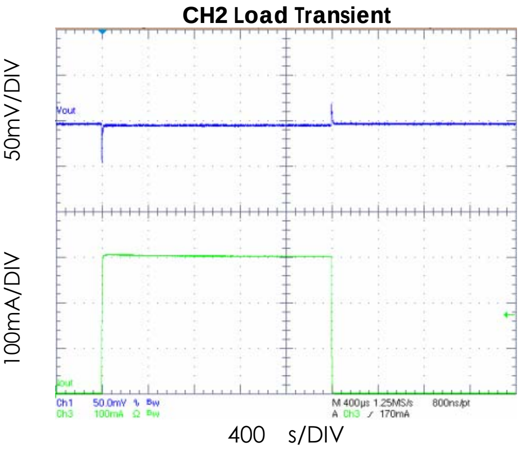

CH2 Dropout Voltage vs. Load Current

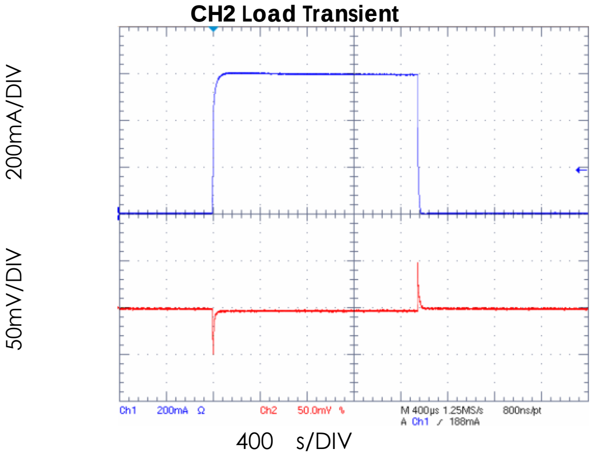

CH2 Supply Current vs. Input Voltage

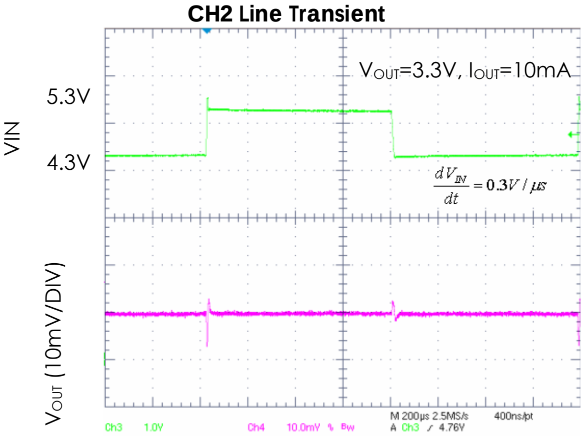

CH2 Supply Current vs. Load Current
Supply Current (µA)
300
250
200
150
100
50
0
0
100
200
300
400
500
600
Load Current (mA)


CH2 Power-Down Response
1V/DIV
Fault
1V/DIV
Output Voltage
Input Voltage
10mS/DIV

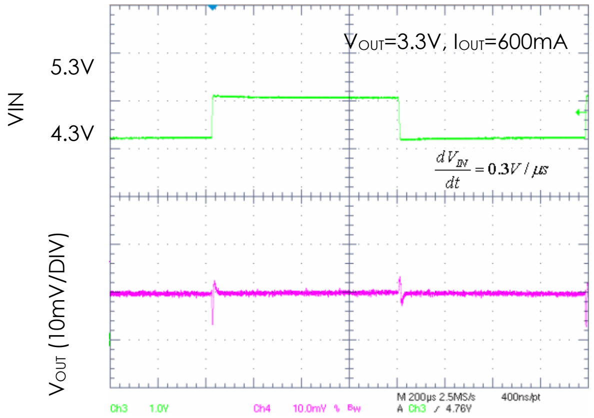

CH2 Power-UP Response
1V/DIV
Fault
1V/DIV
Input Voltage
Output Voltage
10mS/DIV


CH2 Load Transient
50mV/DIV
Vout
100mA/DIV
Iout
Ch1 50.0mV Bw
Ch3 100mA Ω Bw
M 400µs 1.25MS/s 800ns/pt
A Ch3 ⁄ 170mA
400 s/DIV

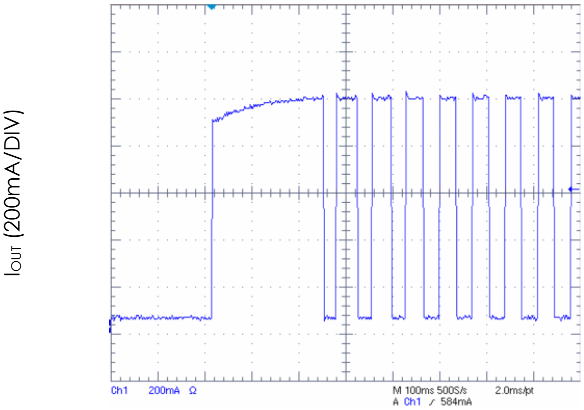

CH2 Load Transient
200mA/DIV
50mV/DIV
Ch1 200mA Ω
Ch2 50.0mV
M 400µs 1.25MS/s 800ns/pt
A Ch1 ⁄ 188mA
400 s/DIV


CH2 Line Transient
VIN
5.3V
4.3V
VOUT=3.3V, IOUT=10mA
dVIN/dt = 0.3V/µs
VOUT (10mV/DIV)
Ch3 1.0V
Ch4 10.0mV Bw
M 200µs 2.5MS/s 400ns/pt
A Ch3 ⁄ 4.76V

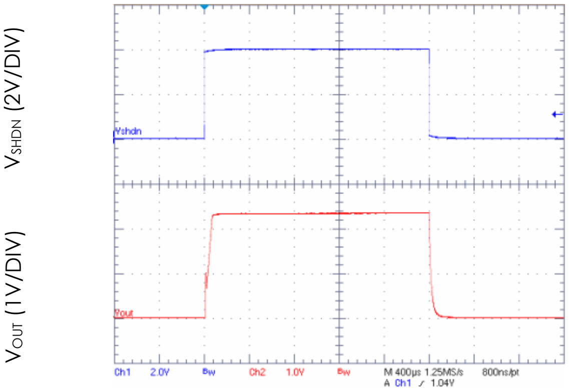
CH2 Line Transient



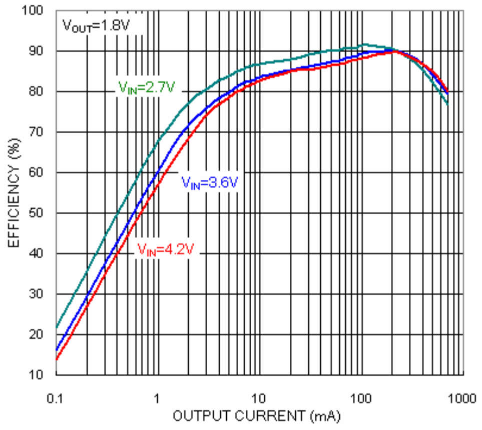
CH2 Current Limit



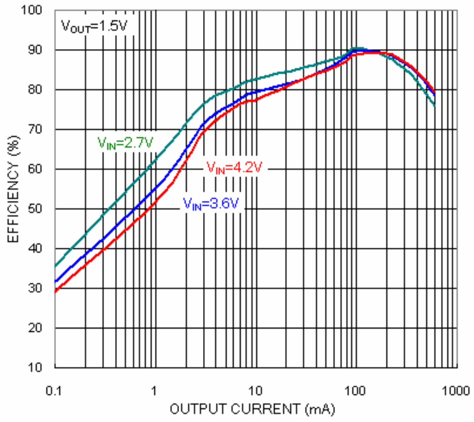
CH2 Enable and Disable



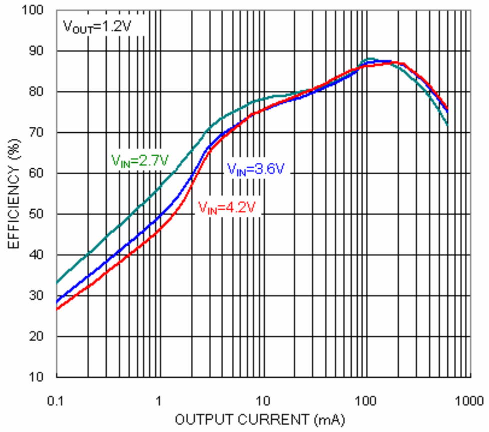
CH3 Efficiency vs Output Current



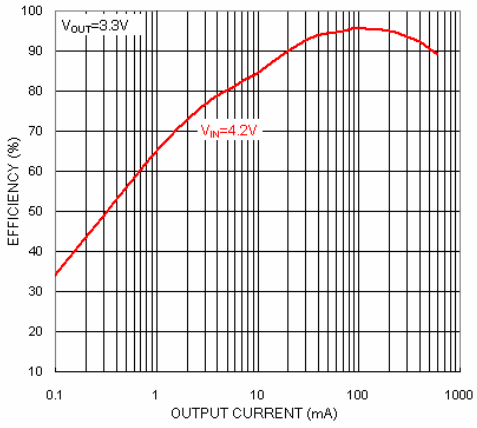
CH3 Efficiency vs Output Current



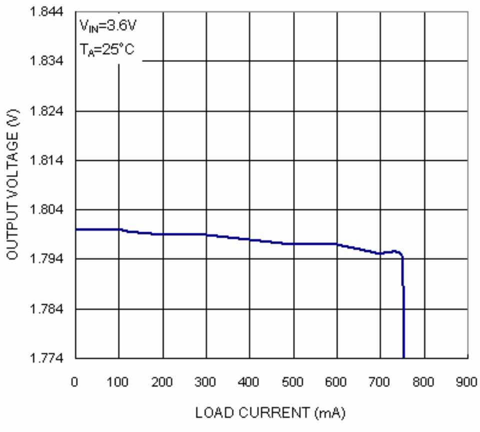
CH3 Efficiency vs Output Current



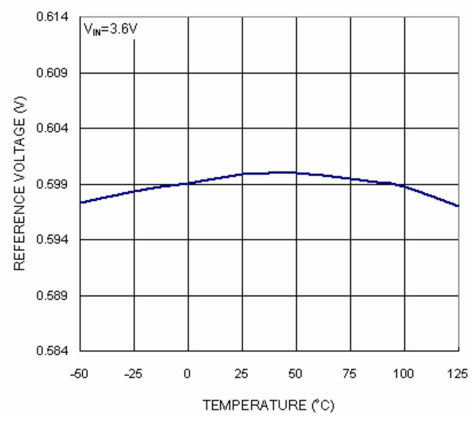
CH3 Efficiency vs Output Current



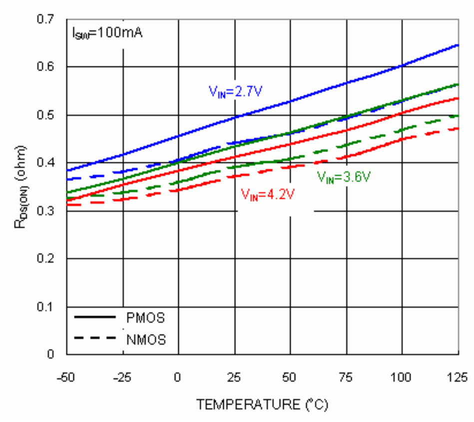
CH3 Output Voltage vs Load Current



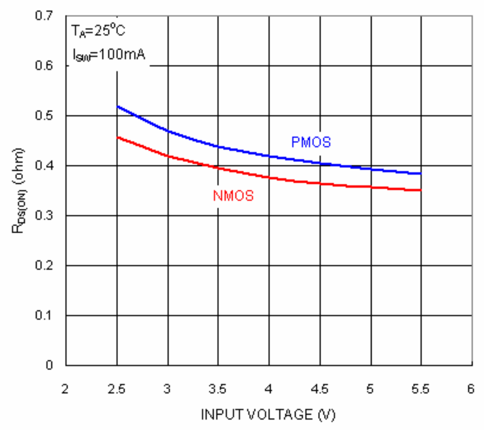
CH3 Reference voltage vs Temperature



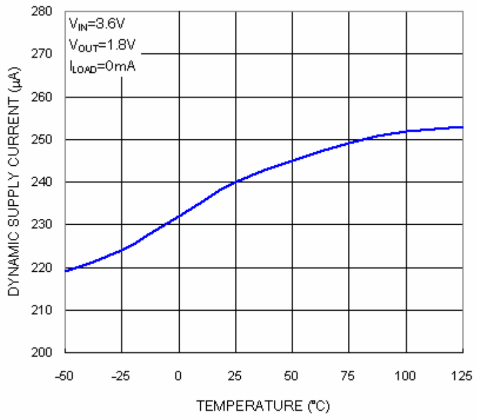
CH3 $R_{DS(ON)}$ vs Temperature



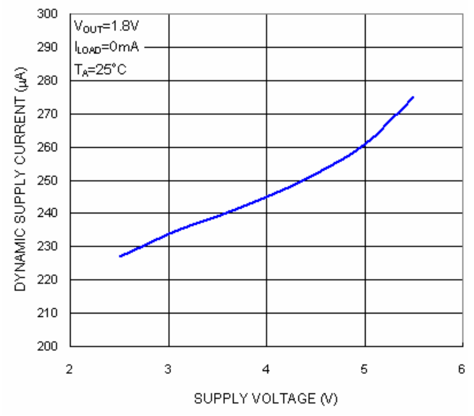
CH3 $R_{DS(ON)}$ vs Input Voltage



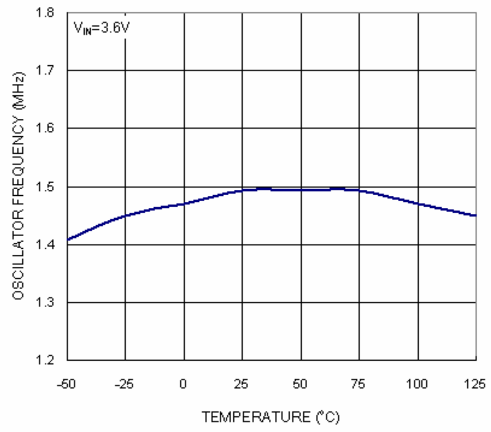
CH3 Dynamic Supply Current vs Temperature



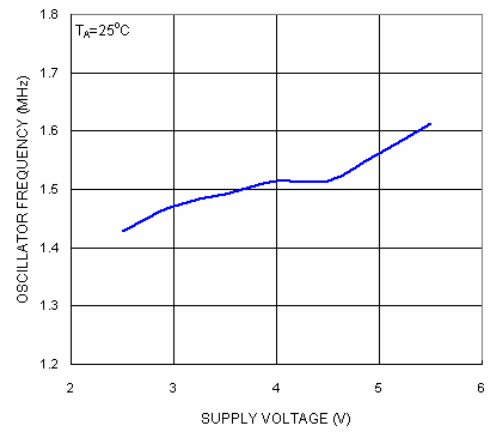
CH3 Dynamic Supply Current vs Supply Voltage



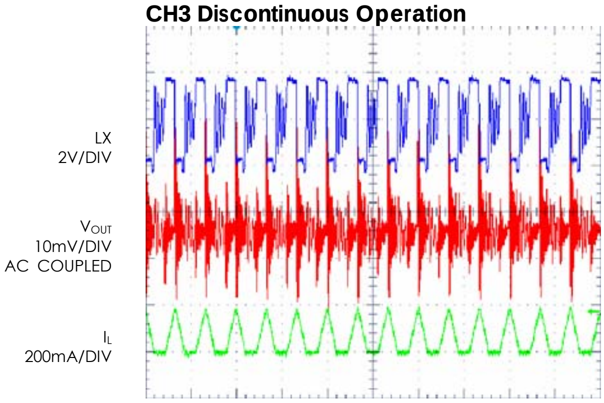
CH3 Oscillator Frequency vs Temperature



CH3 Oscillator Frequency vs Supply Voltage

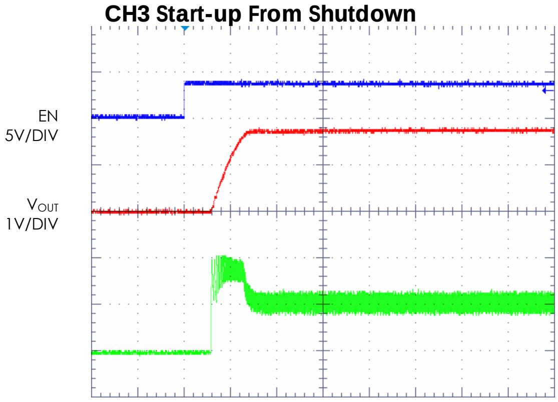


CH3 Discontinuous Operation



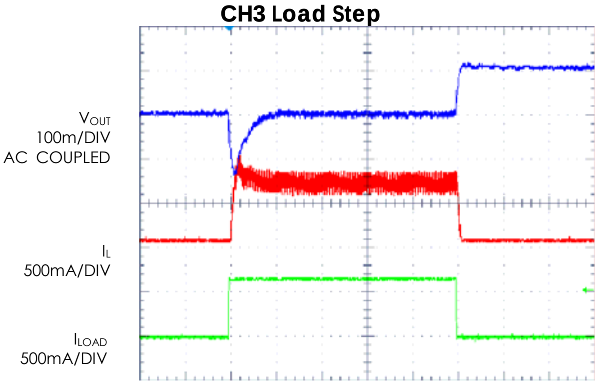
V_{IN}=3.6V 1 µs/DIV
V_{OUT}=1.8V
I_{LOAD}=50mA

CH3 Start-up From Shutdown



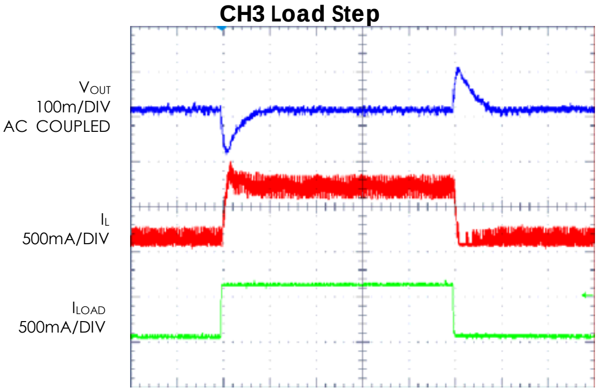
V_{IN}=3.6V 40 µs/DIV
V_{OUT}=1.8V
I_{LOAD}=600mA (3Ω RESISTOR)

CH3 Load Step



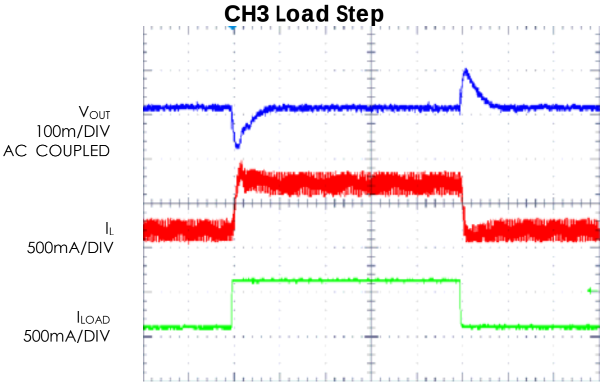
V_{IN}=3.6V 20 µs/DIV
V_{OUT}=1.8V
I_{LOAD}=0mA to 600mA

CH3 Load Step



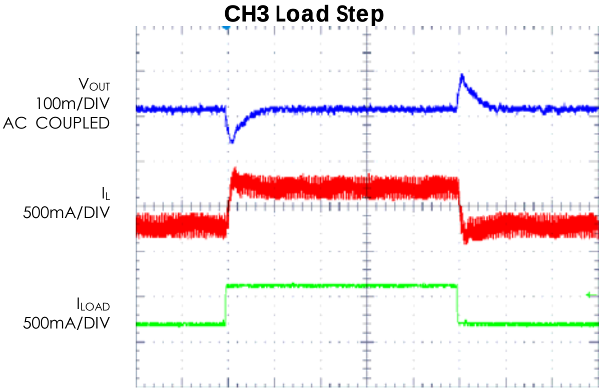
V_{IN}=3.6V 20µs/DIV
V_{OUT}=1.8V
I_{LOAD}=50mA to 600mA

CH3 Load Step



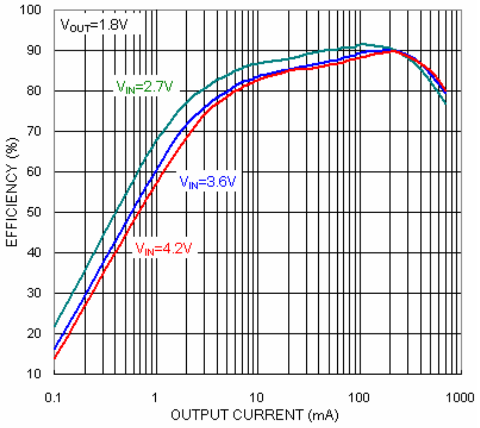
V_{IN}=3.6V 20µs/DIV
V_{OUT}=1.8V
I_{LOAD}=100mA to 600mA

CH3 Load Step

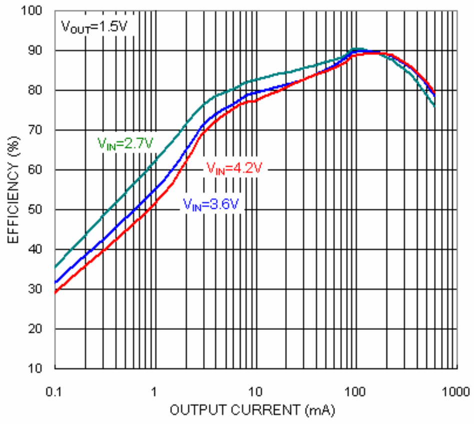


V_{IN}=3.6V 20µs/DIV
V_{OUT}=1.8V
I_{LOAD}=200mA to 600mA

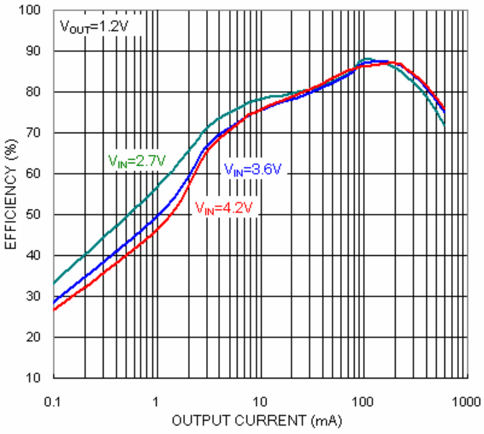
CH4 Efficiency vs Output Current



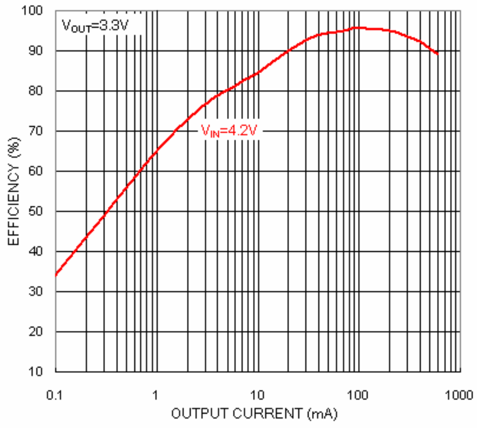
CH4 Efficiency vs Output Current



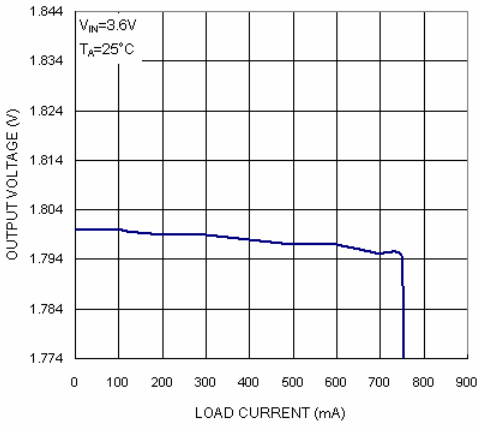
CH4 Efficiency vs Output Current



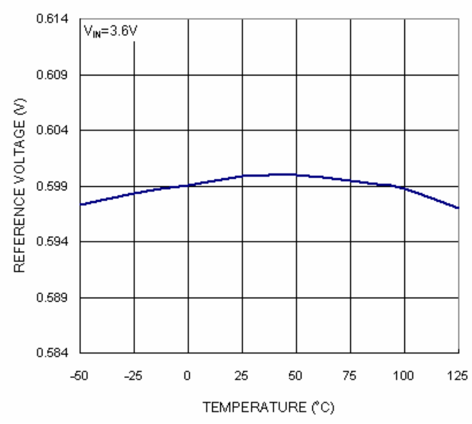
CH4 Efficiency vs Output Current



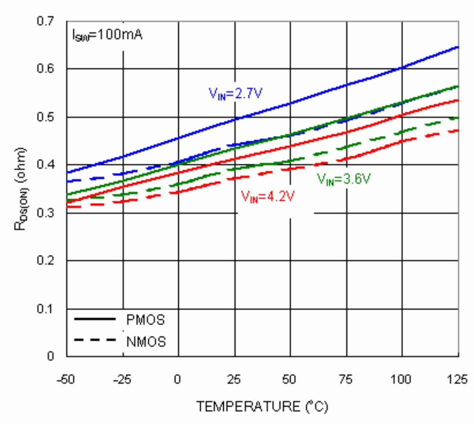
CH4 Output Voltage vs Load Current



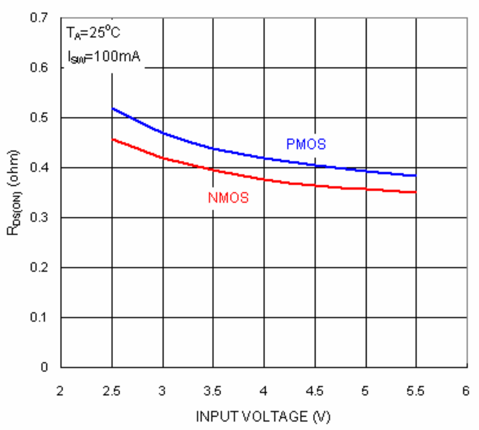
CH4 Reference voltage vs Temperature



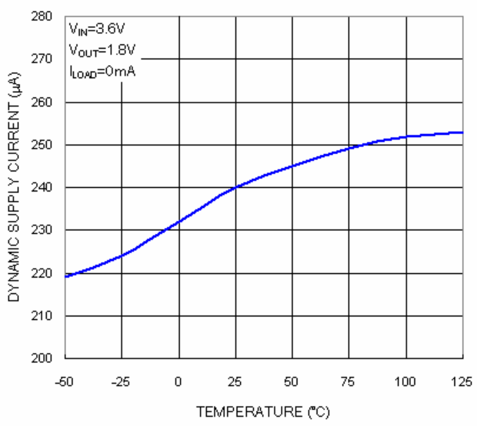
CH4 $R_{DS(ON)}$ vs Temperature



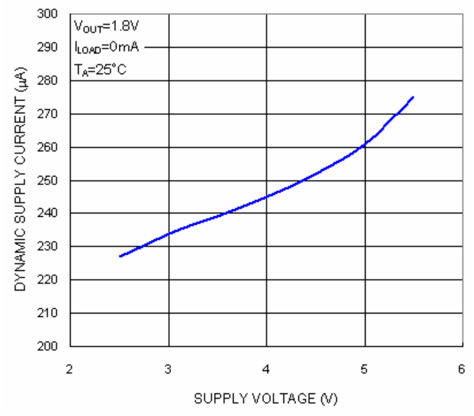
CH4 $R_{DS(ON)}$ vs Input Voltage



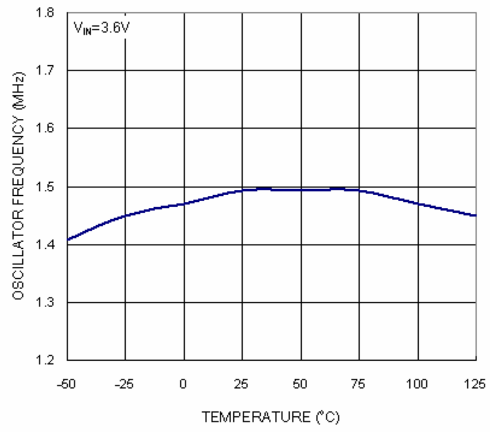
CH4 Dynamic Supply Current vs Temperature



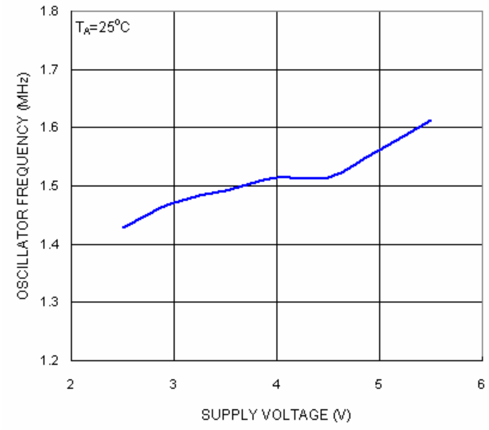
CH4 Dynamic Supply Current vs Supply Voltage



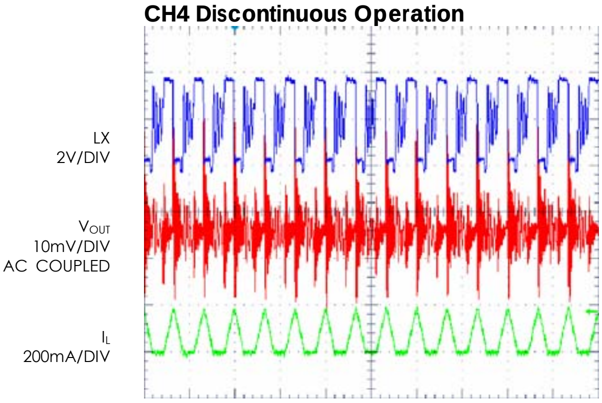
CH4 Oscillator Frequency vs Temperature



CH4 Oscillator Frequency vs Supply Voltage

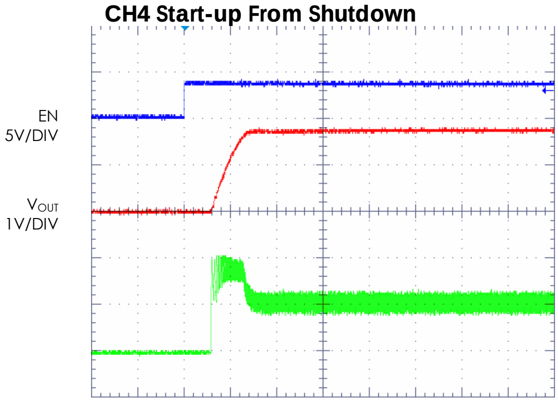


CH4 Discontinuous Operation



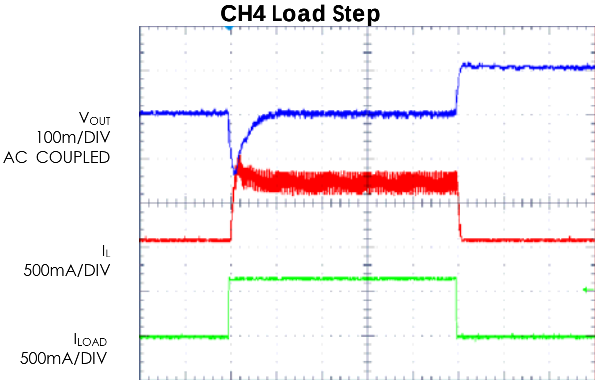
V_{IN}=3.6V 1 μs/DIV
V_{OUT}=1.8V
I_{LOAD}=50mA

CH4 Start-up From Shutdown

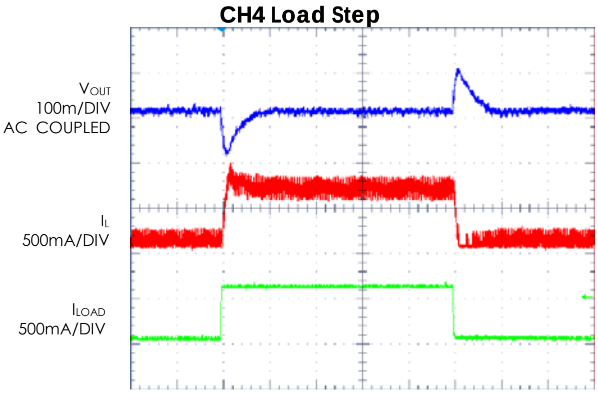


V_{IN}=3.6V 40 μs/DIV
V_{OUT}=1.8V
I_{LOAD}=600mA (3Ω RESISTOR)

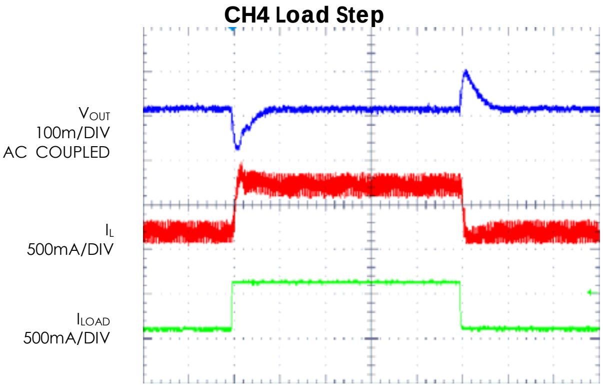
CH4 Load Step



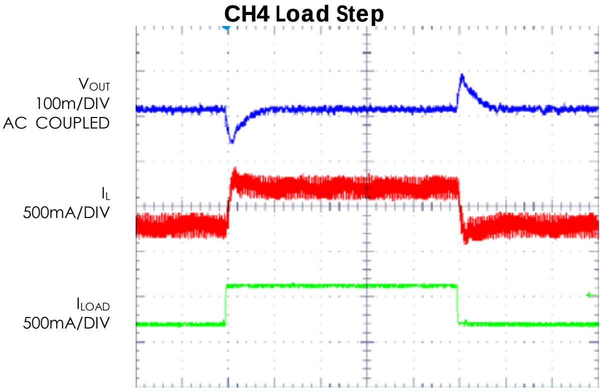
V_{IN}=3.6V 20 μs/DIV
V_{OUT}=1.8V
I_{LOAD}=0mA to 600mA



V_{IN}=3.6V 20μs/DIV
V_{OUT}=1.8V
I_{LOAD}=50mA to 600mA



V_{IN}=3.6V 20μs/DIV
V_{OUT}=1.8V
I_{LOAD}=100mA to 600mA



V_{IN}=3.6V 20μs/DIV
V_{OUT}=1.8V
I_{LOAD}=200mA to 600mA

APPLICATION INFORMATION

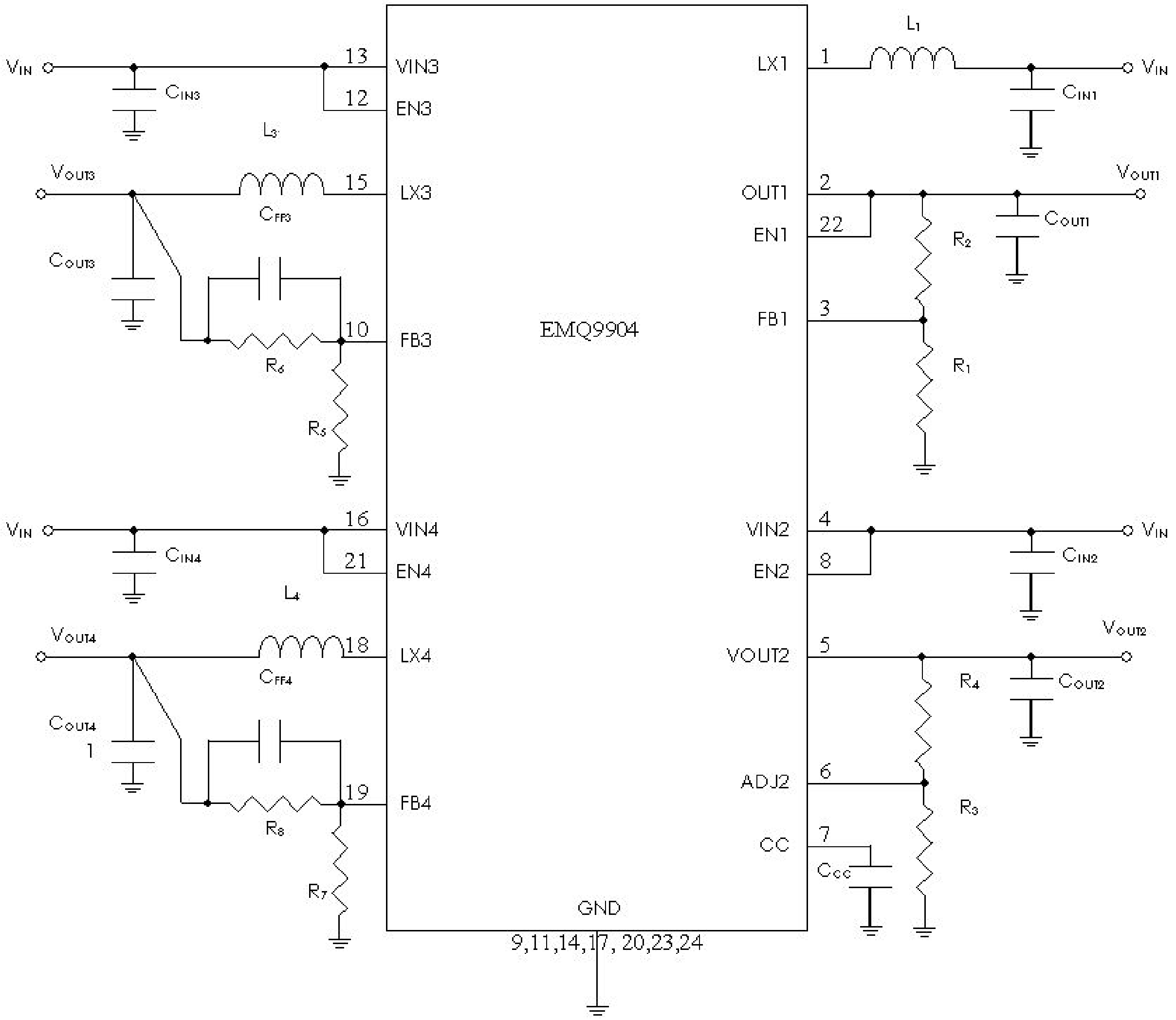


Figure 2. Typical EM9904 Application Circuit That Supports Four Adjustable Output Voltage

APPLICATION INFORMATION

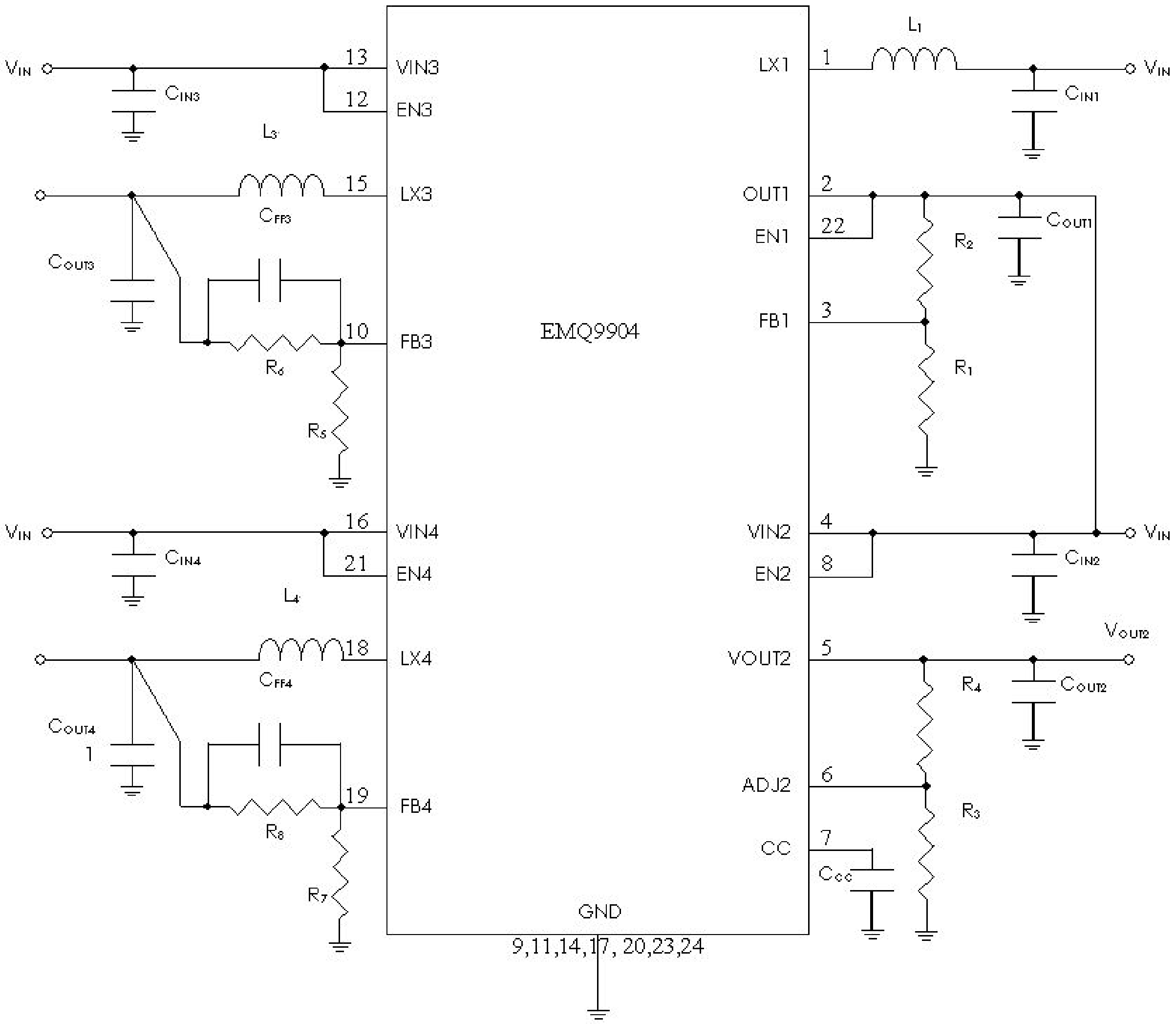


Figure 3. Typical EMQ9904 Application Circuit That Supports Three Adjustable Output Voltage With Improved Boost Ripple Voltage By Cascading Boost and LDO

NOTE A: A 0.1 µF ceramic capacitor is recommended to be placed as close as possible to the OUT1 PIN of the IC under Fig. 2 typical application case.

NOTE B: **Vout1 is set 0.5V higher than Vout2 to get best performance**

Application Information

The EMQ9904 is a high efficiency, 4-channel power management IC for battery-powered, portable devices application.

The four channels are listed as following：

CH1：Battery powered, Synchronous Boost converter CH2：High PSRR, low noise, low dropout 600mA LDO
CH3/4：600mA Synchronous Buck converters
All 4 channels are Vout adjustable

CH1：Battery powered, Synchronous Boost converter

This channel is high efficiency, build-in synchronous, PFM operation DC-DC converter.
The start-up voltage of CH1 is as low as 0.9V and it operates with an input voltage (V_{IN1}) down to 0.6V. Quiescent supply current is only 26μA. The internal P-MOSFET on resistance is typically 0.4Ω to improve overall efficiency by minimizing AC losses. The output voltage of CH1 (V_{OUT1}) can be easily set by two external resistors from 1.8V to 5.5V, connecting FB1 to OUT1 to get 3.3V, or connecting to GND to get 5.0V.
The current limit is 1A still it can reliably provide up to 500mA load current and still maintained a decent efficiency.

■ CH1 PFM Control Scheme

The key feature of the design is to apply a unique minimum off-time, constant on-time and current-limited Pulse Frequency Modulation (PFM) control scheme with the ultra-low quiescent current. The peak current of the internal N MOSFET power switch can be fixed at 1.0A. The switching frequency can be up to 200KHz depending on the loading current. The minimum off-time is 1μS and the maximum on-time is 4μS.

■ Synchronous Rectification

With the internal synchronous rectifier, it eliminates the need for an external Schottky diode. This saves the cost and board space. During the cycle of off-time, P-MOSFET turns on and shunts N- MOSFET. Due to the low turn-on resistance of MOSFET, synchronous rectifier can significantly improve efficiency without an additional external Schottky diode. Thus, the conversion efficiency can be as high as 93%.

■ Reference Voltage

The reference voltage (V_{REF}) is nominally 1.195V with excellent temperature performance. This voltage helps the converter to build expected output voltage within specifications.

■ CH1 Shutdown

The device is in shutdown mode when EN1 is low. At shutdown mode, the current can flow from battery to output due to body diode of the P-MOSFET. V_{OUT1} falls to approximately V_{IN1}-0.6V and LX1 remains in high impedance. The C_{Load} and load current at OUT1 determine the rate of how V_{OUT1} decays. Shutdown can be pulled as high as 6V regardless of the voltage at OUT1.

■ CH1 Selecting the Output Voltage

V_{OUT} can be simply set to 3.3V/5.0V by connecting FB1 pin to OUT1/GND due to the use of internal resistor divider in the IC. In order to adjust output voltage, a resistor divider is connected to OUT1, FB1 and GND. The V_{OUT1} can be calculated by the following equation:

R2=R1 [(V_{OUT1} / V_{REF1})-1] ....(1)

Where V_{REF1} =1.195V and V_{OUT1} is ranging from 1.8V to 5.5V. The recommended R1 is 240K .

■ CH1 Component Selection

1. Inductor Selection

An inductor value of 22μH performs well in most applications. The device also works with inductors in the 10μH to 47μH range. An inductor with higher peak inductor current tends a higher output voltage ripple (I_{PEAK} × output filter capacitor ESR). The inductor's DC resistance significantly affects efficiency. We can calculate the maximum output current as follows:

$$I_{OUT1}(MAX) = \frac{V_{IN1}}{V_{OUT1}}\left[I_{LIM1} - t_{OFF}\left(\frac{V_{OUT1} - V_{IN1}}{2 \times L}\right)\right]\eta \text{........(2)}$$

where I_{OUT} (MAX)=max. output current in amps

V_{IN}=input voltage

L = inductor value in μH

η = efficiency (typically 0.9)

t_{OFF} = LX1 switch' off-time in μS

I_{LIM} =1.0A

2. Capacitor Selection

The output ripple voltage of CH1 relates with the peak inductor current and the output capacitor's ESR. Besides output ripple voltage, the output ripple current also needs to be concerned. A filter capacitor with low ESR is helpful to the efficiency

and steady state output current. A smaller capacitor (down to 47μF with higher ESR) is acceptable for light loads or in applications of which can tolerate higher output ripple.

■ CH1 Ripple Voltage Reduction

The output ripple voltage of CH1 can be significant improved by using two or three parallel output capacitors. The addition of an extra input capacitor also results in a stable output voltage.

■ CH1 PCB Layout and Grounding

Since The Step-up DC/DC converter's switching frequency can range up to 200kHz, it is sensitive to how PCB is layout. PCB layout is important for minimizing ground bounce and noise. The GND pin should be placed close to the ground plane. Keep the Step-up DC/DC converter's GND pin and the ground leads of the input and output filter capacitors as short as possible. In addition, keep all connections to the FB1 and LX1 pins as short as possible. In particular, in case of using external feedback resistors, locate them as close to the FB as possible. To maximize output power and efficiency and minimize output ripple voltage, use a ground plane right under the soldered IC.

CH2：High PSRR, low noise, low dropout 600mA LDO

The LDO adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R3, R4) to sample the output voltage (V_{OUT2}) for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the temperature protection and current protection circuitry.

■ CH2 Output Voltage Control

The LDO allows direct user control of the output voltage in accordance with the amount of negative feedback present. To see the explicit relationship between the output voltage and the negative feedback, it is convenient to conceptualize the LDO as an ideal non-inverting operational amplifier with a fixed DC reference voltage V_{REF2} at its non-inverting input. Such a conceptual representation of the LDO in closed-loop configuration is shown in Figure 4. This ideal op amp features an ultra-high input resistance such that its inverting input voltage is virtually fixed at V_{REF2}. The output voltage is therefore given by:

$$V_{OUT2} = V_{REF2}\left[\frac{R_4}{R_3} + 1\right] \text{..(3)}$$

This equation can be rewritten in the following form to facilitate the determination of the resistor values for a chosen output voltage:

$$R_4 = R_3\left[\frac{V_{OUT2}}{1.19V} - 1\right] \text{..(4)}$$

Set R3 equal to 100kΩ to optimize for overall accuracy, power supply rejection, noise, and power consumption.

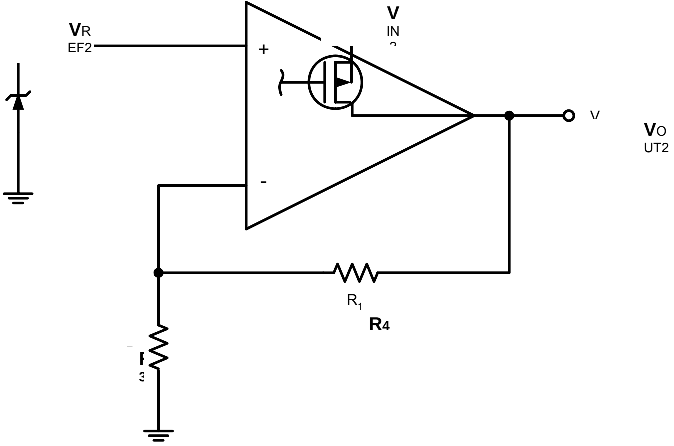


Figure 4. Simplified Regulator Topology

■ CH2 Output Capacitor

The LDO is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the LDO are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

■ CH2 No-Load Stability

The LDO is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

■ CH2 Input Capacitor

A minimum input capacitance of 1μF is required for the LDO. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

■ CH2 Compensation (Noise Bypass) Capacitor

Substantial reduction in the output voltage noise of the LDO is accomplished through the connection of the noise bypass capacitor C_{CC} (33nF optimum) between CC pin and the ground. Because CC pin connects directly to the high impedance output of the bandgap reference circuit, the level of the DC leakage currents in the C_{CC} capacitors used will adversely reduce the regulator output voltage. This sets the DC leakage level as the key selection criterion of the C_{CC} capacitor types for use with the LDO. NPO and COG ceramic capacitors typically offer very low leakage. Although the use of the C_{CC} capacitors does not affect the transient response, it does affect the turn-on time of the regulator. Tradeoff exists between output noise level and turn-on time when selecting this capacitor value.

■ CH2 Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The LDO relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction

temperature T_J exceeding 165°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA}\,(PD) + T_A \quad \text{...} \quad (5)$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

$$P_D = I_{OUT}\,(V_{IN} - V_{OUT}) \quad \text{..} \quad (6)$$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermal overloading the LDO, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

■ CH2 Shutdown

CH2 enters the sleep mode when the EN2 pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1nA. Such a low supply current makes the LDO best suited for battery-powered applications. The maximum guaranteed voltage at the EN2 pin for the sleep mode to take effect is 0.4V. A minimum guaranteed voltage of 1.2V at the EN2 pin would activate the LDO. Direct connection of the EN2 pin to the V_{IN2} to keep the regulator on is allowed for the LDO. In this case, the EN2 pin must not exceed the supply voltage V_{IN2}.

■ Fast Start-Up

Fast start-up time is important for overall system efficiency improvement. The LDO assures fast start-up speed when using the optional noise bypass capacitor (C_{CC}). To shorten start-up time, the LDO internally supplies a 500μA current to charge up the capacitor until it reaches about 90% of its final value.

CH3/4：600mA Synchronous Buck converters

The typical application circuit of the current mode DC/DC converters is shown in Fig.5.

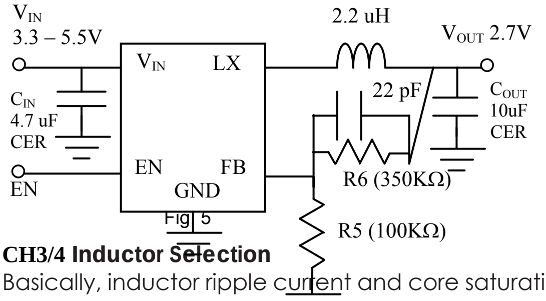


Fig. 5

CH3/4 Inductor Selection

Basically, inductor ripple current and core saturation are two factors considered to decide the Inductor value.

$$\Delta I_L = \frac{1}{f \cdot L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{.................................} \quad (7)$$

The Eq. 7 shows the inductor ripple current is a function of frequency, inductance, V_{IN} (V_{IN3}, V_{IN4})

and V_{OUT} (V_{OUT3}, V_{OUT4}). It is recommended to set ripple current to 40% of max. load current. A low ESR inductor is preferred.

CH3/4 C_{IN} and C_{OUT} Selection

A low ESR input capacitor can prevent large voltage transients at V_{IN} (V_{IN3}, V_{IN4}). The RMS current of input capacitor is required larger than I_{RMS} calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}\left(V_{IN}-V_{OUT}\right)}}{V_{IN}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

ESR is an important parameter to select C_{OUT} (C_{OUT3}, C_{OUT4}). The output ripple $\triangle V_{OUT}$ ($\triangle V_{OUT3}$, $\triangle V_{OUT4}$) is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}} \right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

Higher values, lower cost ceramic capacitors are now available in smaller sizes. These ceramic capacitors have high ripple currents, high voltage ratings and low ESR that make them ideal for switching regulator applications. Optimize very low output ripple and small circuit size is doable from C_{OUT} selection since C_{OUT} does not affect the internal control loop stability. It is recommended to use the X5R or X7R which have the best temperature and voltage characteristics of all the ceramics for a given value and size.

CH3/4 Output Voltage (V_{OUT3}, V_{OUT4})

The output voltage can be determined by following equation:

$$V_{OUT} = 0.6\,V\left(1+\frac{R_6}{R_5}\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (10)$$

CH3 Case, Replace R_5 as R_7, R_6 as R_8 in CH4 case.

CH3/4 Thermal Considerations

Although thermal shutdown is build-in in the step-down DC/DC converter(s) that protects the device from thermal damage, the total power dissipation that the converter(s) can sustain should be base on the package thermal capability. The formula to ensure the safe operation is shown in Note 3.

To avoid the DC/DC converter(s) from exceeding the maximum junction temperature, the user will need to do some thermal analysis.

CH3/4 Guidelines for PCB Layout

To ensure proper operation of the DC/DC converter(s) , please note the following PCB layout guidelines:

1. The GND trace, the LX (LX3, LX4) trace and the V_{IN} (V_{IN3}, V_{IN4}) trace should be kept short, direct and wide.
2. V_{FB} (FB3, FB4) pin must be connected directly to the feedback resistors. Resistive divider R_5/R_6 (CH3); R_7/R_8 (CH4) must be connected and parallel to the output capacitor C_{OUT} (C_{OUT3}, C_{OUT4}).
3. The Input capacitor C_{IN} (C_{IN3}, C_{IN4}) must be connected to pin V_{IN} (V_{IN3}, V_{IN4}) as closely as possible.
4. Keep LX (LX3, LX4) node away from the sensitive V_{FB} (FB3, FB4) node since this node is with high frequency and voltage swing.
5. Keep the (–) plates of C_{IN} (C_{IN3}, C_{IN4}) and C_{OUT} (C_{OUT3}, C_{OUT4}) as close as possible.

CH3/4 Self-Enable Application

A self-enable function could be used when the step-down DC/DC converter(s) is (are) connected as fig. 6.

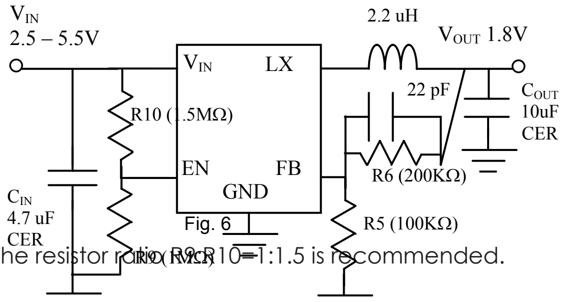


Fig. 6

The resistor ratio R9:R10=1:1.5 is recommended.

CH3/4 Design Example

Assume the Step-down DC/DC converter(s) is (are) used in a single lithium-ion battery-powered application. The V_{IN} (V_{IN3}, V_{IN4}) range will be about 2.7V to 4.2V. Output voltage (V_{OUT3}, V_{OUT4}) is 1.8V.

With this information we can calculate L using equation:

$$L = \frac{1}{f \cdot \Delta I_L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (11)$$

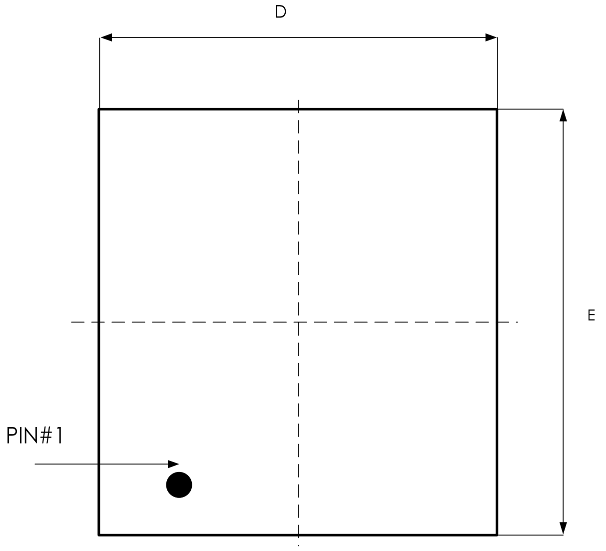
Substituting V_{OUT} = 1.8V, V_{IN} = 4.2V, I_L = 240mA and f = 1.5MHz in eq. 12 gives:

$$L = \frac{1.8V}{1.5MHz \cdot 240mA}\left(1 - \frac{1.8V}{4.2V}\right) = 2.86\mu H \ldots\ldots\ldots\ldots (12)$$

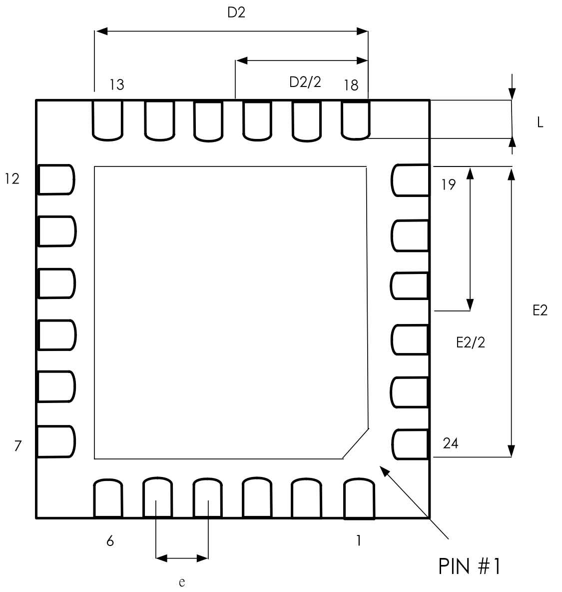
A 2.2μH inductor could be chose with this application.

A greater inductor with less equivalent series resistance makes best efficiency. C_{IN} (C_{IN3}, C_{IN4}) will require an RMS current rating of at least $I_{LOAD(MAX)}/2$ and low ESR. In most cases, a ceramic capacitor will satisfy this requirement.

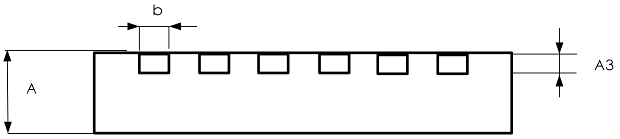
TQFN-24 4x4x0.75mm OUTLINE DIMENSION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.700	0.750	0.800	0.027	0.029	0.031
A3	0.195	0.203	0.211	0.0077	0.0080	0.0083
b	0.180	0.230	0.300	0.007	0.009	0.012
D	3.925	4.000	4.075	0.154	0.157	0.160
E	3.925	4.000	4.075	0.154	0.157	0.160
e	0.50 BSC			0.020 BSC		
L	0.300	0.350	0.400	0.012	0.014	0.016
D2/E2	2.50/2.50	2.65/2.65	2.80/2.80	0.098/0.098	0.104/0.104	0.110/0.110

Revision History

Revision	Date	Description
2.0	2009.05.26	EMP transferred from version 1.0

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