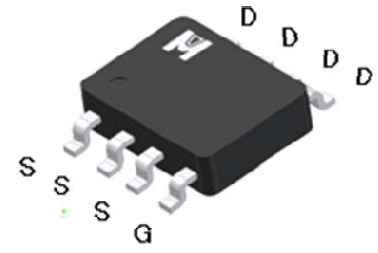
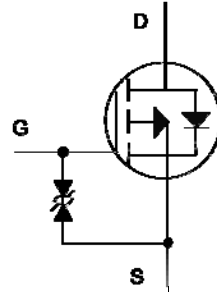


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DS(on)} (MAX.)$	8.5m Ω
I_D	-15A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ESD Protection



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	-15	A
	$T_C = 100\text{ }^\circ\text{C}$		-11	
Pulsed Drain Current ¹		I_{DM}	-60	
Avalanche Current		I_{AS}	-25	
Avalanche Energy	$L = 0.1\text{mH}, I_D = -25\text{A}, R_G = 25\text{ }\Omega$	E_{AS}	31.25	mJ
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	2.5	W
	$T_A = 100\text{ }^\circ\text{C}$		1	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = -15\text{V}$, $L = 0.1\text{mH}$, $V_G = -10\text{V}$, $I_L = -15\text{A}$, Rated $V_{DS} = -30\text{V}$ P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT		
			MIN	TYP	MAX			
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.5	-3			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 10	μA		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA		
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			-10			
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-15			A		
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -12A$		7	8.5	$m\Omega$		
		$V_{GS} = -4.5V, I_D = -9A$		12	15			
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -12A$		26		S		
DYNAMIC								
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		3091		pF		
Output Capacitance	C_{oss}			476				
Reverse Transfer Capacitance	C_{rss}			404				
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		3.5		Ω		
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = -15V, V_{GS} = -10V, I_D = -10A$		54		nC		
	$Q_g(V_{GS}=4.5V)$			32				
Gate-Source Charge ^{1,2}	Q_{gs}			7.3				
Gate-Drain Charge ^{1,2}	Q_{gd}			13				
Turn-On Delay Time ^{1,2}	$t_{d(on)}$		$V_{DS} = -15V, I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7\Omega$		24			nS
Rise Time ^{1,2}	t_r				20			
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			70				
Fall Time ^{1,2}	t_f			12				
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)								
Continuous Current	I_S				-3.6	A		
Pulsed Current ³	I_{SM}				-14.4			
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			-1.2	V		
Reverse Recovery Time	t_{rr}	$I_F = I_S, di_F/dt = 100A / \mu S$		52		nS		
Reverse Recovery Charge	Q_{rr}			60		nC		

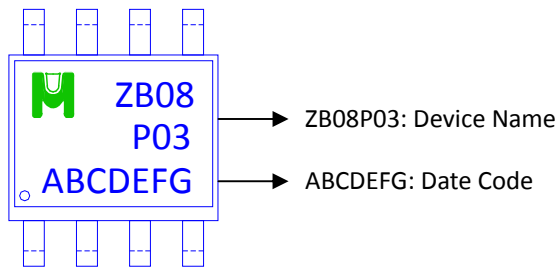
¹Pulse test : Pulse Width $\leq 300\ \mu sec$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

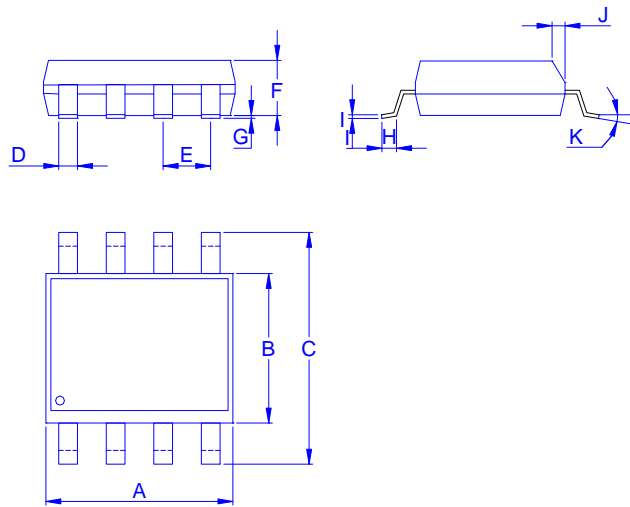
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMZB08P03G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

