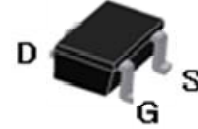
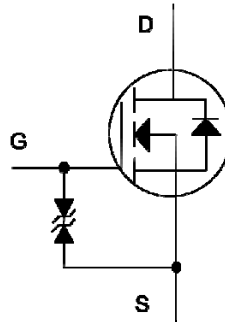


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	100V
$R_{DSON (MAX.)}$	200m $\Omega$
$I_D$	1.7A



Pb-Free Lead Plating & Halogen Free

ESD Protection



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	1.7	A
	$T_A = 100\text{ }^\circ\text{C}$		1.1	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	6.8	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	1.25	W
	$T_A = 100\text{ }^\circ\text{C}$		0.5	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to- Ambient	$R_{\theta JA}$		100	$^\circ\text{C} / \text{W}$

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

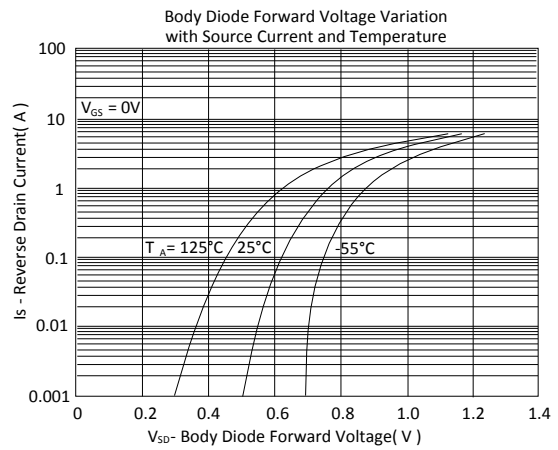
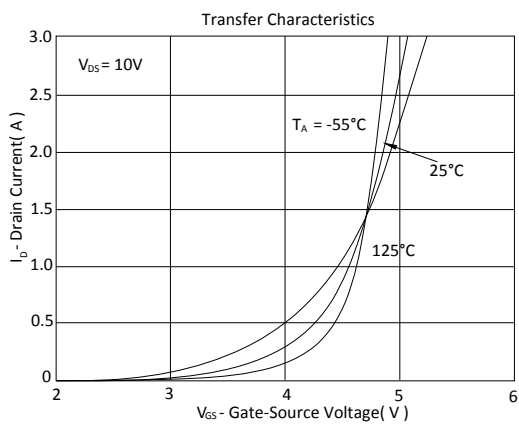
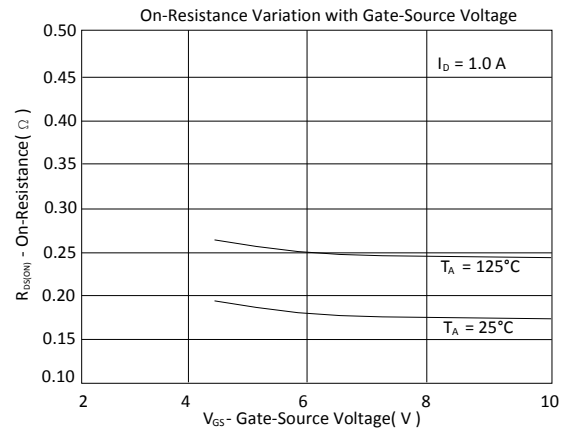
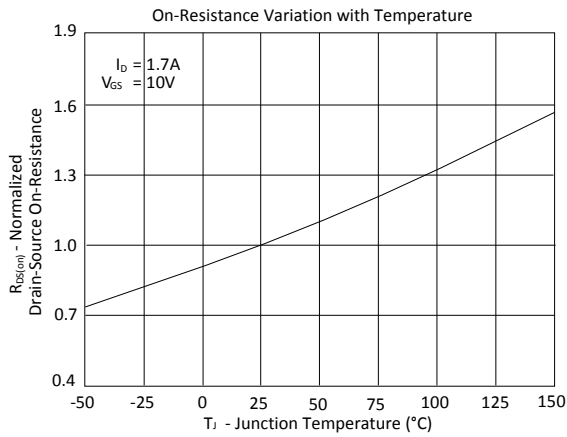
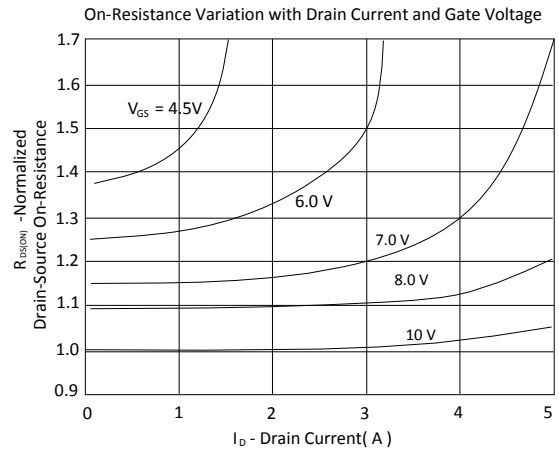
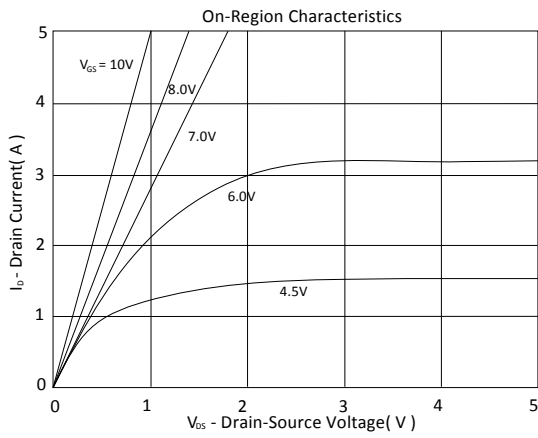
ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

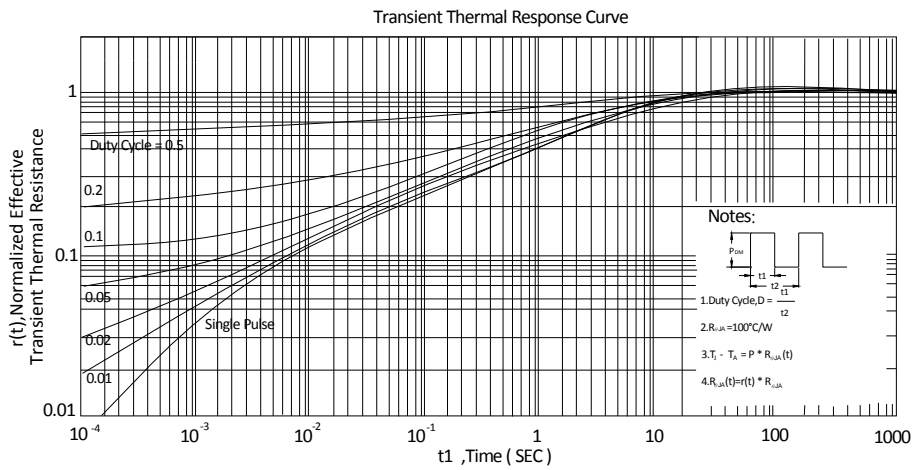
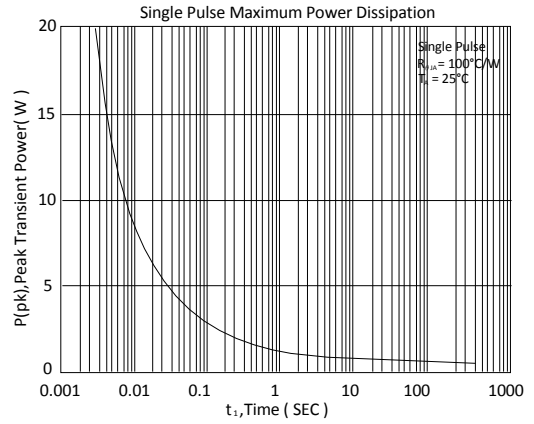
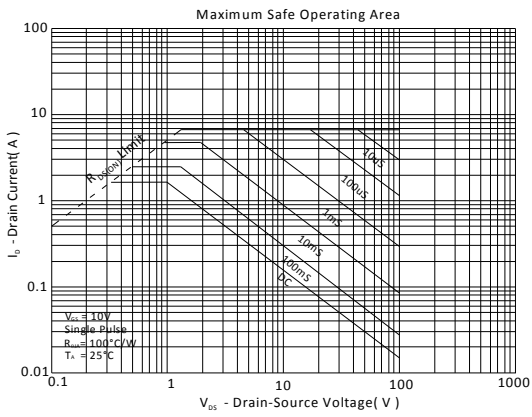
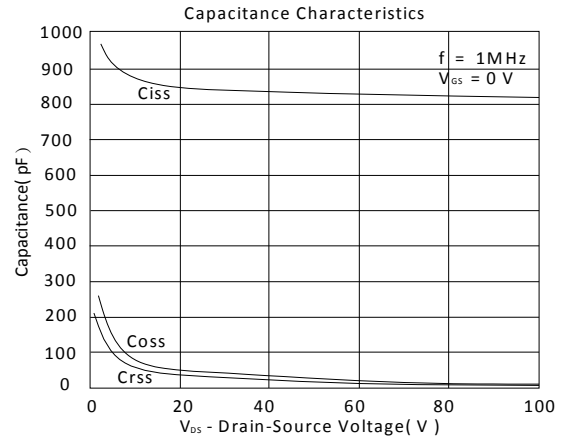
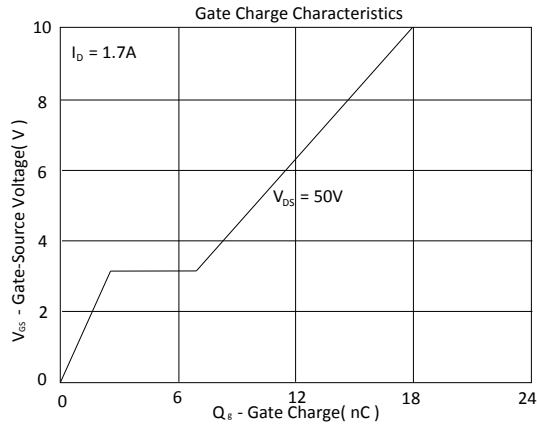
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	100			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	2	3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±16V			±30	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 70V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 10V	1.7			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.7A		170	200	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 1.0A		185	235	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 1.7A		4		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 50V, f = 1MHz		830		pF
Output Capacitance	C <sub>oss</sub>			30		
Reverse Transfer Capacitance	C <sub>rss</sub>			23		
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.7A		17.9		nC
Gate-Source Charge <sup>1,2</sup>	Q <sub>gs</sub>			2.3		
Gate-Drain Charge <sup>1,2</sup>	Q <sub>gd</sub>			5.0		
Turn-On Delay Time <sup>1,2</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 1A, V <sub>GS</sub> = 10V, R <sub>GS</sub> = 6Ω		20		nS
Rise Time <sup>1,2</sup>	t <sub>r</sub>			25		
Turn-Off Delay Time <sup>1,2</sup>	t <sub>d(off)</sub>			30		
Fall Time <sup>1,2</sup>	t <sub>f</sub>			30		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				1.7	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				6.8	
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			1.1	V
Reverse Recovery Time	t <sub>rr</sub>			30		nS
Reverse Recovery Charge	Q <sub>rr</sub>			40		nC

<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

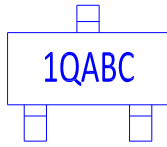






Ordering & Marking Information:

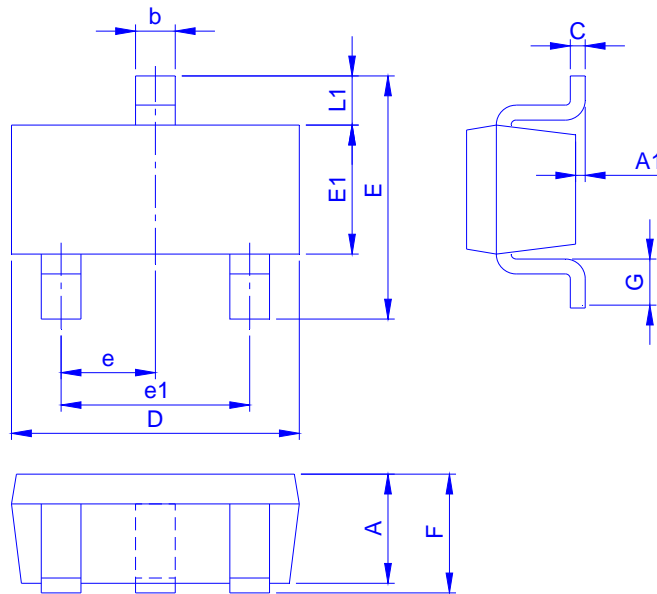
Device Name: EMZBB0N10J for SOT-23



1Q: Device Code, 1Q for EMZBB0N10J

ABC: Date Code

Outline Drawing



Dimension in mm

Dimension	A	A1	A2	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.7	0		0.35	0.1	2.8	2.6	1.5	0.9		0.8	0.3	0.55
Typ.						2.9	2.8	1.6	0.95	1.9			
Max.	1.12	0.1		0.5	0.2	3	3	1.7	1		1.2	0.6	0.65

Footprint

