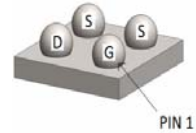
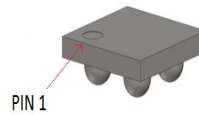
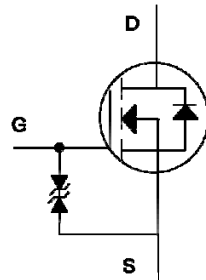


**N-Channel Logic Level Enhancement Mode Field Effect Transistor**

**Product Summary:**

$BV_{DSS}$	30V
$R_{DS(on)}$ (MAX.)	60m $\Omega$
$I_D$	3.2A



Pb-Free Lead Plating & Halogen Free

ESD Protection



**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	3.2	A
	$T_A = 70\text{ }^\circ\text{C}$		2.5	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	12.8	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	1.3	W
	$T_A = 70\text{ }^\circ\text{C}$		0.84	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$		95	$^\circ\text{C} / \text{W}$

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

<sup>3</sup>95 $^\circ\text{C} / \text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	0.4	0.8	1.2	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±12V			±5	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			10	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 4.5V	3.2			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 1A		50	60	mΩ
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 1A		63	80	
		V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 0.5A		82	110	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 1A		7		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz		515		pF
Output Capacitance	C <sub>oss</sub>			90		
Reverse Transfer Capacitance	C <sub>rss</sub>			75		
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 1A		8.5		nC
Gate-Source Charge <sup>1,2</sup>	Q <sub>gs</sub>			1.0		
Gate-Drain Charge <sup>1,2</sup>	Q <sub>gd</sub>			2.7		
Turn-On Delay Time <sup>1,2</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 1A, V <sub>GS</sub> = 4.5V, R <sub>GEN</sub> = 6Ω		23		nS
Rise Time <sup>1,2</sup>	t <sub>r</sub>			12		
Turn-Off Delay Time <sup>1,2</sup>	t <sub>d(off)</sub>			35		
Fall Time <sup>1,2</sup>	t <sub>f</sub>			18		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				3.2	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				12.8	
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = 1A, V <sub>GS</sub> = 0V			1.2	V

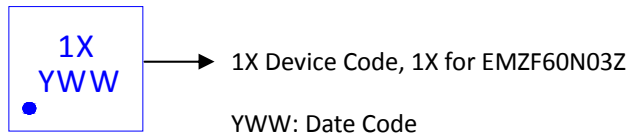
<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

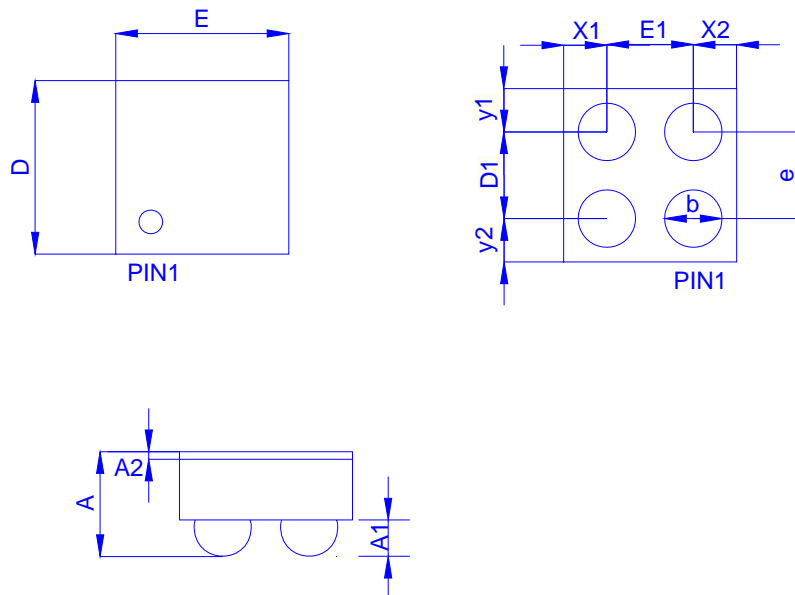
<sup>3</sup>Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMZF60N03Z for WLCSP



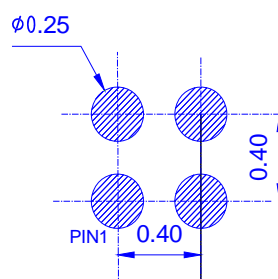
Outline Drawing



Dimension in mm

Dimension	A	A1	A2	D	D1	E	E1	b	e	X1	X2	y1	y2
Min.	0.463	0.168	0.020	0.770	0.400 (BSC)	0.770	0.400 (BSC)	0.265	0.400 (BSC)	0.200 (REF)	0.200 (REF)	0.200 (REF)	0.200 (REF)
Max.	0.503	0.228	0.050	0.830		0.830							

Footprint





TYPICAL CHARACTERISTICS

