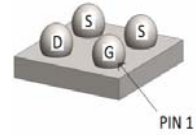
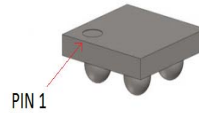
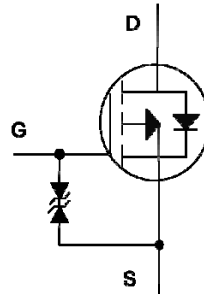


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DS(on) (MAX.)}$	110m Ω
I_D	-2.4A



Pb-Free Lead Plating & Halogen Free

ESD Protection



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	I_D	-2.4	A
	$T_A = 70\text{ }^\circ\text{C}$		-1.8	
Pulsed Drain Current ¹		I_{DM}	-9.6	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	1.3	W
	$T_A = 70\text{ }^\circ\text{C}$		0.84	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient ³	$R_{\theta JA}$		95	$^\circ\text{C} / \text{W}$

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³95 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.4	-0.8	-1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 5	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -4.5V$	-2.4			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -1A$		90	110	m Ω
		$V_{GS} = -3.7V, I_D = -1A$		100	125	
		$V_{GS} = -2.5V, I_D = -0.5A$		115	150	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -1A$		5		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		525		pF
Output Capacitance	C_{oss}			92		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -15V, V_{GS} = -4.5V,$ $I_D = -1A$		8.6		nC
Gate-Source Charge ^{1,2}	Q_{gs}			1.0		
Gate-Drain Charge ^{1,2}	Q_{gd}			2.9		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -4.5V, R_{GEN} = 6\Omega$		25		nS
Rise Time ^{1,2}	t_r			15		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			40		
Fall Time ^{1,2}	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				-2.4	A
Pulsed Current ³	I_{SM}				-9.6	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			-1.2	V

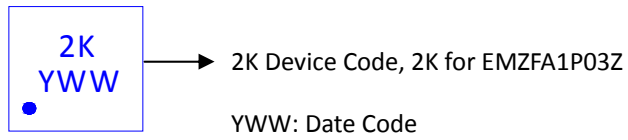
¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

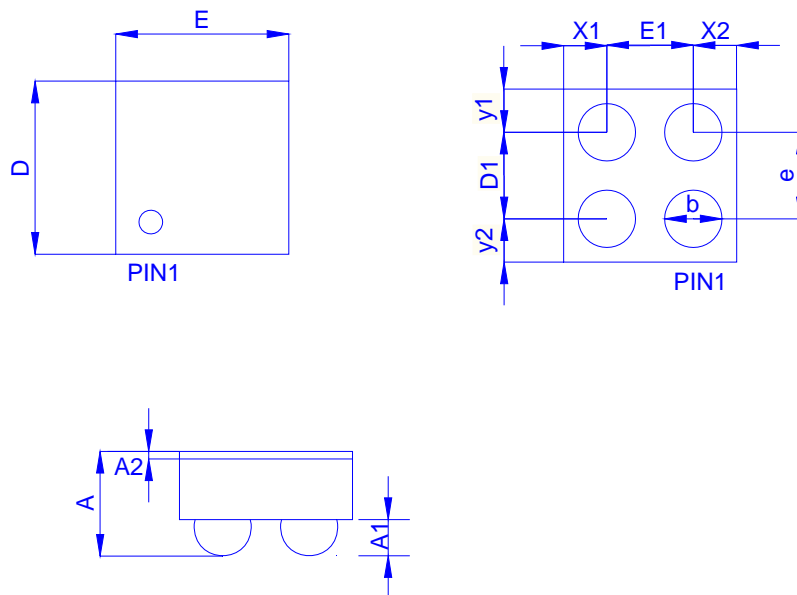
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMZFA1P03Z for WLCSP



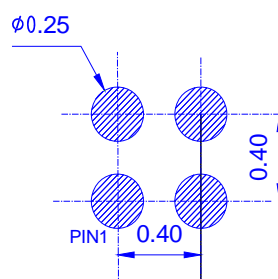
Outline Drawing



Dimension in mm

Dimension	A	A1	A2	D	D1	E	E1	b	e	X1	X2	y1	y2
Min.	0.463	0.168	0.020	0.770	0.400 (BSC)	0.770	0.400 (BSC)	0.265	0.400 (BSC)	0.200 (REF)	0.200 (REF)	0.200 (REF)	0.200 (REF)
Max.	0.503	0.228	0.050	0.830		0.830							

Footprint





TYPICAL CHARACTERISTICS

