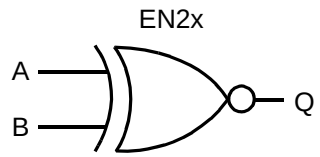
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

EN2x is a family of 2-input gates which perform the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

HDL Syntax

Verilog ..... EN2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EN2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EN21	EN22	EN23	EN24	EN26
A	2.1	4.2	4.2	4.3	4.2
B	2.1	4.2	4.2	4.3	4.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EN21	3.0	TBD	3.9
EN22	5.0	TBD	8.8
EN23	7.0	TBD	12.9
EN24	8.0	TBD	14.6
EN26	8.0	TBD	18.4

a. See page 2-15 for power equation.

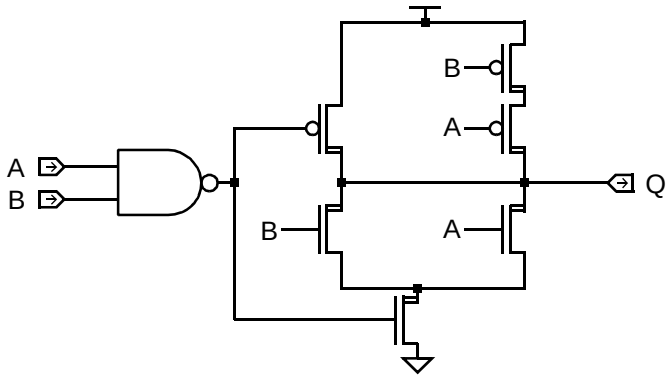
Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

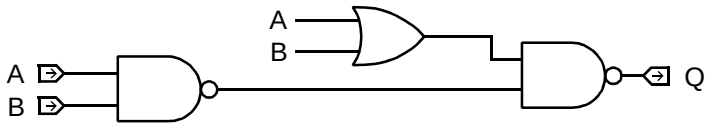
EN21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.29 0.19	0.33 0.25	0.42 0.38	0.51 0.52	0.56 0.62
EN22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.28 0.16	0.33 0.23	0.39 0.32	0.45 0.44	0.51 0.53
EN23	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.26 0.47	0.37 0.61	0.47 0.73	0.57 0.85	0.68 0.99
EN24	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.30 0.51	0.42 0.66	0.54 0.78	0.65 0.89	0.76 1.00
EN26	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.58	0.47 0.76	0.58 0.89	0.67 0.99	0.77 1.09

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Logic Schematic



LOGICAL



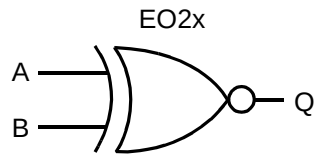
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

EO2x is a family of 2-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

HDL Syntax

Verilog ..... EO2x *inst_name* (Q, A, B);

VHDL..... *inst_name*: EO2x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads				
	EO21	EO22	EO23	EO24	EO26
A	2.1	4.2	4.2	4.2	4.2
B	2.1	4.2	4.3	4.3	4.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO21	3.0	TBD	4.2
EO22	6.0	TBD	9.6
EO23	6.0	TBD	11.3
EO24	7.0	TBD	14.0
EO26	8.0	TBD	17.7

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

EO21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.33 0.18	0.38 0.23	0.54 0.37	0.69 0.52	0.79 0.62
EO22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.29 0.15	0.36 0.23	0.46 0.33	0.58 0.45	0.68 0.53
EO23	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.25 0.42	0.38 0.54	0.49 0.65	0.59 0.76	0.71 0.88
EO24	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.31 0.45	0.41 0.58	0.51 0.70	0.61 0.81	0.71 0.91
EO26	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.35 0.49	0.46 0.62	0.57 0.72	0.67 0.82	0.77 0.93

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Logic Schematic