# EN27LN51208

## 512 Megabit (64 M x 8) SLC, 3.3 V NAND Flash Memory

## 1. Features

- Voltage Supply: 3.3V (2.7V ~ 3.6V )
- Organization
  x 8:
  - Memory Cell Array :
    (64M + 2M) x 8bit
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  x 8:
  - Page Program : (2K + 64) Byte
  - Block Erase : (128K + 4K) Byte
- Page Read Operation
  - Page Size : (2K + 64) Byte (x 8)
  - Random Read : 25µs (Max.)
  - Serial Access : 25ns (Min.)
- Memory Cell: 1bit/Memory Cell
- Fast Write Cycle Time
  - Page Program Time : 300µs (Typ.)
  - Block Erase Time : 3ms (Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - ECC Requirement: x 8 - 4bit/512 Byte
  - Endurance: 100K Program/Erase cycles
  - Data Retention: 10 years
- Command Register Operation
- Automatic Page 0 Read at Power-Up Option
  - Boot from NAND support
  - Automatic Memory Download
- NOP: 4 cycles
- Cache Program Operation for High Performance Program
- Cache Read Operation
- Copy-Back Operation
- EOD mode
- OTP Operation
- Bad-Block-Protect
- Commercial temperature Range

# 2. General Description

The Eon EN27LN51208 is a 64Mx8bit with spare 2Mx8bit capacity. The device is offered in 3.3V Vcc Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 512 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to write the 2,112-Byte page in typical 250us and an erase operation can be performed in typical 2ms on a 128K-Byte for X 8 device block.

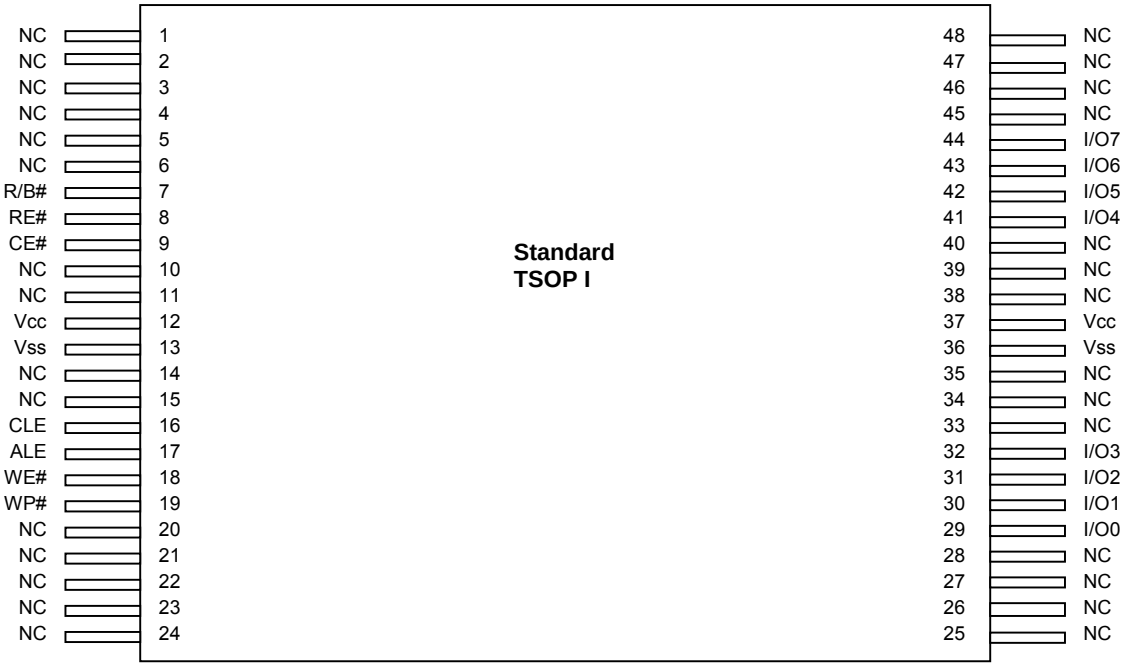
Data in the page mode can be read out at 25ns cycle time per Word. The I/O pins serve as the ports for address and command inputs as well as data input/output. The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array. This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This device includes extra feature: Automatic Read at Power Up.

# 3. Package

## Pin Configuration

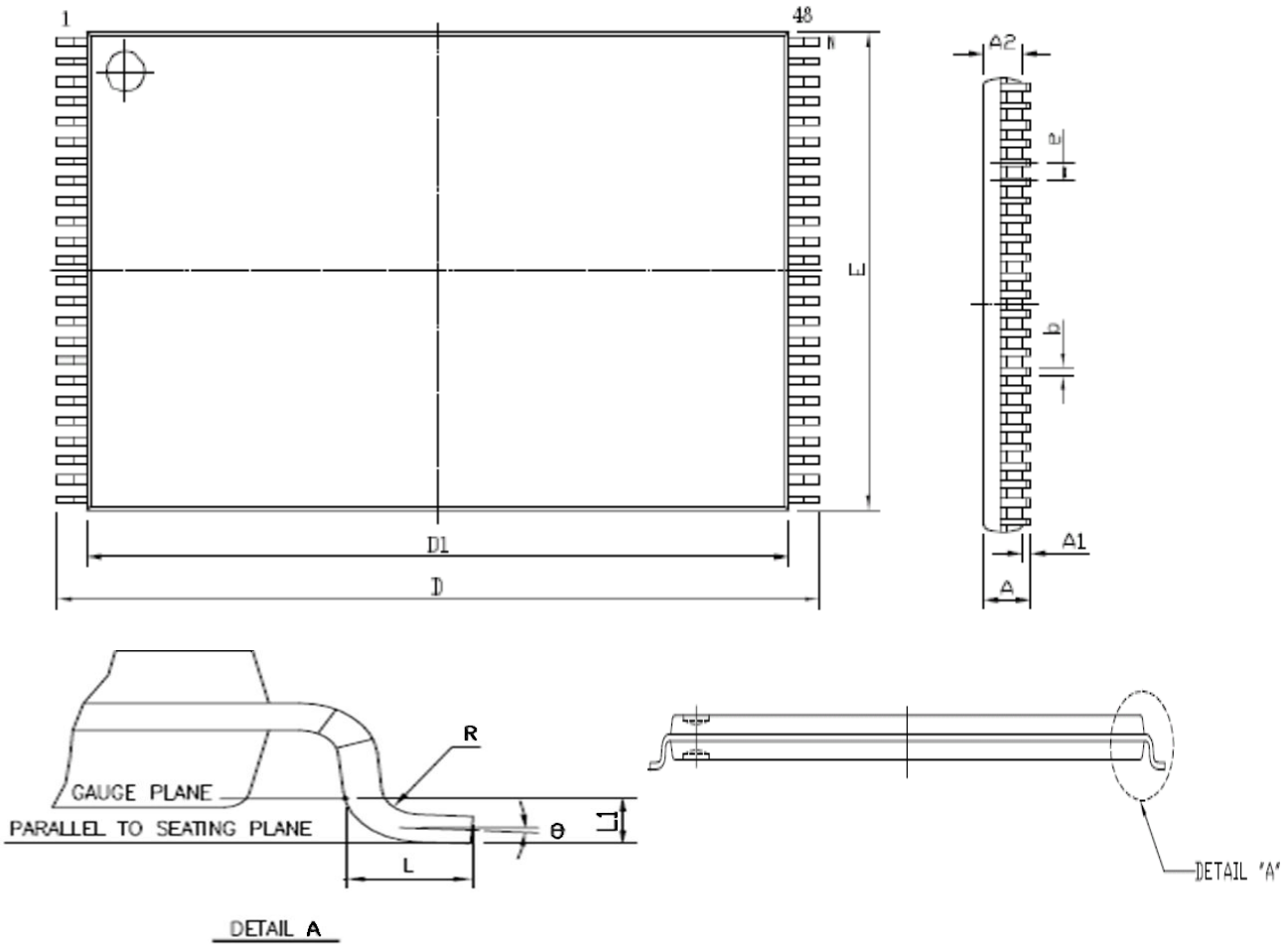
**Figure 1. Pin-Out Diagram of x 8 Device**

**(TOP VIEW)**
(TSOPI 48L, 12mm X 20mm Body, 0.5mm Pin Pitch)



# Package Dimension

**Figure 2. 48L TSOPI 12mm x 20mm package outline**




| SYMBOL | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN. | NOR | MAX |
| A | - - - | - - - | 1.20 |
| A1 | 0.05 | - - - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| D | 19.80 | 20.00 | 20.20 |
| D1 | 18.30 | 18.40 | 18.50 |
| E | 11.9 | 12.00 | 12.10 |
| e | - - - | 0.50 | - - - |
| b | 0.17 | 0.22 | 0.27 |
| L | 0.5 | 0.60 | 0.70 |
| L1 | - - - | 0.25 | - - - |
| R | 0.08 | - - - | 0.20 |
| θ | $0^0$ | $3^0$ | $5^0$ |

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm at the pkg ends, 0.25 mm between leads.

# 4. Pin Description

| Symbol | Pin Name | Function |
|---|---|---|
| I/O0 – I/O7 (x 8) | Data Inputs/Outputs | The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to Hi-Z when the chip is deselected or when the outputs are disabled. |
| CLE | Command Latch Enable | The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE# signal. |
| ALE | Address Latch Enable | The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high. |
| CE# | Chip Enable | The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation. |
| RE# | Read Enable | The RE# input is the serial data-out control, and when it is active low, it drives the data onto the I/O bus. Data is valid $t_{REA}$ after the falling edge of RE# which also increments the internal column address counter by one. |
| WE# | Write Enable | The WE# input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse. |
| WP# | Write Protect | The WP# pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low. |
| R/B# | Ready/Busy Output | The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to Hi-Z condition when the chip is deselected or when outputs are disabled. |
| $V_{CC}$ | Power Supply | $V_{CC}$ is the power supply for device. |
| $V_{SS}$ | Ground | |
| NC | No Connection | Lead is not internally connected. |

**Note:** Connect all $V_{CC}$ and $V_{SS}$ pins of each device to common power supply outputs. Do not leave $V_{CC}$ or $V_{SS}$ disconnected.

# 5. Block Diagram

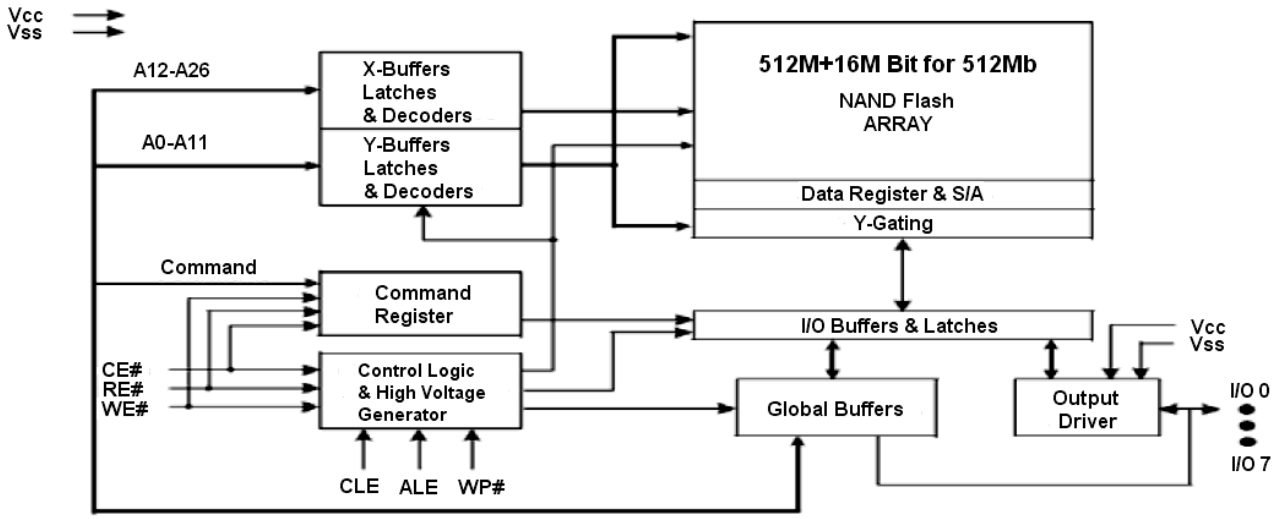



**Figure 3. Functional Block Diagram (x8)**

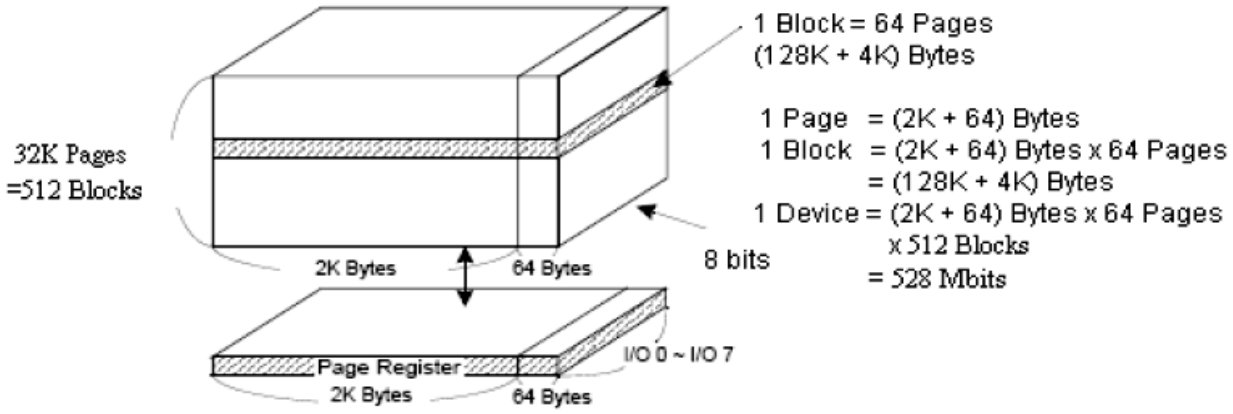



**Figure 4. Array Organization (x8)**

**Table 1. Array Address (x8)**

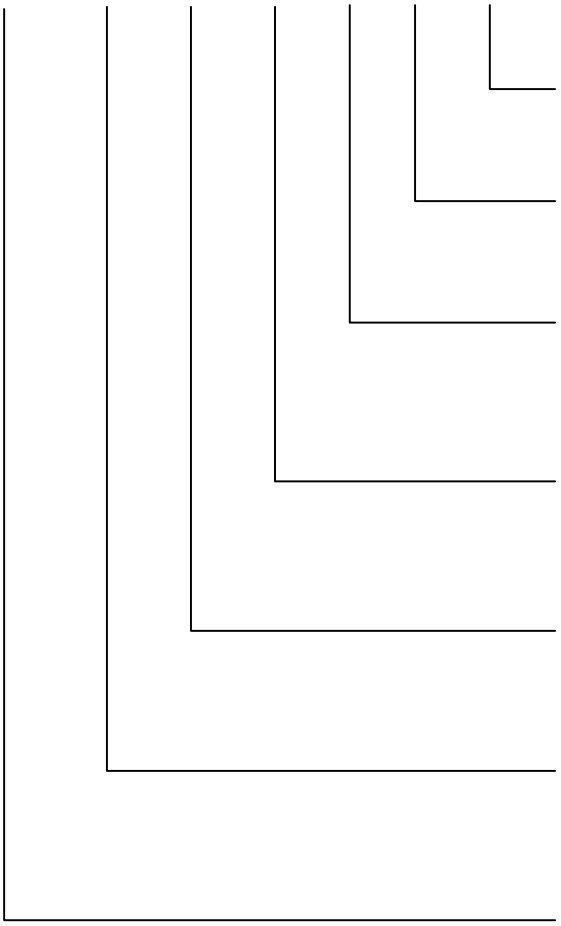
| | I/O 0 | I/O 1 | I/O 2 | I/O 3 | I/O 4 | I/O 5 | I/O 6 | I/O 7 | Address |
|---|---|---|---|---|---|---|---|---|---|
| **1st Cycle** | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | **Column Address** |
| **2nd Cycle** | A8 | A9 | A10 | A11 | L* | L* | L* | L* | **Column Address** |
| **3rd Cycle** | A12 | A13 | A14 | A15 | A16 | A17 | A18 | A19 | **Row Address** |
| **4th Cycle** | A20 | A21 | A22 | A23 | A24 | A25 | A26 | L* | **Page Address** |

**Note:**

1. Column Address : Starting Address of the Register.
2. L* must be set to “Low”.
3. The device ignores any additional input of address cycles than required.

## 6. Ordering Information

EN27LN 512 08 - 25 T C P



**PACKAGING CONTENT**
P = RoHS, Halogen-Free and REACH compliant

**TEMPERATURE RANGE**
C = Commercial (0 to 75℃)

**PACKAGE**
T = 48-pin TSOP

**SPEED OPTION for BURST ACCESS TIME**
25 = 25ns

**Data Length**
08 = 8-bit width

**DENSITY**
512 = 512 Megabit [(64M + 2M) x 8 Bit]

**BASE PART NUMBER**
EN = Eon Silicon Solution Inc.
27LN = 3.0V Operation NAND Flash

# 7. Product Introduction

The EN27LN51208 is a 528Mbit memory organized as 32K rows (pages) by 2,112x8 columns. Spare 64x8 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 4,096 separately erasable 128K-byte blocks. It indicates that the bit-by-bit erase operation is prohibited on the EN27LN51208.

The EN27LN51208 has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Those are latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

**Table 2. Command Set**

| Function | 1st Cycle | 2nd Cycle | Acceptable Command during Busy |
|---|---|---|---|
| Read | 00h | 30h | |
| Read for Copy Back | 00h | 35h | |
| Read ID | 90h | - | |
| Reset | FFh | - | **O** |
| Page Program | 80h | 10h | |
| Copy-Back Program | 85h | 10h | |
| Block Erase | 60h | D0h | |
| Random Data Input (1) | 85h | - | |
| Random Data Output (1) | 05h | E0h | |
| Read Status | 70h | - | **O** |
| Cache Program | 80h | 15h | |
| Cache Read | 31h | - | |
| Read Start For Last Page Cache Read | 3Fh | - | |

**Note:**
1. Random Data Input / Output can be executed in a page.

## 7.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{CC}$ | -0.6 to +4.6 | V |
| | $V_{IN}$ | -0.6 to +4.6 | |
| | $V_{I/O}$ | -0.6 to VCC + 0.3 (< 4.6) | |
| Temperature Under Bias | $T_{BIAS}$ | -40 to +125 | ℃ |
| Storage Temperature | $T_{STG}$ | -65 to +150 | ℃ |
| Short Circuit Current | $I_{OS}$ | 5 | mA |

**Note:**

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 7.2 Recommended Operating Conditions

(Voltage reference to GND, $T_A$ = 0 to 75℃)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2.7 | 3.3 | 3.6 | V |
| Supply Voltage | $V_{SS}$ | 0 | 0 | 0 | V |

## 7.3 DC and Operation Characteristics

(Recommended operating conditions otherwise noted)

| Parameter | | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating Current | Page Read with Serial Access | $I_{CC1}$ | $t_{RC}$=25ns, CE# =$V_{IL}$, $I_{OUT}$=0mA | - | 15 | 30 | mA |
| | Program | $I_{CC2}$ | - | - | 15 | 30 | |
| | Erase | $I_{CC3}$ | - | - | 15 | 30 | |
| Stand-by Current (TTL) | | $I_{SB1}$ | CE# =$V_{IH}$, WP# =0V/$V_{CC}$ | - | - | 1 | mA |
| Stand-by Current (CMOS) | | $I_{SB2}$ | CE# = $V_{CC}$ -0.2, WP# =0V/ $V_{CC}$ | - | 10 | 50 | uA |
| Input Leakage Current | | $I_{LI}$ | $V_{IN}$=0 to $V_{CC}$ (max) | - | - | ±10 | uA |
| Output Leakage Current | | $I_{LO}$ | $V_{OUT}$=0 to $V_{CC}$ (max) | - | - | ±10 | uA |
| Input High Voltage | | $V_{IH}$ (1) | - | 0.8 x $V_{CC}$ | - | $V_{CC}$ +0.3 | V |
| Input Low Voltage, All inputs | | $V_{IL}$ (1) | - | -0.3 | - | 0.2 x $V_{CC}$ | V |
| Output High Voltage Level | | $V_{OH}$ | $I_{OH}$=-400uA | 2.4 | - | - | V |
| Output Low Voltage Level | | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.4 | V |
| Output Low Current (R/B#) | | $I_{OL}$ (R /B#) | $V_{OL}$=0.4V | 8 | 10 | - | mA |

**Note:**

1. $V_{IL}$ can undershoot to -0.4V and $V_{IH}$ can overshoot to $V_{CC}$+0.4V for durations of 20ns or less.
2. Typical value are measured at $V_{CC}$ =3.3V, $T_A$ = 25℃. And not 100% tested.

## 7.4 VALID BLOCK

| Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $N_{VB}$ | 502 | - | 512 | Blocks |

**Note:**
1. The device may include initial invalid blocks when first shipped. The number of valid blocks is presented as first shipped. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 4bit/512Byte ECC.

## 7.5 AC TEST CONDITION

($T_A$ = 0 to 70°C, $V_{CC}$=2.7V~3.6V, unless otherwise noted)

| Parameter | Condition |
|---|---|
| Input Pulse Levels | 0V to $V_{CC}$ |
| Input Rise and Fall Times | 5 ns |
| Input and Output Timing Levels | $V_{CC}$ /2 |
| Output Load (1) | 1 TTL Gate and $C_L$=50pF |

**Note:**
1. Refer to 11.10 Ready/Busy#, R/B# output's Busy to Ready time is decided by the pull-up resistor (Rp) tied to the R/B# pin.

## 7.6 CAPACITANCE

($T_A$ = 25°C, $V_{CC}$=3.3V, f =1.0MHz)

| Item | Symbol | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Input / Output Capacitance | $C_{I/O}$ | $V_{IL}$ = 0V | - | 8 | pF |
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0V | - | 8 | pF |

**Note:** Capacitance is periodically sampled and not 100% tested.

## 7.7 MODE SELECTION

| CLE | ALE | CE# | WE# | RE# | WP# | Mode | |
|---|---|---|---|---|---|---|---|
| H | L | L | Rising | H | X | Read Mode | Command Input |
| L | H | L | Rising | H | X | | Address Input (5 clock) |
| H | L | L | Rising | H | H | Write Mode | Command Input |
| L | H | L | Rising | H | H | | Address Input (5 clock) |
| L | L | L | Rising | H | H | Data Input | |
| L | L | L | H | Falling | X | Data Output | |
| X | X | X | X | H | X | During Read (Busy) | |
| X | X | X | X | X | H | During Program (Busy) | |
| X | X | X | X | X | H | During Erase (Busy) | |
| X | X (1) | X | X | X | L | Write Protect | |
| X | X | H | X | X | 0V/$V_{CC}$ (2) | Stand-by | |

**Note:**
1. X can be $V_{IL}$ or $V_{IH}$.
2. WP# should be biased to CMOS high or CMOS low for stand-by.

## 7.8 Program / Erase Characteristics

($T_A$=0 to 75℃, Vcc=2.7V ~ 3.6V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Average Program Time | $t_{PROG}$ | - | 300 | 750 | us |
| Dummy Busy Time for Cache Program | $t_{CBSY}$ | - | 3 | 750 | us |
| Number of Partial Program Cycles in the Same Page | $N_{OP}$ | - | - | 4 | cycle |
| Block Erase Time | $t_{BERS}$ | - | 3 | 10 | ms |
| Dummy Busy Time for Two-Plane Page Program | $T_{DBSY}$ | - | 0.5 | 1 | us |

**Note:**
1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V $V_{CC}$ and 25°C temperature.
2. **tPROG is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.**
3. Max. time of $t_{CBSY}$ depends on timing between internal program completion and data in.

## 7.9 AC Timing Characteristics for Command / Address / Data Input

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| CLE Setup Time | $t_{CLS}$ (1) | 12 | - | ns |
| CLE Hold Time | $t_{CLH}$ | 5 | - | ns |
| CE# Setup Time | $t_{CS}$ (1) | 20 | - | ns |
| CE# Hold Time | $t_{CH}$ | 5 | - | ns |
| WE# Pulse Width | $t_{WP}$ | 12 | - | ns |
| ALE Setup Time | $t_{ALS}$ (1) | 12 | - | ns |
| ALE Hold Time | $t_{ALH}$ | 5 | - | ns |
| Data Setup Time | $t_{DS}$ (1) | 12 | - | ns |
| Data Hold Time | $t_{DH}$ | 5 | - | ns |
| Write Cycle Time | $t_{WC}$ | 25 | - | ns |
| WE# High Hold Time | $t_{WH}$ | 10 | - | ns |
| ALE to Data Loading Time | $t_{ADL}$ (2) | 100 | - | ns |

**Note:**
1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. $t_{ADL}$ is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

## 7.10 AC Characteristics for Operation

| Parameter | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Data Transfer from Cell to Register | | $t_R$ | - | 25 | us |
| ALE to RE# Delay | | $t_{AR}$ | 10 | - | ns |
| CLE to RE# Delay | | $t_{CLR}$ | 10 | - | ns |
| Ready to RE# Low | | $t_{RR}$ | 20 | - | ns |
| RE# Pulse Width | | $t_{RP}$ | 12 | - | ns |
| WE# High to Busy | | $t_{WB}$ | - | 100 | ns |
| WP# Low to WE# Low (disable mode) | | $t_{WW}$ | 100 | - | ns |
| WP# High to WE# Low (enable mode) | | | | | |
| Read Cycle Time | | $t_{RC}$ | 25 | - | ns |
| RE# Access Time | | $t_{REA}$ | - | 20 | ns |
| CE# Access Time | | $t_{CEA}$ | - | 25 | ns |
| RE# High to Output Hi-Z | | $t_{RHZ}$ | - | 100 | ns |
| CE# High to Output Hi-Z | | $t_{CHZ}$ | - | 30 | ns |
| CE# High to ALE or CLE Don't Care | | $t_{CSD}$ | 0 | - | ns |
| RE# High to Output Hold | | $t_{RHOH}$ | 15 | - | ns |
| RE# Low to Output Hold | | $t_{RLOH}$ | 5 | - | ns |
| CE# High to Output Hold | | $t_{COH}$ | 15 | - | ns |
| RE# High Hold Time | | $t_{REH}$ | 10 | - | ns |
| Output Hi-Z to RE# Low | | $t_{IR}$ | 0 | - | ns |
| RE# High to WE# Low | | $t_{RHW}$ | 100 | - | ns |
| WE# High to RE# Low | | $t_{WHR}$ | 60 | - | ns |
| Device Resetting Time during ... | Read | $t_{RST}$ | - | 5 | us |
| | Program | | - | 10 | us |
| | Erase | | - | 500 | us |
| | Ready | | - | 5 (1) | us |
| Cache Busy in Read Cache (following 31h and 3Fh) | | $T_{DCBSYR}$ | - | 30 | us |

**Note:**
If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

# 8. NAND Flash Technical Notes

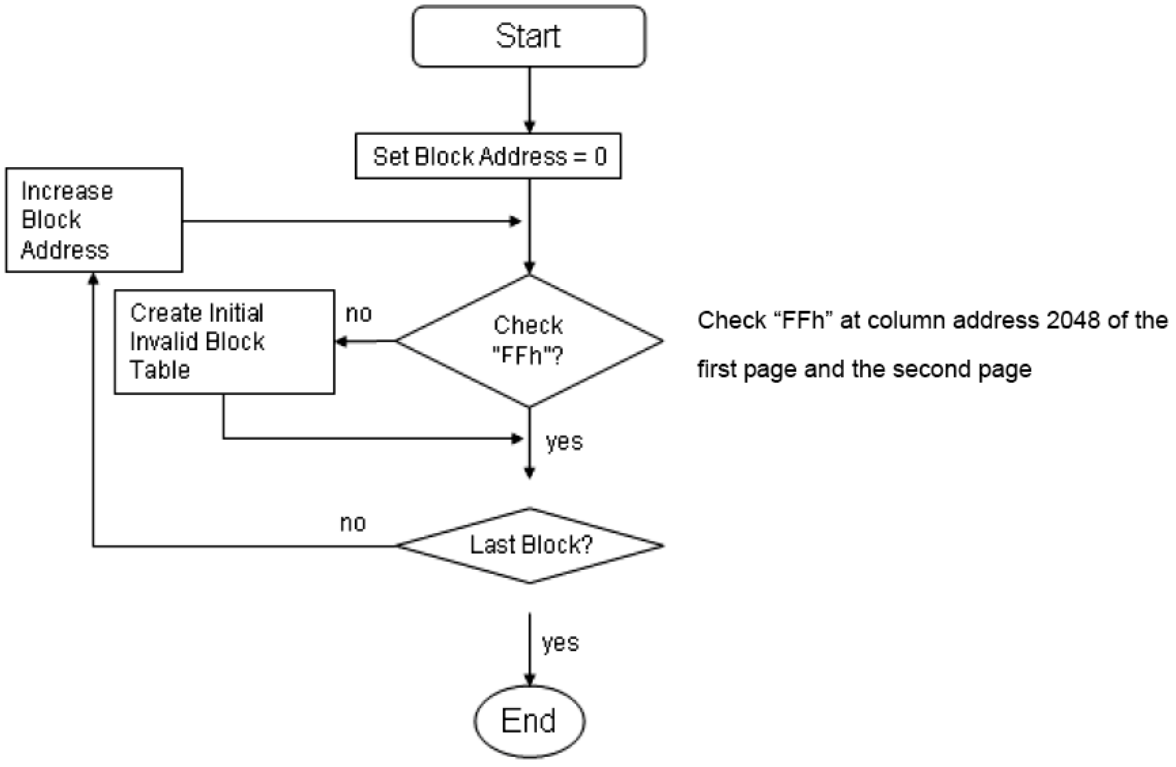
## 8.1 Mask Out Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Eon. The information regarding the initial invalid block(s) is called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1 bit/528 bytes ECC.

## 8.2 Identifying Initial Invalid Block(s) and Block Replacement Management

Unpredictable behavior may result from programming or erasing the defective blocks. Figure 5 illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.
A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address of 2048. If the read data is not FFh, the block is interpreted as an invalid block. Do not erase or program factory-marked bad blocks. The host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.



```
For (i=0; i<Num_of_LUs; i++)
{
    For (j=0; j<Blocks_Per_LU; j++)
    {
        Defect_Block_Found=False;

        Read_Page(lu=i, block=j, page=0);
        If (Data[coloumn=0]!=FFh)   Defect_Block_Found=True;
        If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

        Read_Page(lu=i, block=j, page=1);
        If (Data[coloumn=0]!=FFh)   Defect_Block_Found=True;
        If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

        If (Defect_Block_Found)   Mark_Block_as_Defective(lu=i, block=j);
    }

}
```

**Figure 5. Algorithm for Bad Block Scanning**

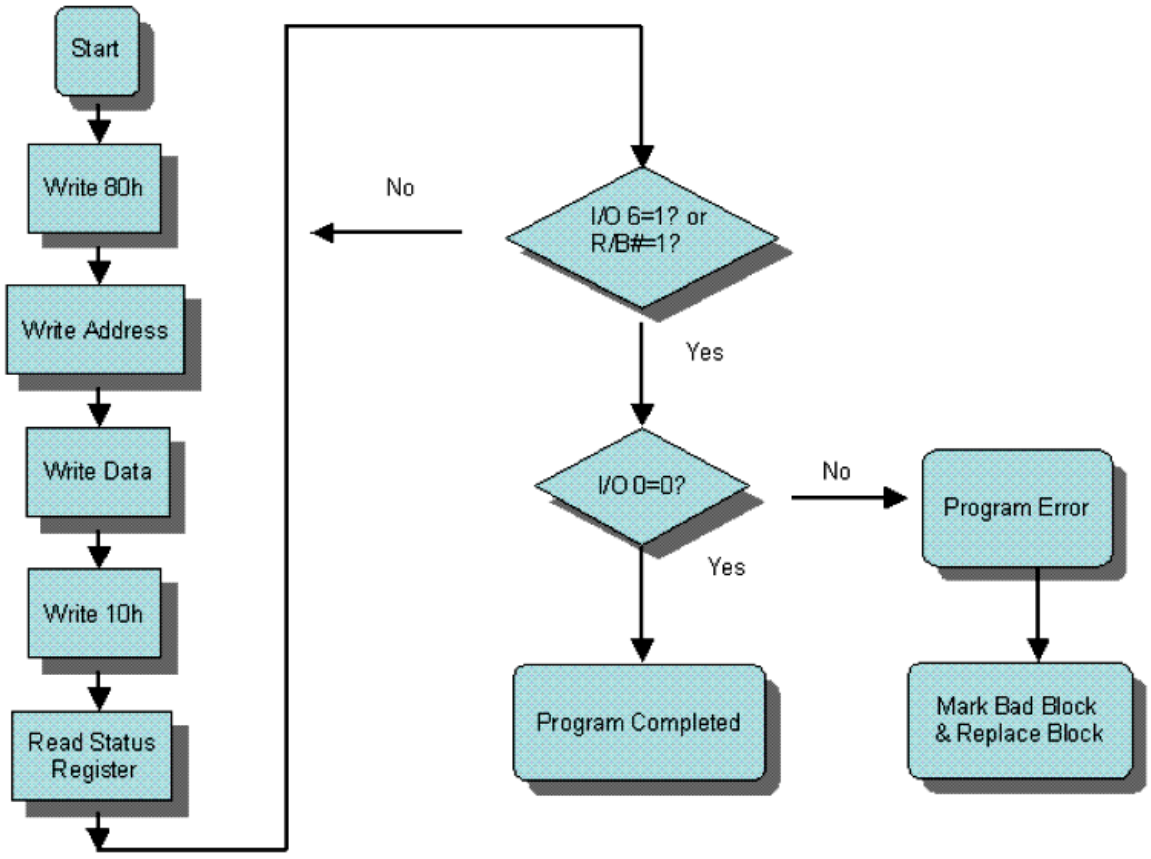
## 8.3 Error in Write or Read Operation

Within its lifetime, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

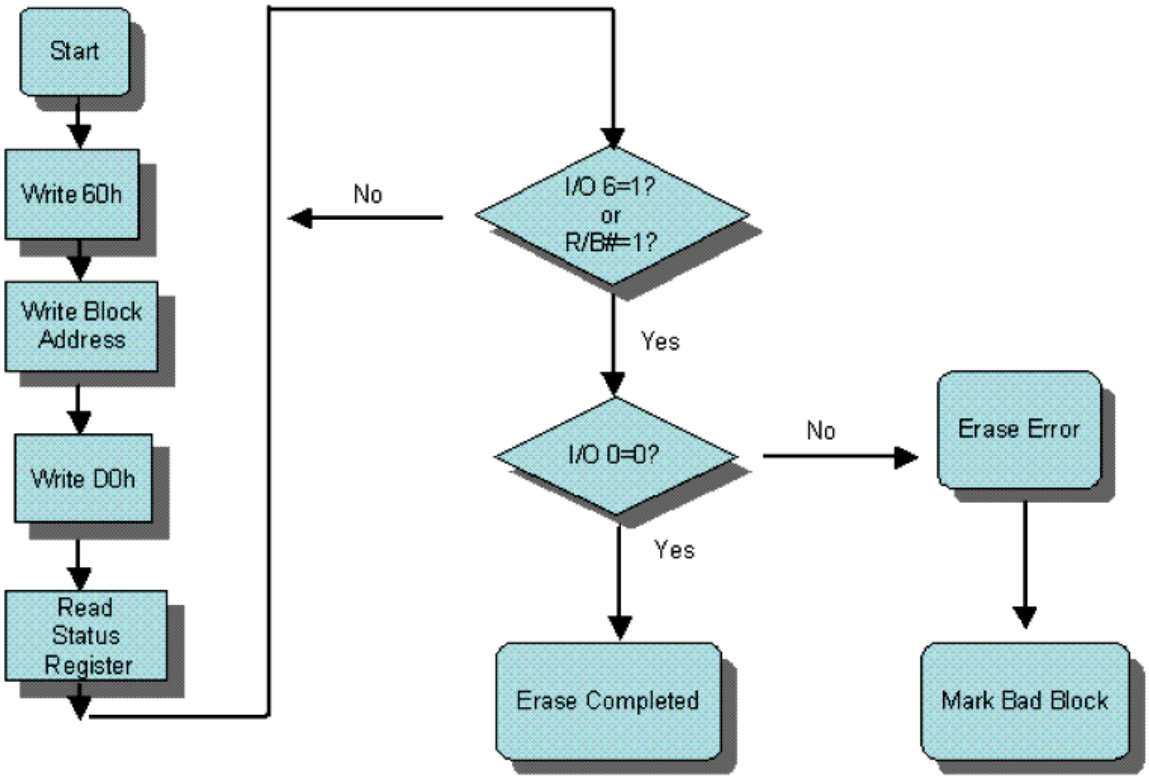
| Failure | | Detection and Countermeasure sequence |
|---|---|---|
| Write | Erase failure | Read Status after Erase → Block Replacement |
| | Program failure | Read Status after Program → Block Replacement |
| Read | Up to 4 bits failure | Verify ECC → ECC Correction |

**Note:**
Error Correcting Code → RS Code or BCH Code etc.
Example: 4bit correction / 512 Byte

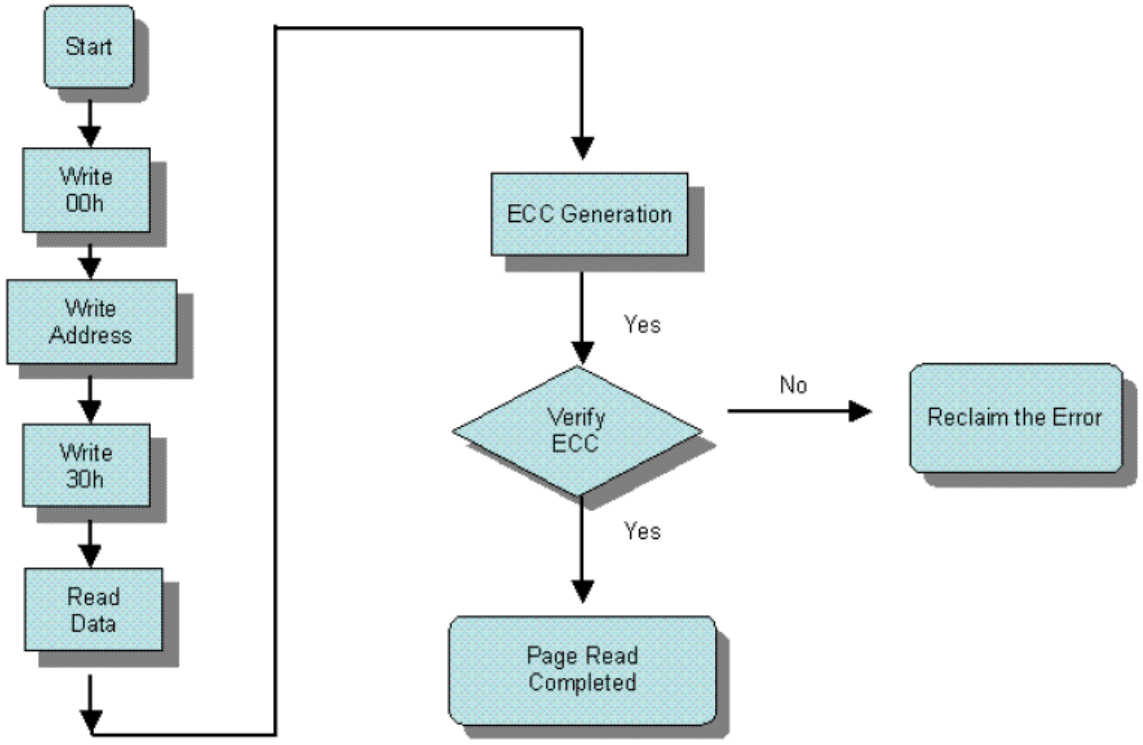
## Program Flow Chart



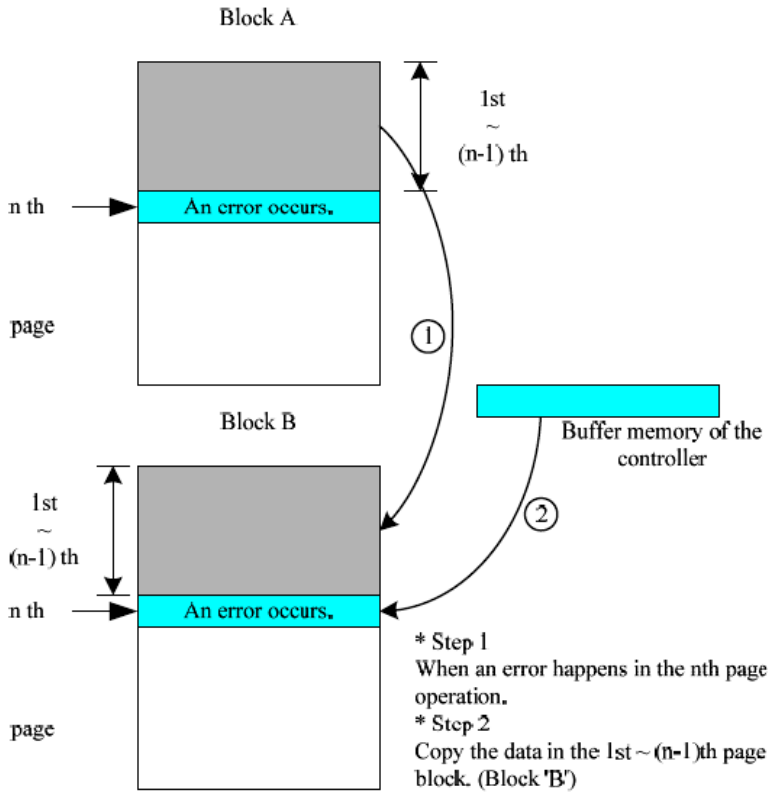
## Erase Flow Chart




## Read Flow Chart



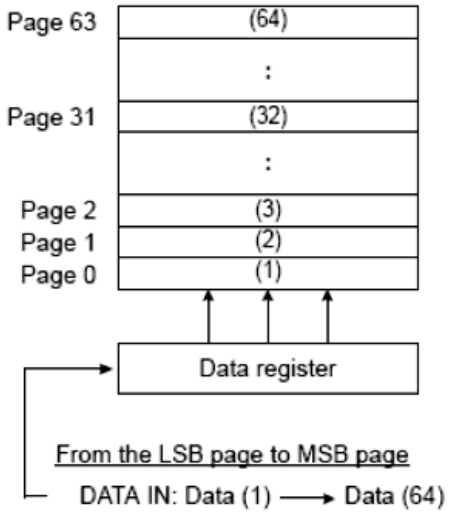
## Block Replacement

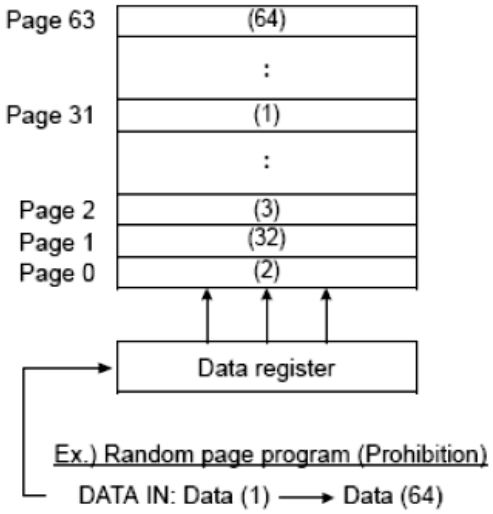



* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

## 8.4 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.




## 8.5 System Interface Using CE# Don't Care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications that use slow cycle time on the order of µ-seconds, de-activating CE# during the data-loading and serial access would provide significant savings in power consumption.

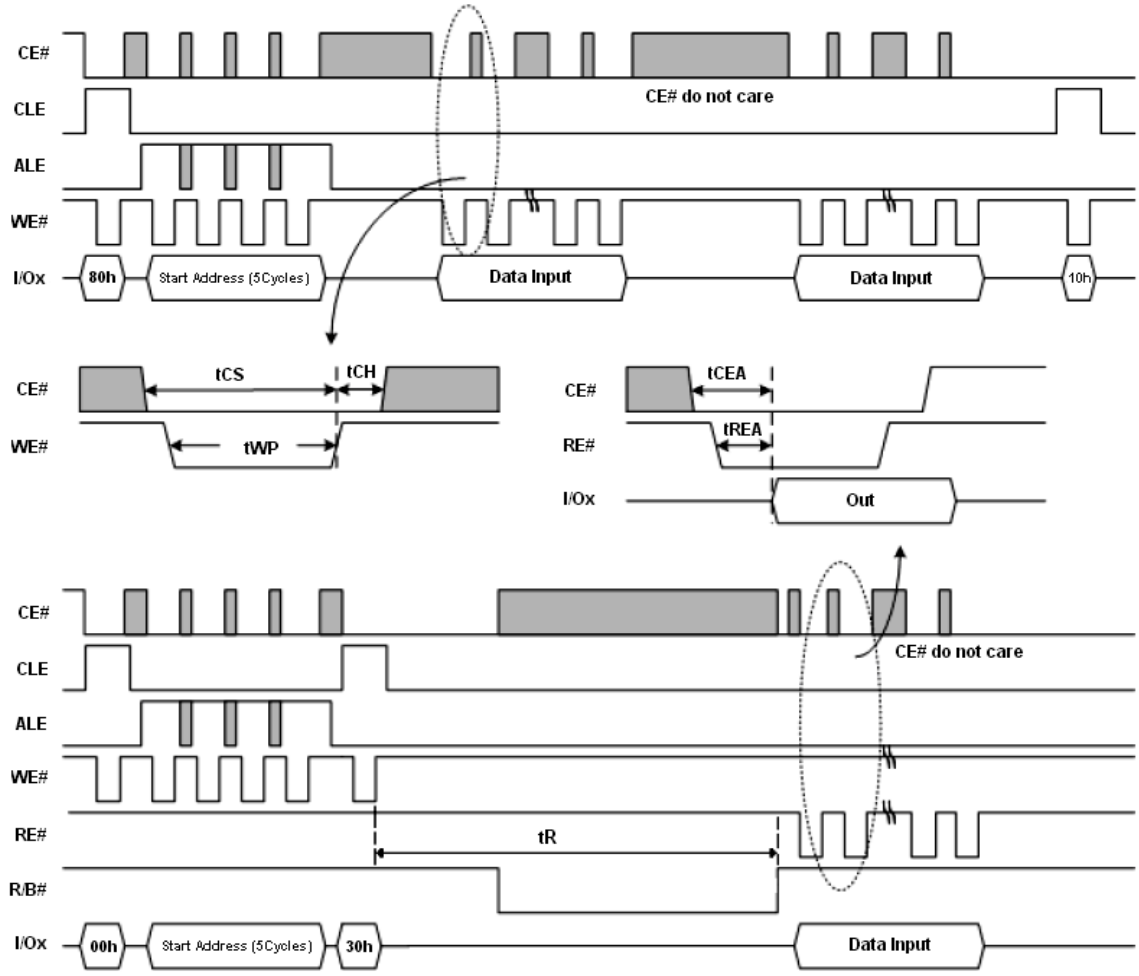



**Figure 6. Program/Read Operation with "CE# not-care"**

### Address Information

| I/O | DATA | ADDRESS | | | |
|---|---|---|---|---|---|
| I/Ox | Data In / Out | Col. Add1 | Col. Add2 | Row Add1 | Row Add2 |
| I/O0~7 | ~ 2112 bytes | A0 ~ A7 | A8 ~ A11 | A12 ~ A19 | A20 ~ A26 |

# 9. Timing Diagrams

## 9.1 Command Latch Cycle

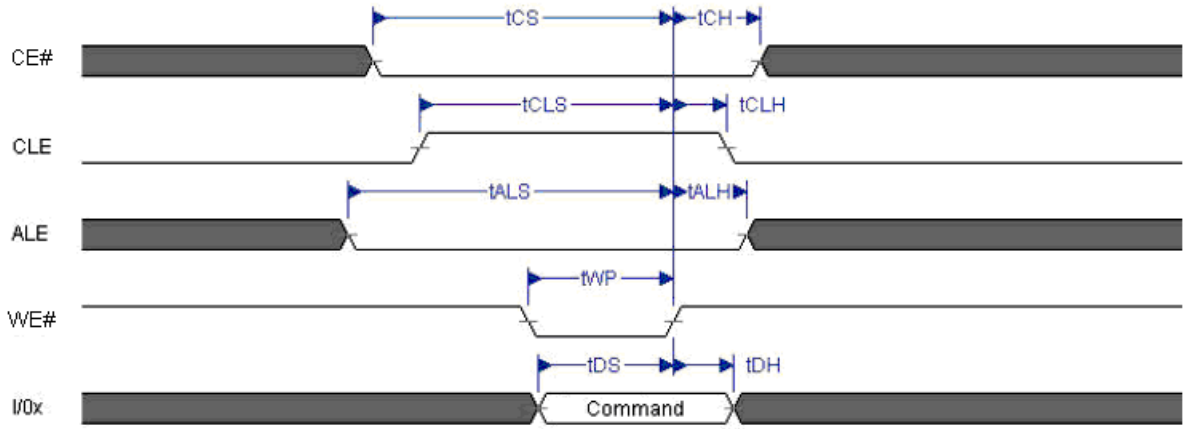



**Figure 7. Command Latch Cycle**

## 9.2 Address Latch Cycle

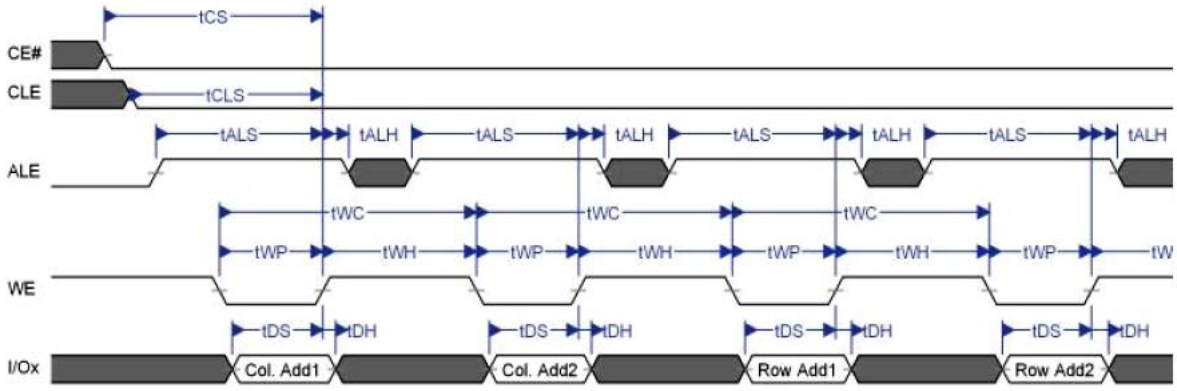



**Figure 8 Address Latch Cycle**

## 9.3 Input Data Latch Cycle

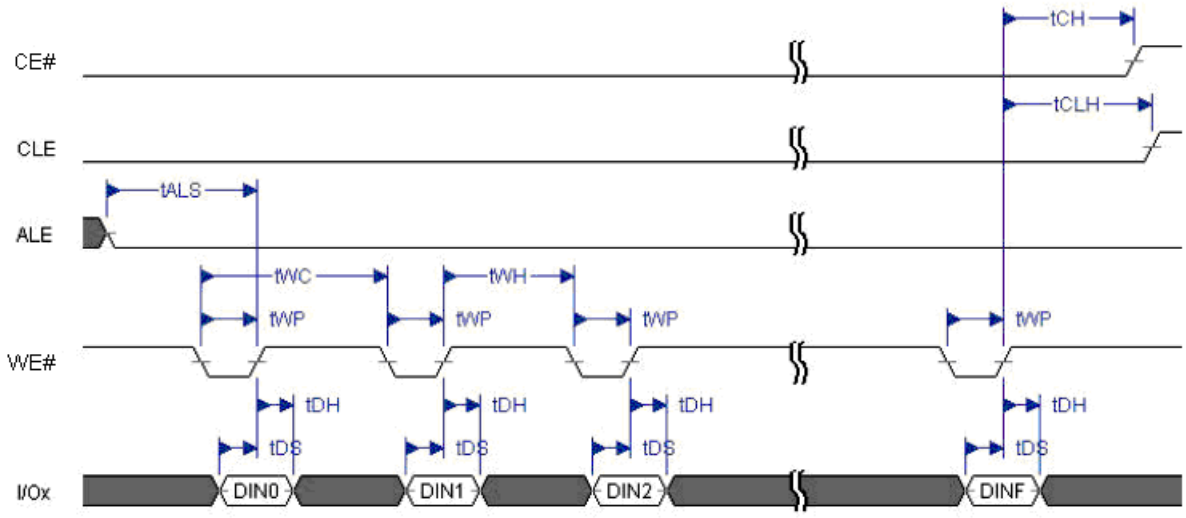



**Figure 9 Input Data Latch Cycle**

## 9.4 Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

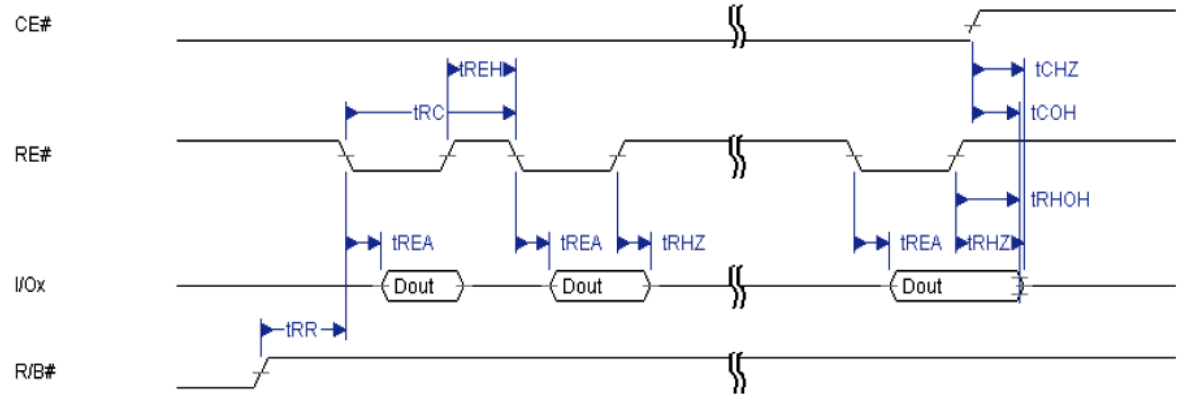



**Figure 10. Sequential Out Cycle after Read**

**Note:**

1. Dout transition is measured at ±200mV from steady state voltage at I/O with load.
2. $t_{RHOH}$ starts to be valid when frequency is lower than 33MHz.

## 9.5 Serial Access Cycle after Read (EDO Type CLE=L, WE#=H, ALE=L)

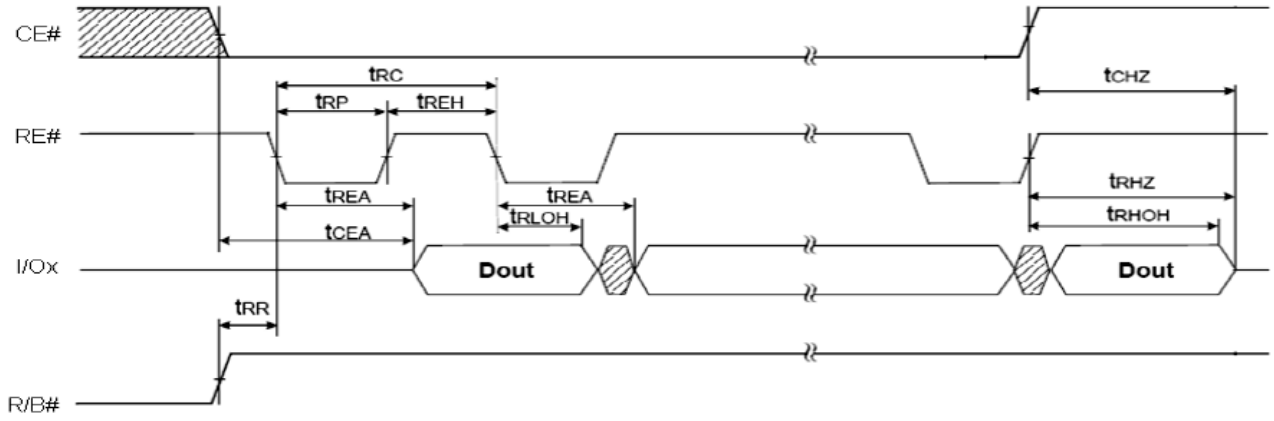



**Figure 11. Sequential Out Cycle after Read (EDO Type CLE=L, WE#=H, ALE=L)**

**Note:**
1. Transition is measured at ±200mV from steady state voltage with load.
   This parameter is sampled and not 100% tested. ($t_{CHZ}$, $t_{RHZ}$)
2. $t_{RLOH}$ is valid when frequency is higher than 33MHz.
   $t_{RHOH}$ starts to be valid when frequency is lower than 33MHz.

## 9.6 Status Read Cycle

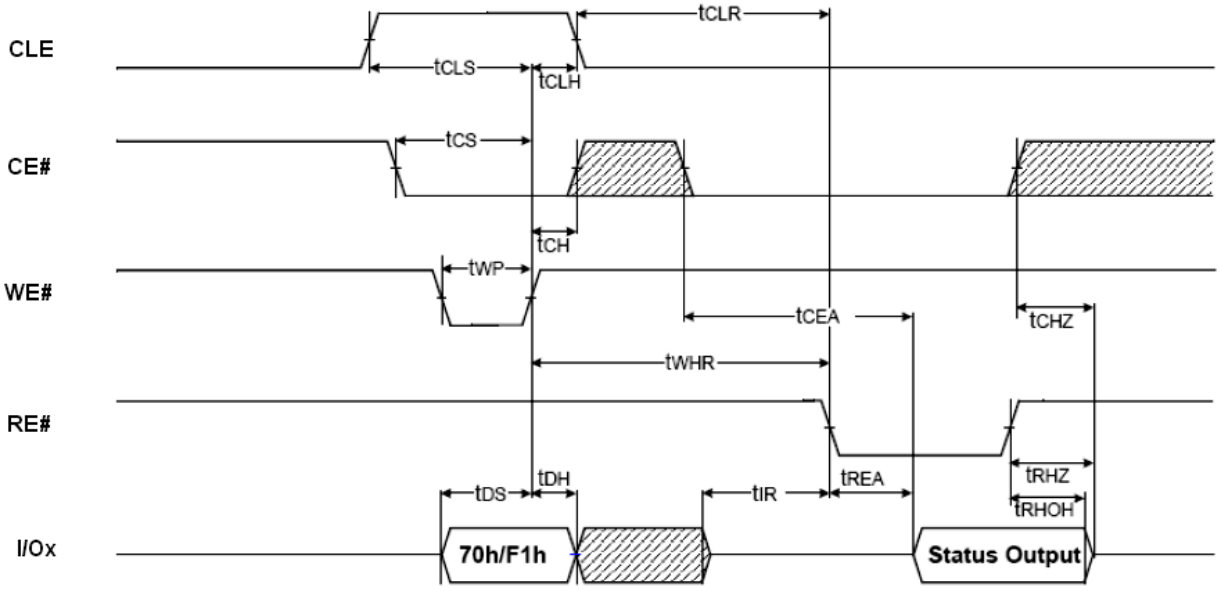



**Figure 12. Status Read Cycle**

## 9.7 Read Operation

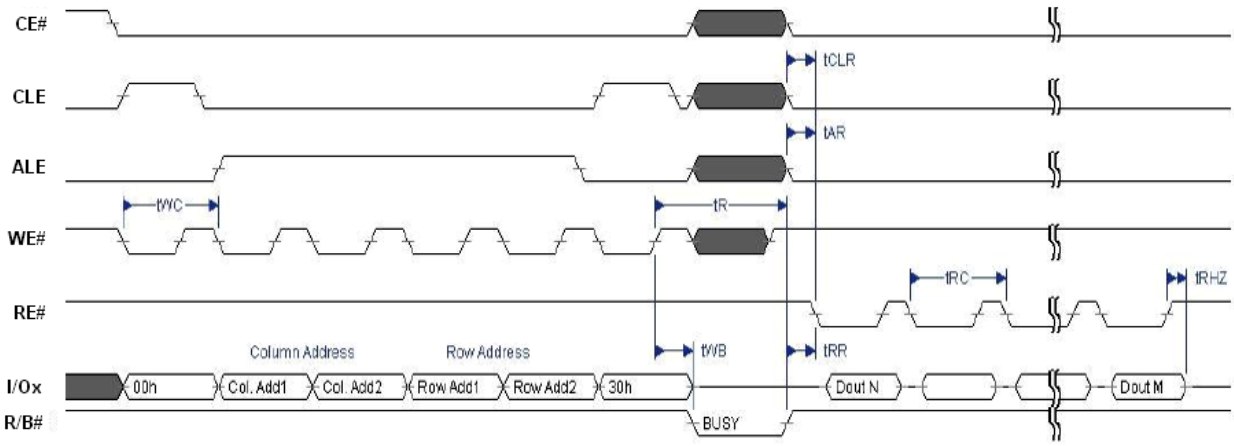



**Figure 13. Read Operation (Read One Page)**

## 9.8 Read Operation (Intercepted by CE#)

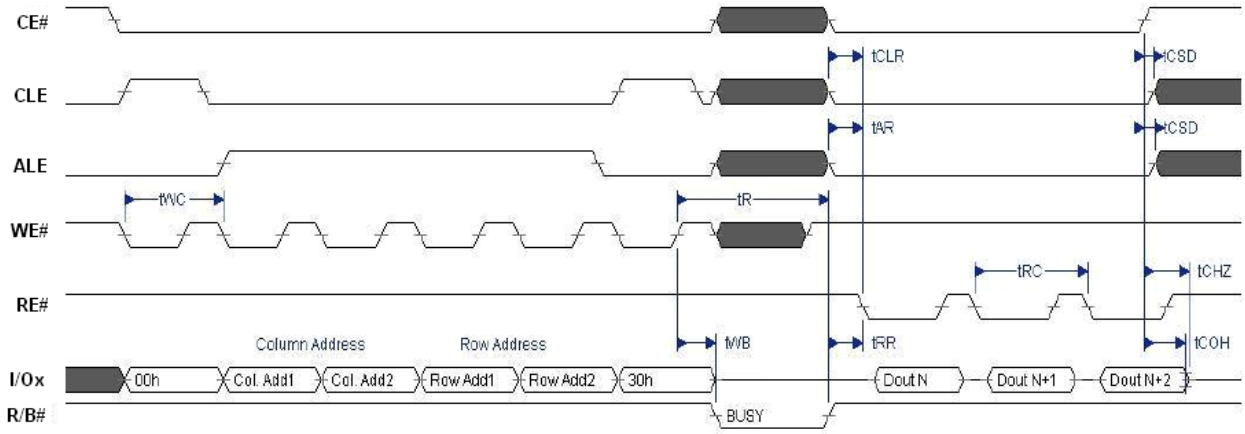



**Figure 14. Read Operation Intercepted by CE#**

## 9.9 Random Data Output In a Page

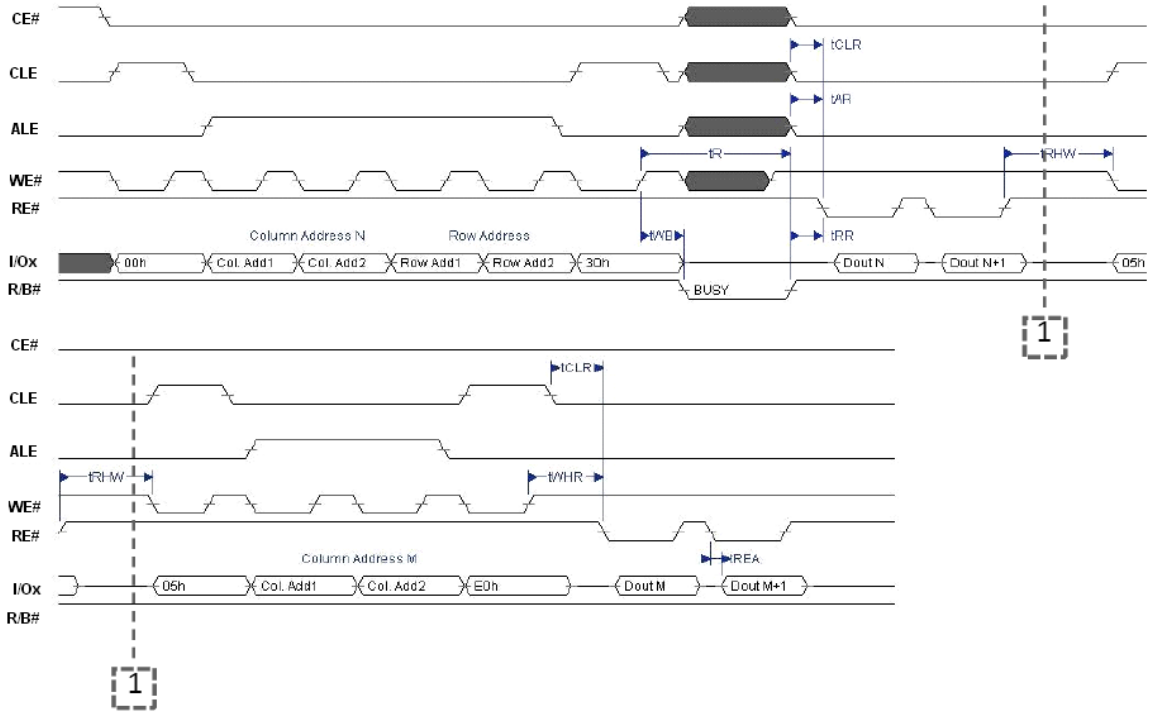



**Figure 15. Random Data Output**

## 9.10 Page Program Operation

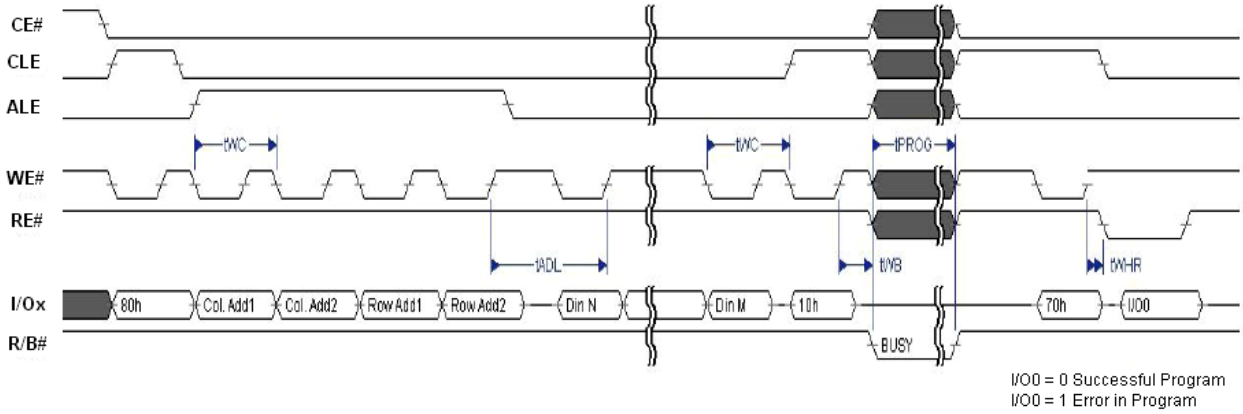



**Figure 16. Page Program Operation**

## 9.11 Page Program Operation with Random Data Input

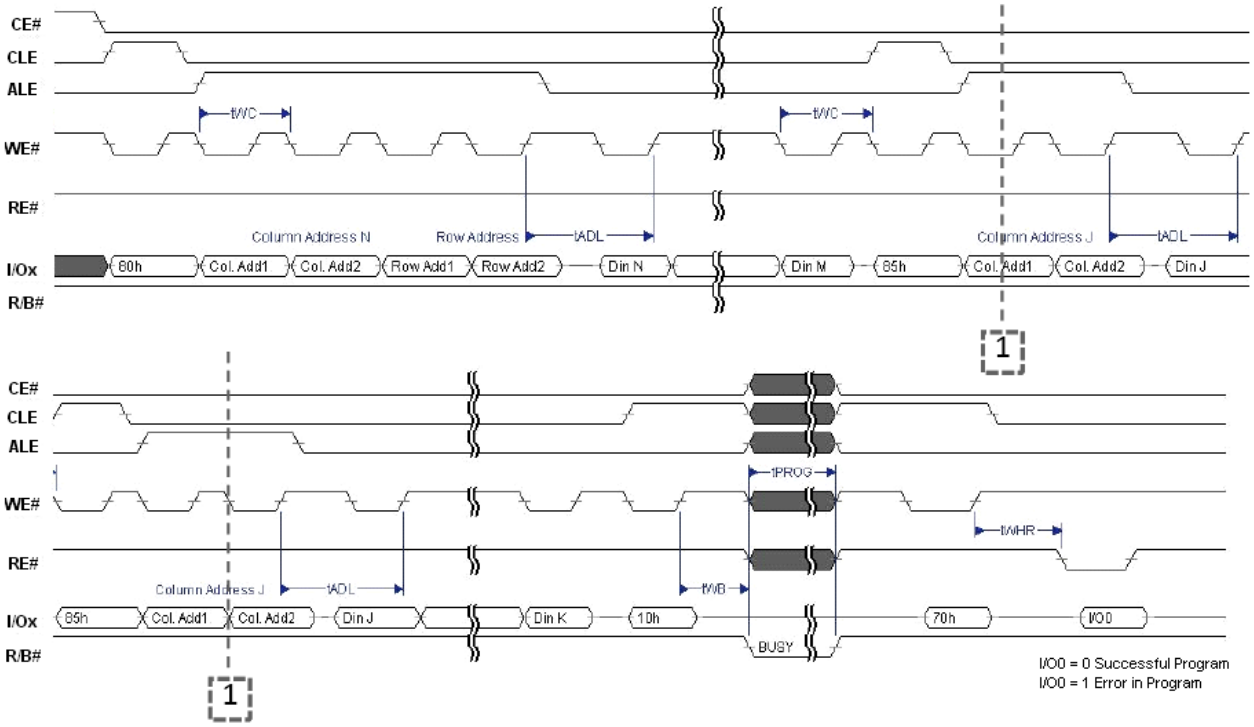



**Figure 17. Random Data Input**

**Note:** $t_{ADL}$ is the time from WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

## 9.12 Copy-Back Program Operation with Random Data Input

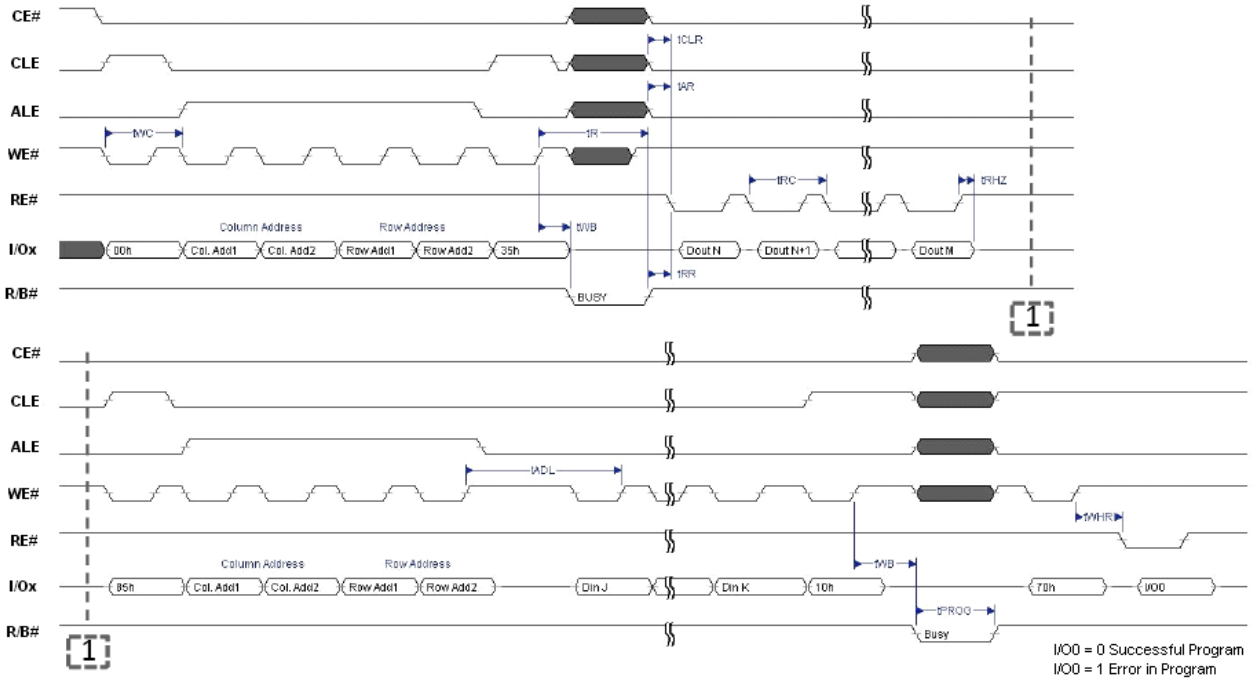



**Figure 18. Copy-Back Operation with Random Data Input**

## 9.13 Cache Program Operation

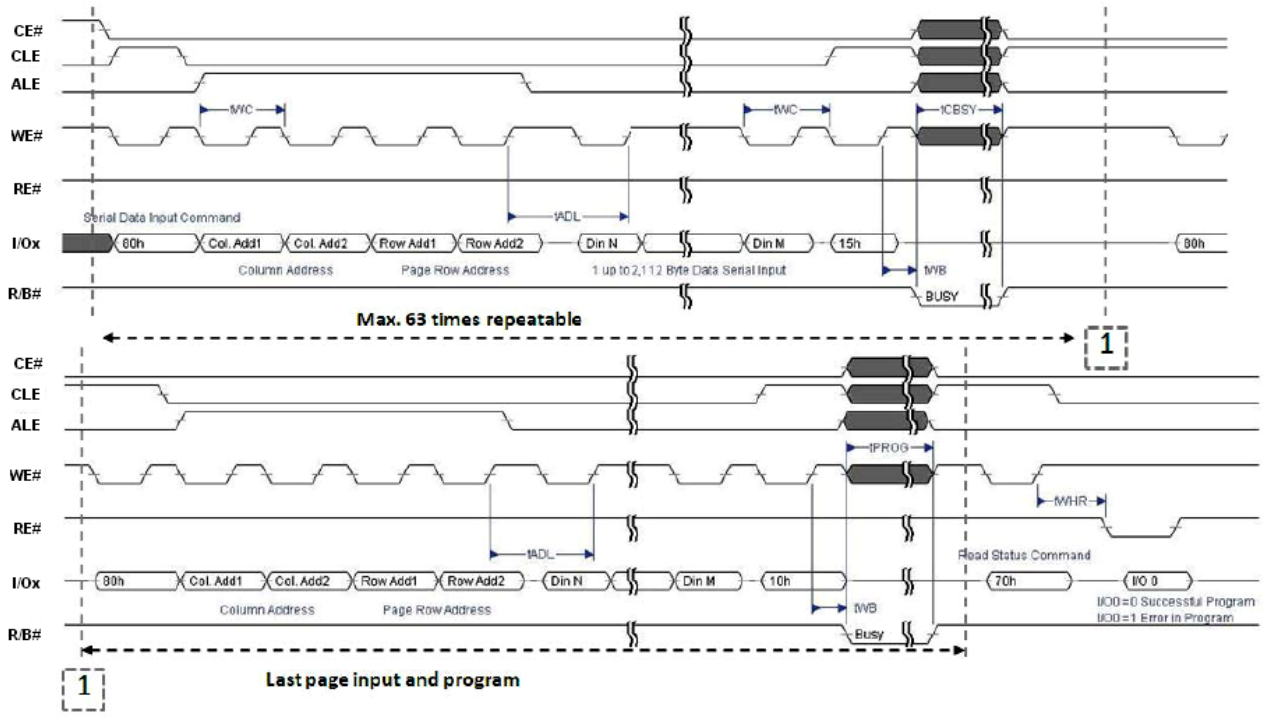



**Figure 19. Cache Program Operation**

## 9.14 Cache Read Operation

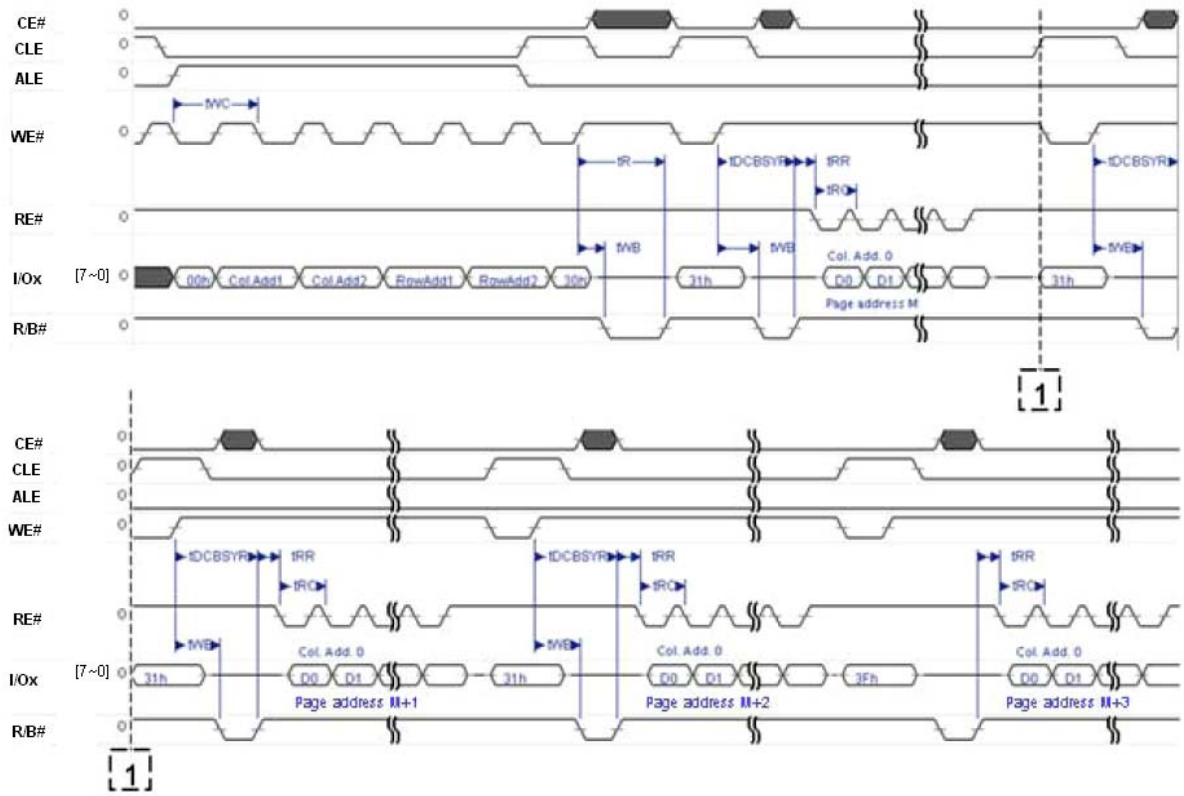



**Figure 20. Cache Read Operation**

## 9.15 Block Erase Operation (Erase One Block)

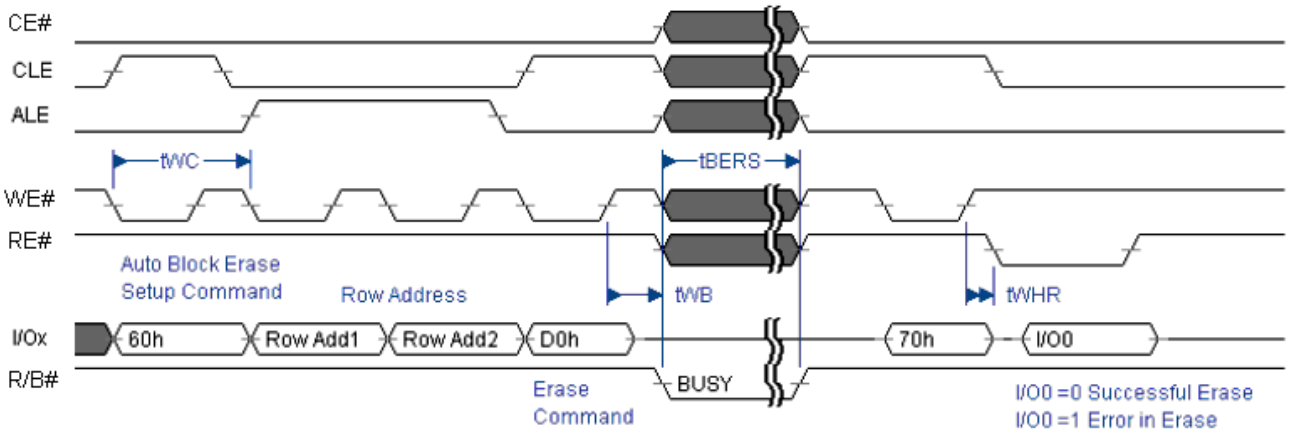



**Figure 21. Block Erase Operation**

## 9.16 Read ID Operation

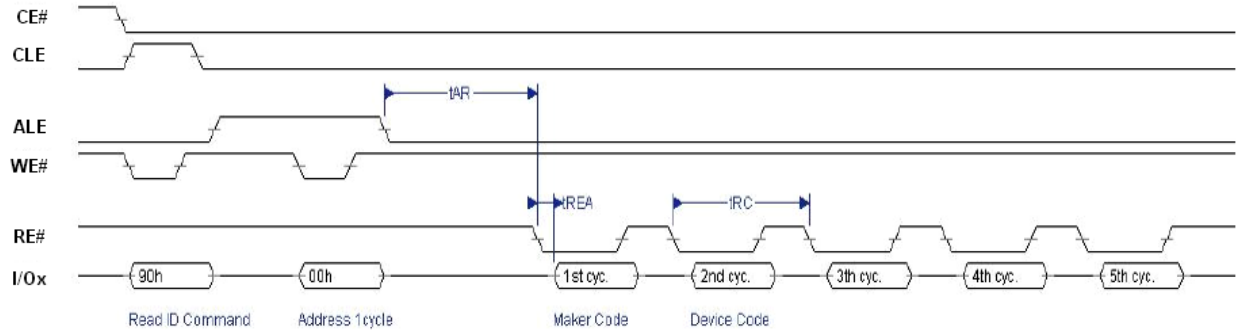



**Figure 22 Read ID Operation**

# 10. ID Definition Table

ID Access command = 90h

| 1st Cycle (Maker Code) | 2nd Cycle (Device Code) | 3rd Cycle | 4th Cycle | 5th Cycle | 6th ~ 8th Cycle |
|---|---|---|---|---|---|
| C8h | D0h | 90h | 95h | 30h | 7Fh |

| | Description |
|---|---|
| 1st Byte | Maker Code |
| 2nd Byte | Device Code |
| 3rd Byte | Internal Chip Number, Cell Type, etc. |
| 4th Byte | Page Size, Block Size, etc. |
| 5th Byte | Plane Number, Plane Size |
| 6th Byte | JEDEC Maker Code Continuation Code, 7Fh |
| 7th Byte | JEDEC Maker Code Continuation Code, 7Fh |
| 8th Byte | JEDEC Maker Code Continuation Code, 7Fh |

**3rd ID Data**

| Item | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---|---|---|---|---|---|---|---|---|---|
| Internal Chip Number | 1<br>2<br>4<br>8 | | | | | | | 0<br>0<br>1<br>1 | 0<br>1<br>0<br>1 |
| Cell Type | 2 Level Cell<br>4 Level Cell<br>8 Level Cell<br>16 Level Cell | | | | | 0<br>0<br>1<br>1 | 0<br>1<br>0<br>1 | | |
| Reserved | Reserved | | | 0 | 1 | | | | |
| Interleave Program Between multiple chips | Not Support<br>Support | | 0<br>1 | | | | | | |
| Cache Program | Not Support<br>Support | 0<br>1 | | | | | | | |

**4th ID Data**

| Item | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---|---|---|---|---|---|---|---|---|---|
| Page Size (w/o redundant area) | 1KB | | | | | | | 0 | 0 |
| | 2KB | | | | | | | 0 | 1 |
| | 4KB | | | | | | | 1 | 0 |
| | 8KB | | | | | | | 1 | 1 |
| Redundant Area Size (byte/512byte) | 8 | | | | | | 0 | | |
| | 16 | | | | | | 1 | | |
| Block Size (w/o redundant area) | 64KB | | | 0 | 0 | | | | |
| | 128KB | | | 0 | 1 | | | | |
| | 256KB | | | 1 | 0 | | | | |
| | 512KB | | | 1 | 1 | | | | |
| Organization | x8 | | 0 | | | | | | |
| | x16 | | 1 | | | | | | |
| Serial Access Time | 45ns | 0 | | | | 0 | | | |
| | Reserved | 0 | | | | 1 | | | |
| | 25ns | 1 | | | | 0 | | | |
| | Reserved | 1 | | | | 1 | | | |

**5th ID Data**

| Item | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---|---|---|---|---|---|---|---|---|---|
| ECC Level | 4bit/512B | | | | | | | 0 | 0 |
| | 2 bit/512B | | | | | | | 0 | 1 |
| | 1bit/512B | | | | | | | 1 | 0 |
| | Reserved | | | | | | | 1 | 1 |
| Plane Number | 1 | | | | | 0 | 0 | | |
| | 2 | | | | | 0 | 1 | | |
| | 4 | | | | | 1 | 0 | | |
| | 8 | | | | | 1 | 1 | | |
| Plane Size (without redundant area) | 64Mb | | 0 | 0 | 0 | | | | |
| | 128Mb | | 0 | 0 | 1 | | | | |
| | 256Mb | | 0 | 1 | 0 | | | | |
| | 512Mb | | 0 | 1 | 1 | | | | |
| | 1Gb | | 1 | 0 | 0 | | | | |
| | 2Gb | | 1 | 0 | 1 | | | | |
| | 4Gb | | 1 | 1 | 0 | | | | |
| | 8Gb | | 1 | 1 | 1 | | | | |
| Reserved | Reserved | 0 | | | | | | | |

**6th ~ 8th ID Data**

| Item | Description | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC Maker Code Continuation Code | 7F | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# 11. Device Operation

## 11.1 Page Read

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h command, five-cycle address, and 30h command. After initial power up, the 00h command can be skipped because it has been latched in the command register. The 2,112Byte of data on a page are transferred to cache registers via data registers within 25us ($t_R$). Host controller can detect the completion of this data transfer by checking the R/B# output. Once data in the selected page have been loaded into cache registers, each Byte can be read out in 45ns/ 25ns cycle time by continuously pulsing RE#. The repetitive high-to-low transitions of RE# clock signal make the device output data starting from the designated column address to the last column address.

The device can output data at a random column address instead of sequential column address by using the Random Data Output command. Random Data Output command can be executed multiple times in a page.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation. A page read sequence is illustrated in Figure 23, where column address, page address are placed in between commands 00h and 30h. After $t_R$ read time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 30h. Host controller can toggle RE# to access data starting with the designated column address and their successive bytes.

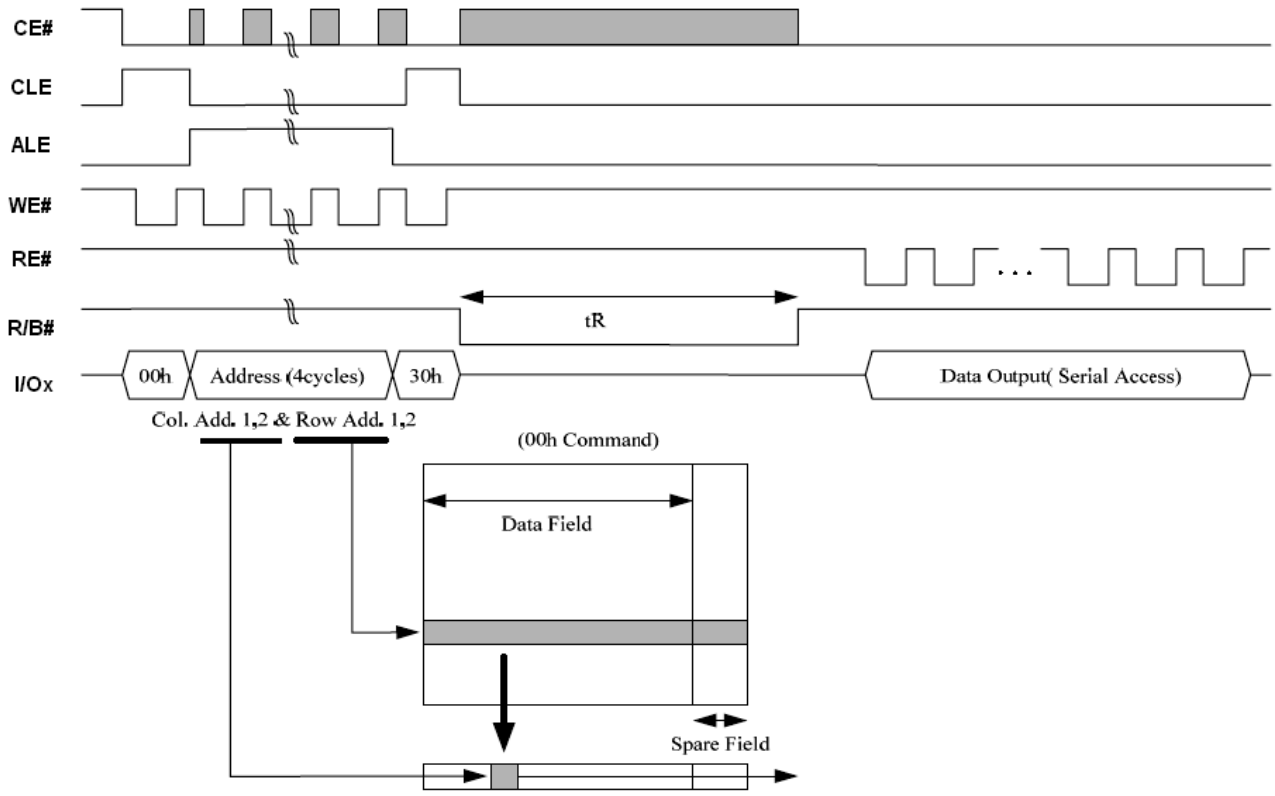



**Figure 23. Read Operation**

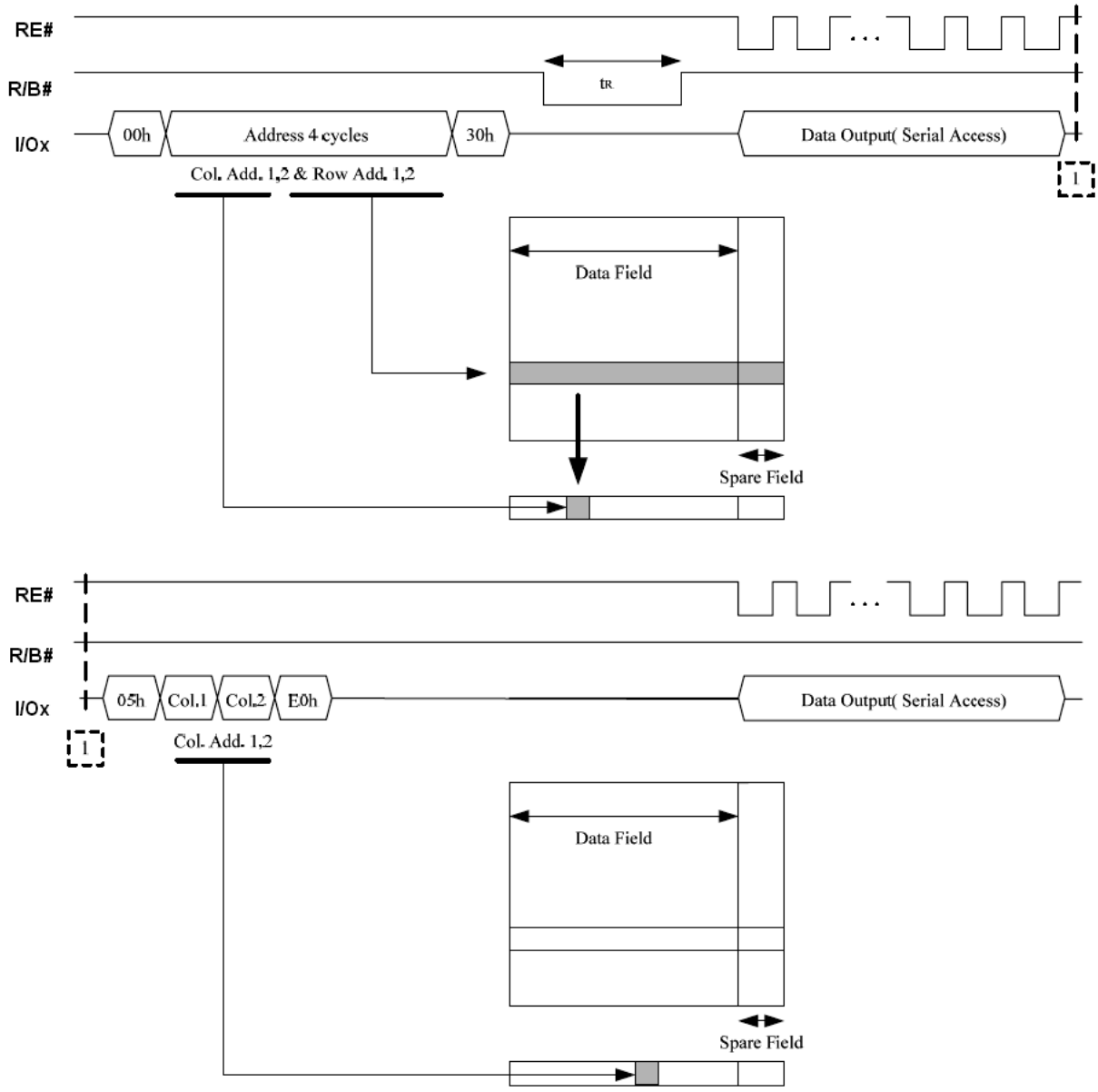



**Figure 24. Random Data Output In a Page**

## 11.2 Page Program

The device is programmed based on the unit of a page, and consecutive partial page programming on one page without intervening erase operation is strictly prohibited. Addressing of page program operations within a block should be in sequential order. A complete page program cycle consists of a serial data input cycle in which up to 2,112byte (1,056word) of data can be loaded into data register via cache register, followed by a programming period during which the loaded data are programmed into the designated memory cells.

The serial data input cycle begins with the Serial Data Input command (80h), followed by a five-cycle address input and then serial data loading. The bytes not to be programmed on the page do not need to be loaded. The column address for the next data can be changed to the address follows Random Data Input command (85h). Random Data Input command may be repeated multiple times in a page. The Page Program Confirm command (10h) starts the programming process. Writing 10h alone without entering data will not initiate the programming process. The internal write engine automatically executes the corresponding algorithm and controls timing for programming and verification, thereby freeing the host controller for other tasks. Once the program process starts, the host controller can detect the completion of a program cycle by monitoring the R/B# output or reading the Status bit (I/O6) using the Read Status command. Only Read Status and Reset commands are valid during programming. When the Page Program operation is completed, the host controller can check the Status bit (I/O0) to see if the Page Program operation is successfully done. The command register remains the Read Status mode unless another valid command is written to it.

A page program sequence is illustrated in Figure 25, where column address, page address, and data input are placed in between 80h and 10h. After $t_{PROG}$ program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.

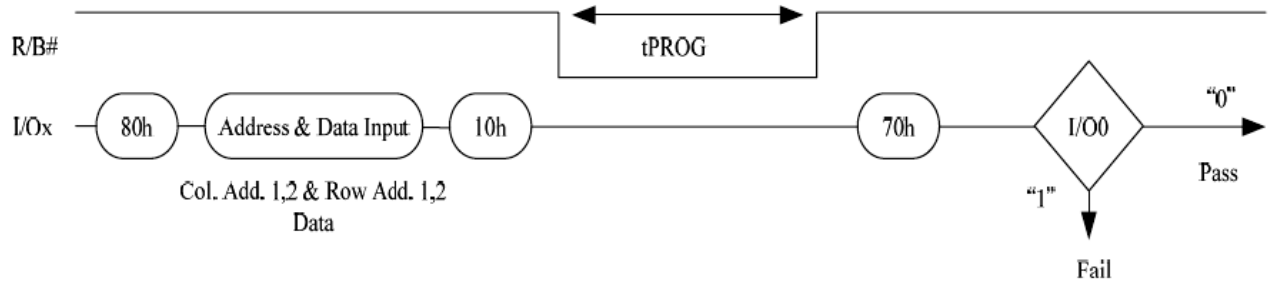



**Figure 25. Program & Read Status Operation**

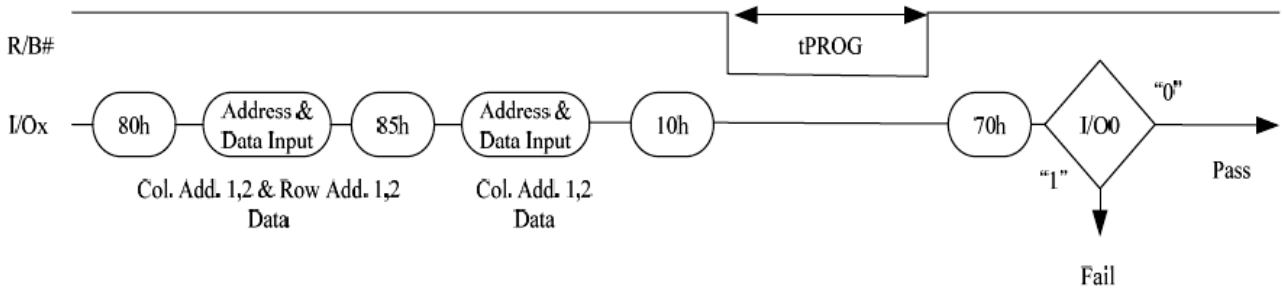



**Figure 26. Random Data Input In a Page**

## 11.3 Cache Program

Cache Program is an extension of Page Program, which is executed with 2,112 byte (x8) or 1,056 words (x16) data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2,112 bytes (x8) or 1,056 words (x16) into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time ($t_{CBSY}$) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, $t_{CBSY}$ is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identity the completion of internal programming. If the system monitors the progress of programming only with R/B#, the last page of the target programming sequence must be programmed with actual Page Program command (10h).

**Cache Program** (available only within a block)

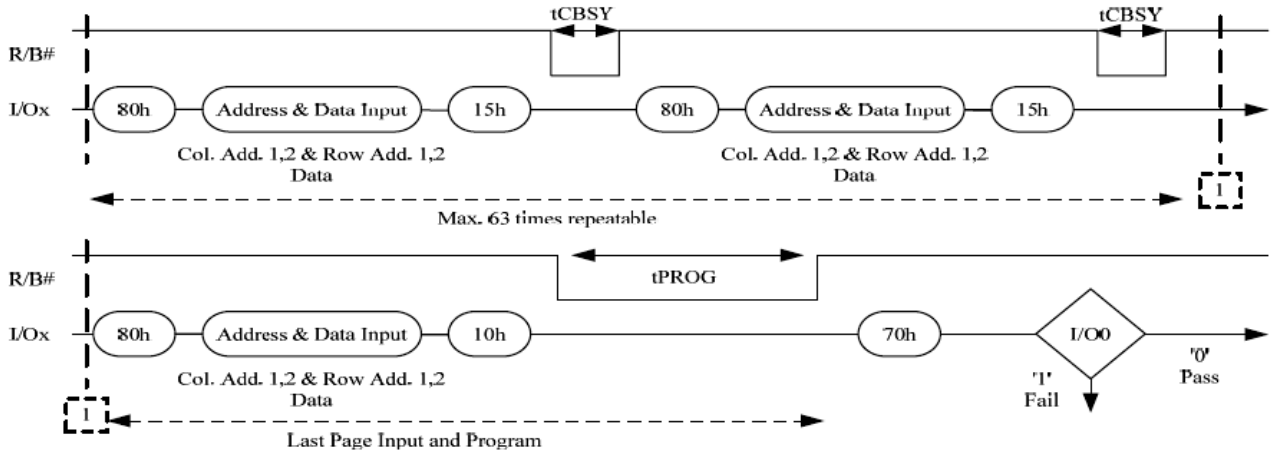



**Figure 27. Cache Program**

**Note:**

1. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.
2. $t_{PROG}$ = Program time for the last page + Program time for the (last-1)th page – (Program command cycle time + Last page data loading time)

## 11.4 Copy-Back Program

Copy-Back Program is designed to efficiently copy data stored in memory cells without time-consuming data reloading when there is no bit error detected in the stored data. The benefit is particularly obvious when a portion of a block is updated and the rest of the block needs to be copied to a newly assigned empty block. Copy-Back operation is a sequential execution of Read for Copy-Back and of Copy-Back Program with Destination address. A Read for Copy-Back operation with “35h” command and the Source address moves the whole 2,112byte data into the internal buffer. The host controller can detect bit errors by sequentially reading the data output. Copy-Back Program is initiated by issuing Page-Copy Data-Input command (85h) with Destination address. If data modification is necessary to correct bit errors and to avoid error propagation, data can be reloaded after the Destination address. Data modification can be repeated multiple times as shown in Figure 29. Actual programming operation begins when Program Confirm command (10h) is issued. Once the program process starts, the Read Status command (70h) may be entered to read the status register. The host controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Copy-Back Program is complete, the Status Bit (I/O0) may be checked. The command register remains Read Status mode until another valid command is written to it.

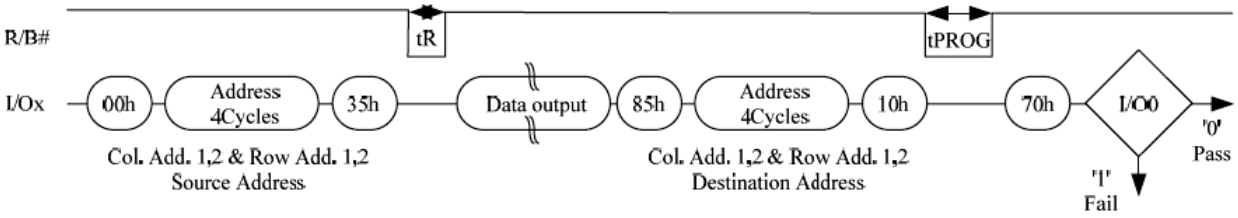



**Figure 28. Page Copy-Back Program Operation**

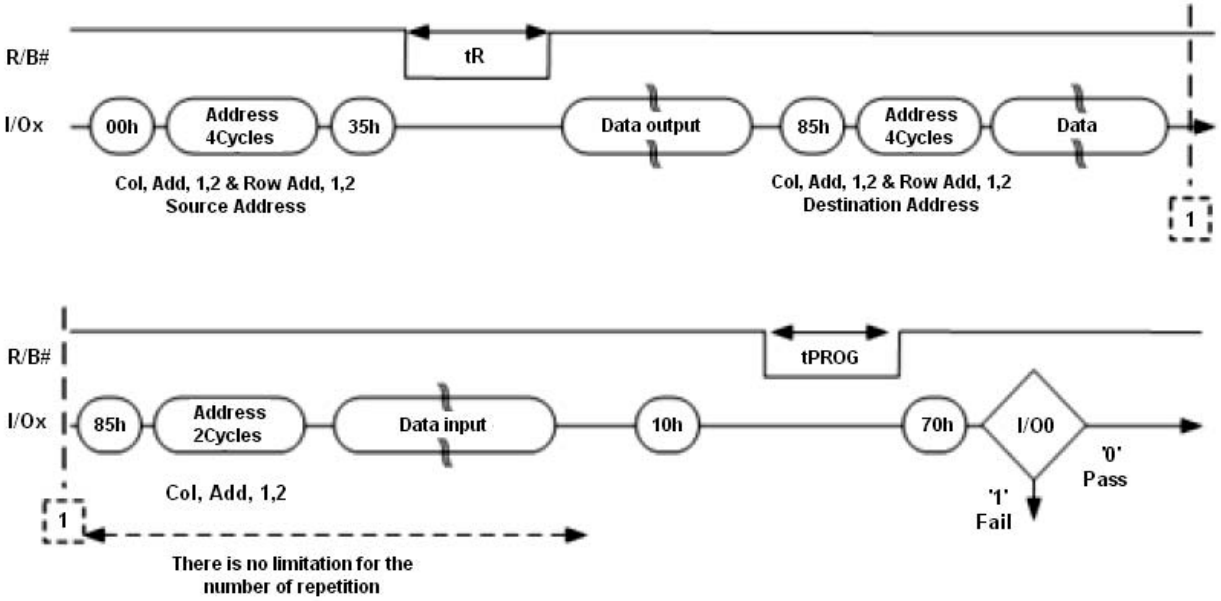



**Figure 29. Page Copy-Back Program Operation with Random Data Input**

## 11.5 Block Erase

The block-based Erase operation is initiated by an Erase Setup command (60h), followed by a three-cycle row address, in which only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command (D0h) following the row address starts the internal erasing process. The two-step command sequence is designed to prevent memory content from being inadvertently changed by external noise.

At the rising edge of WE# after the Erase Confirm command input, the internal control logic handles erase and erase-verify. When the erase operation is completed, the host controller can check Status bit (I/O0) to see if the erase operation is successfully done. Figure 30 illustrates a block erase sequence, and the address input (the first page address of the selected block) is placed in between commands 60h and D0h. After $t_{BERASE}$ erase time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after D0h to check the execution status of erase operation.

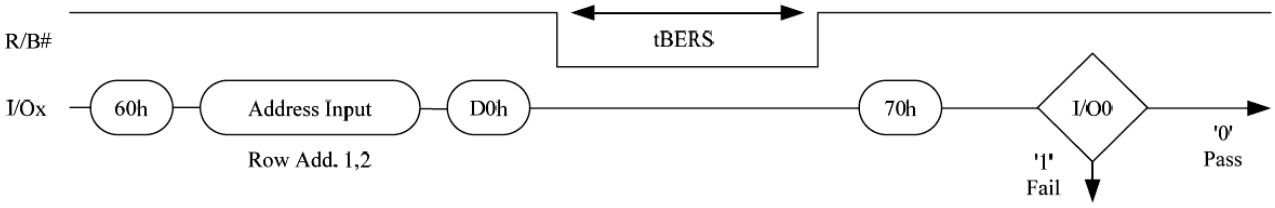



**Figure 30. Block Erase Operation**

## 11.6 One-Time Programmable (OTP) Operations

This Eon flash device offers one-time programmable memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the Set Feature (EFh-90h-01h) command. When the device is in OTP operation mode, subsequent Read and/or Page Program are applied to the OTP area. **When you want to come back to normal operation, you need to use EFh-90h-00h for OTP mode release. Otherwise, device will stay in OTP mode.**

To program an OTP page, issue the Serial Data Input (80h) command followed by 4 address cycles. The first two address cycles are column address that must be set as 00h. For the third cycle, select a page in the range of 00h through 1Dh. The fourth and fifth cycle is fixed at 00h. Next, up to 2,112 bytes of data can be loaded into data register. The bytes other than those to be programmed do not need to be loaded. Random Data Input (85h) command in this device is prohibited. The Page Program confirms (10h) command initiates the programming process. The internal control logic automatically executes the programming algorithm, timing and verification. Please note that **no partial-page program** is allowed in the OTP area. In addition, the OTP pages must be programmed in the ascending order. A programmed OTP page will be **automatically protected**.

Similarly, to read data from an OTP page, set the device to OTP operation mode and then issue the Read (00h-30h) command. The first two address cycles are column address that must be set as 00h and Random Data Output (05h-E0h) command is prohibited as well.

All pages in the OTP area will be protected simultaneously by issuing the Set Feature (EFh-90h-03h) command to set the device to OTP protection mode. After the OTP area is protected, no page in the

area is programmable and the whole area cannot be unprotected.

The Read Status (70h) command is the only valid command for reading status in OTP operation mode.

**Table 3. OTP Modes and Commands**

| | | Set Feature | Command |
|---|---|---|---|
| **OTP Operation mode** | Read | EFh-90h[1]-01h[2] | 00h-30h |
| | Page Program | EFh-90h-01h | 80h-10h |
| **OTP Protection mode** | Program Protect | EFh-90h-03h | 80h-10h |
| **OTP Release mode** | Leave OTP mode | EFh-90h-00h | |

**Note:**
1. 90h is OTP status register address.
2. 00h, 01h, and 03h are OTP status register data values.

**Table 4. OTP Area Details**

| Description | Value |
|---|---|
| Number of OTP pages | 30 |
| OTP pages address | 00h – 1Dh |
| Number of partial page programs for each page in the OTP area | 1 |

## 11.7 Read Status

A status register on the device is used to check whether program or erase operation is completed and whether the operation is completed successfully. After writing 70h/F1h command to the command register, a read cycle outputs the content of the status register to I/O pins on the falling edge of CE# or RE#, whichever occurs last. These two commands allow the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to toggle for status change.

The command register remains in Read Status mode unless other commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h) is needed to start read cycles.

**Table 5. Status Register Definition for 70h Command**

| I/O | Page Program | Block Erase | Read | Cache Read | Definition |
|---|---|---|---|---|---|
| I/O0 | Pass / Fail | Pass / Fail | N/A | N/A | Pass: ”0” , Fail: ”1” |
| I/O1 | N/A | N/A | N/A | N/A | Don’t cared |
| I/O2 | N/A (Pass/Fail, OTP) | N/A | N/A | N/A | Don’t cared |
| I/O3 | N/A | N/A | N/A | N/A | Don’t cared |
| I/O4 | N/A | N/A | N/A | N/A | Don’t cared |
| I/O5 | N/A | N/A | N/A | True Ready / Busy | Busy: ”0” Ready: ”1” |
| I/O6 | Ready / Busy | Ready / Busy | Ready / Busy | Ready / Busy | Busy: ”0” Ready: ”1” |
| I/O7 | Write Protect | Write Protect | Write Protect | Write Protect | Protected: ”0” Not Protected: ”1” |

**Note:**

1. I/Os defined NA are recommended to be masked out when Read Status is being executed.
2. n : current page, n-1 : previous page.

## 11.8 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

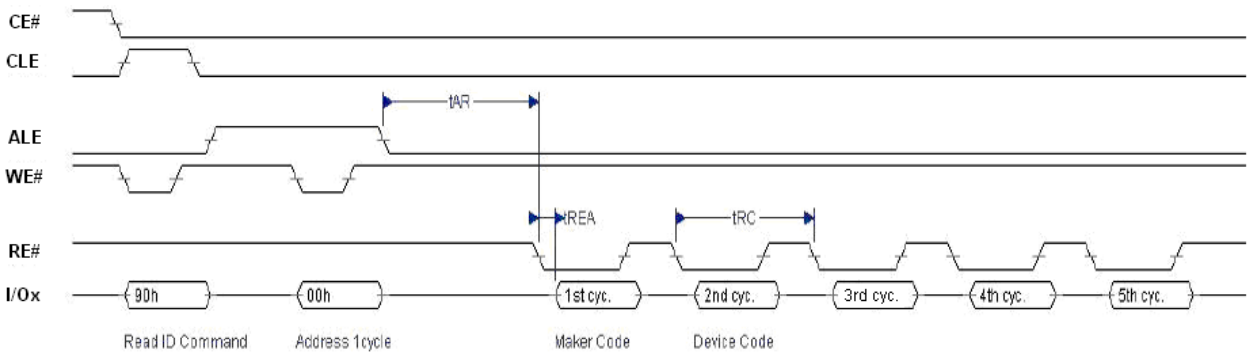



**Figure 31. Read ID Operation**

**Table 6. ID Definition Table**

ID Access command = 90h

| 1st Cycle (Maker Code) | 2nd Cycle (Device Code) | 3rd Cycle | 4th Cycle | 5th Cycle |
|---|---|---|---|---|
| C8h | D0h | 90h | 95h | 30h |

## 11.9 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP# is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin changes to low for tRST after the Reset command is written. Refer to Figure 32 below.

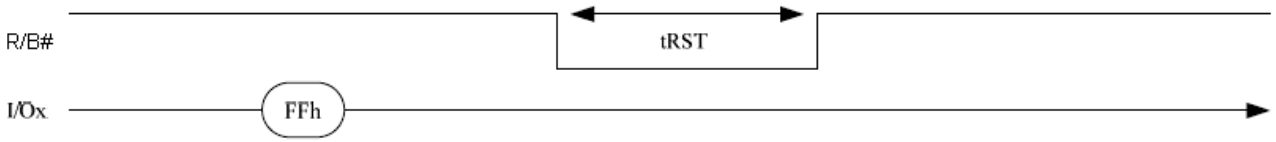



**Figure 32. Reset Operation**

**Table 7. Device Status**

| | After Power-up | After Reset |
|---|---|---|
| Operation mode | 00h Command is latched | Waiting for next command |

## 11.10 Cache Read

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of tDCBSYR, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.

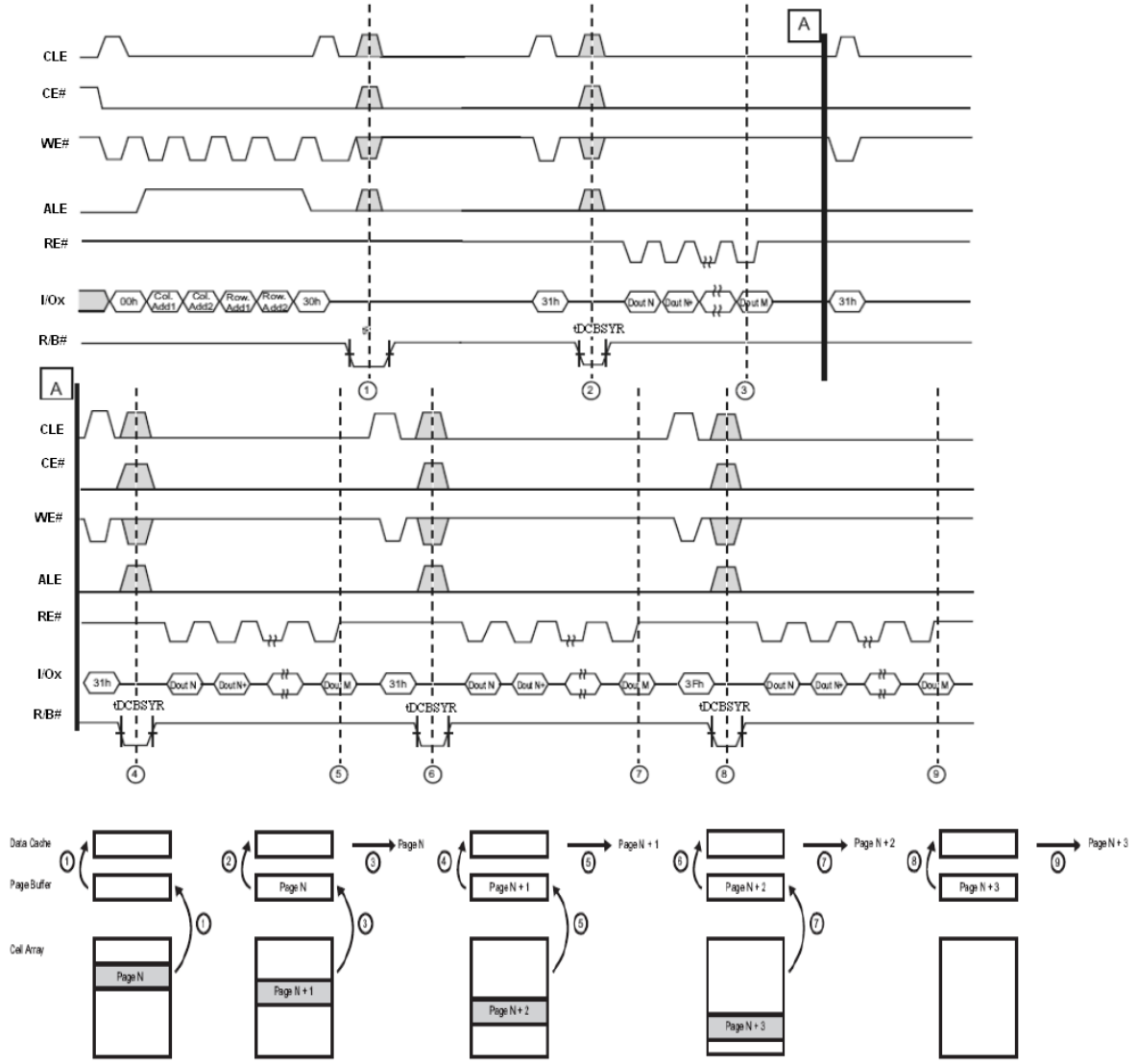
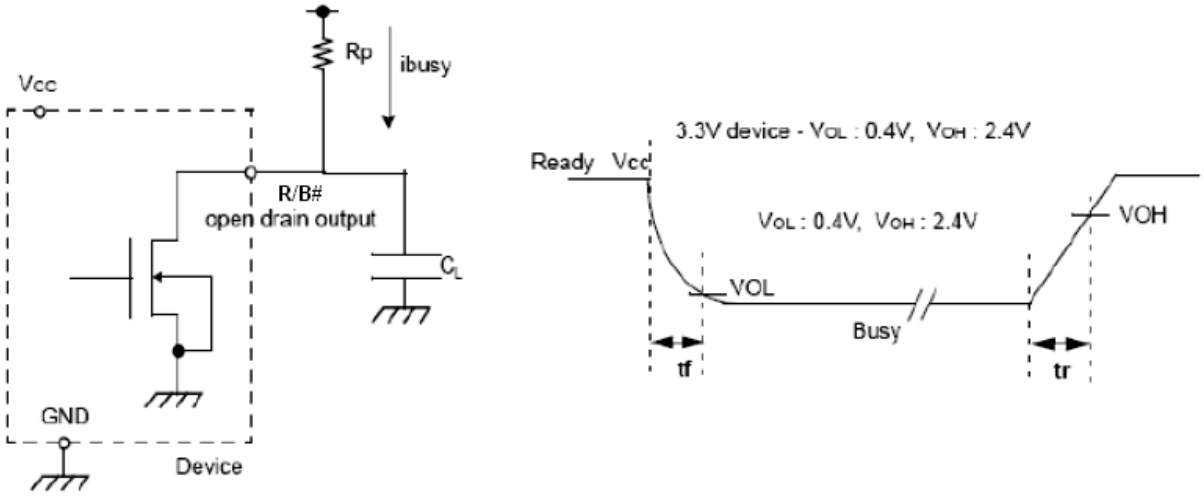


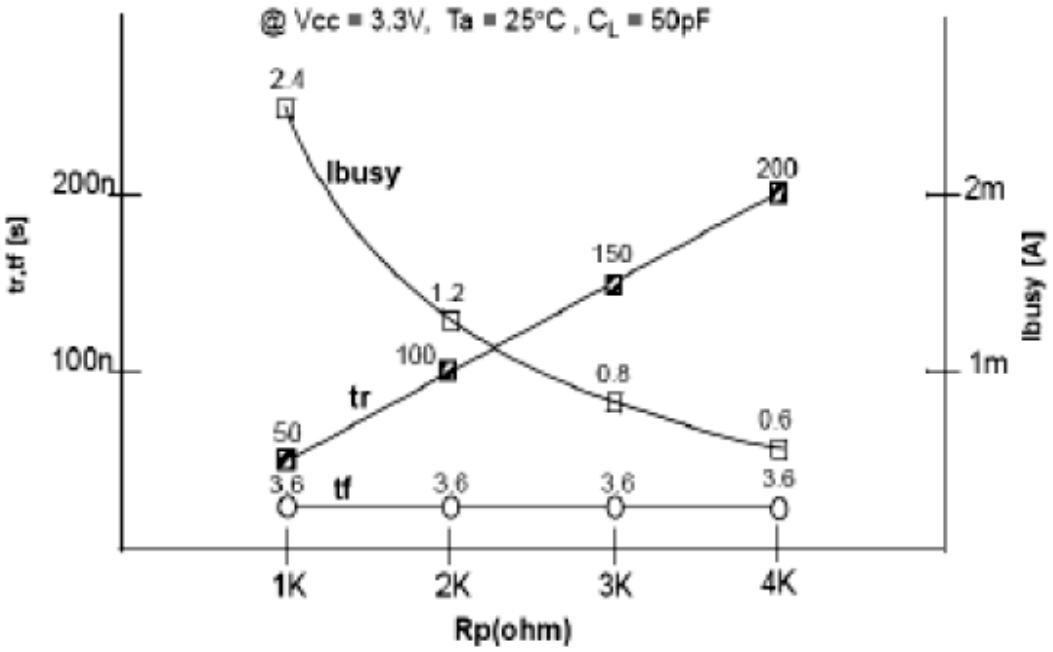

**Figure 33. Read Operation with Cache Read**

## 11.11 Ready/Busy#

The device has a R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transition to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr (R/B#) and current drain during busy (ibusy), an appropriate value can be obtained with the following reference chart (Fig. 34). Its value can be determined by the following guidance.




## $R_P$ vs $t_{RHOH}$ vs $C_L$




## $R_P$ value guidance

$$Rp(min, 3.3V\ part) = \frac{VCC(Max.) - VOL(Max.)}{IOL + \Sigma IL} = \frac{3.2V}{8mA + \Sigma IL}$$

where $I_L$ is the sum of the input currents of all devices tied to the R/B# pin.
$R_P$ (max) is determined by maximum permissible limit of tr

**Figure 34. Read/Busy# Pin Electrical Specifications**

## 11.12 Data Protection & Power-up sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device R/B# signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are 70h.

The WP# signal is useful for protecting against data corruption at power on/off.

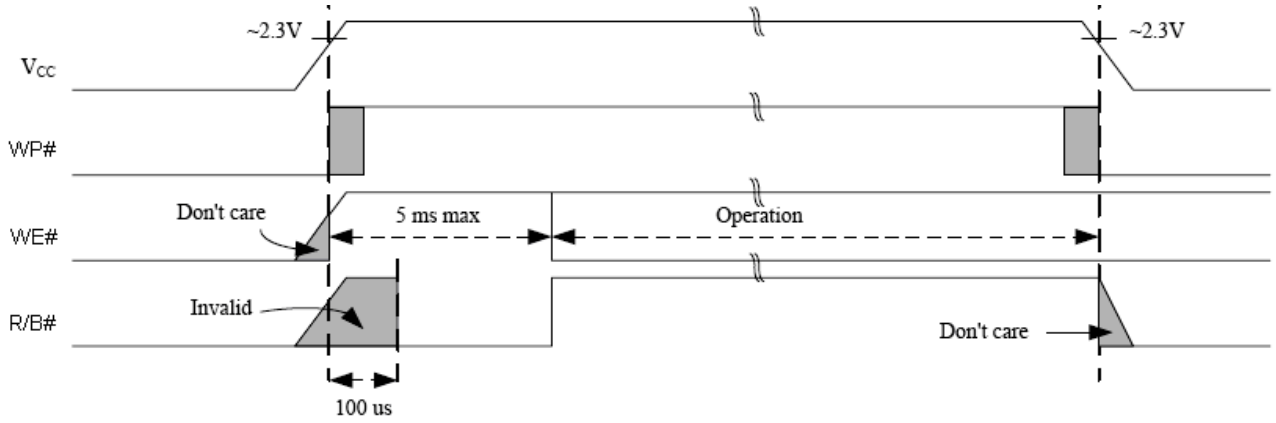
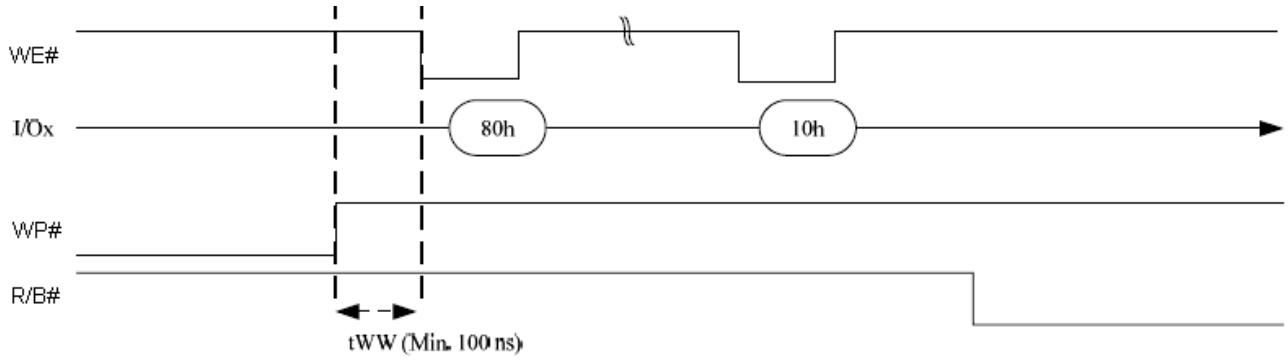



**Figure 35. AC Waveforms for Power Transition**

## 11.13 Write Protect Operation

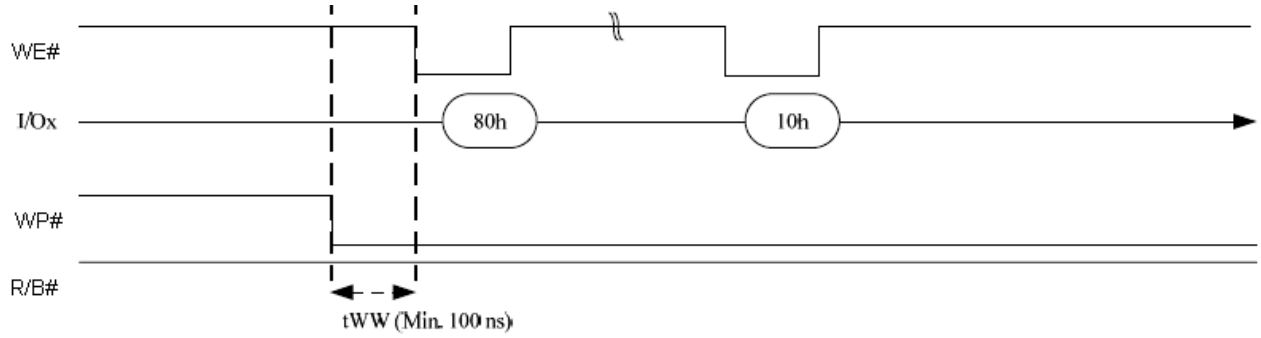
Enabling WP# during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

**Enable Programming:**

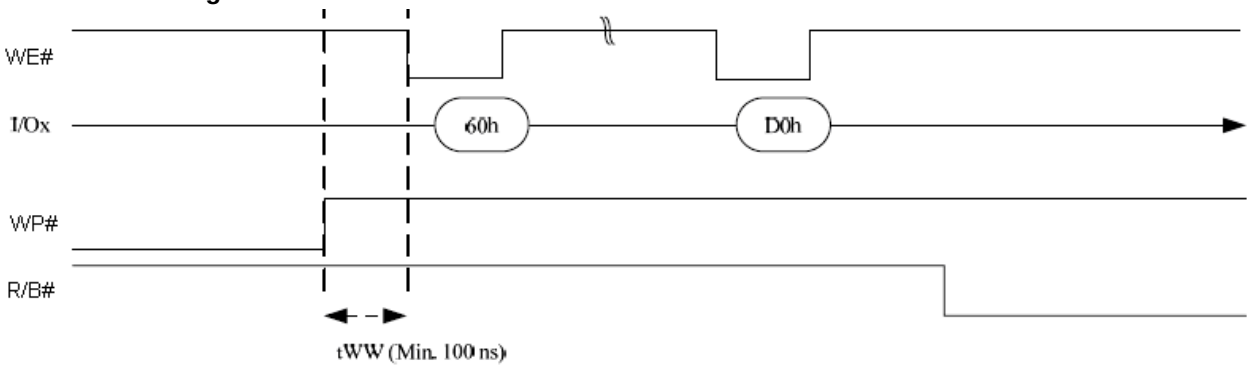



**Note**: WP# keeps “High” until programming finish

**Disable Programming:**




**Enable Erasing:**




**Note**: WP# keeps “High” until erasing finish

**Disable Erasing:**

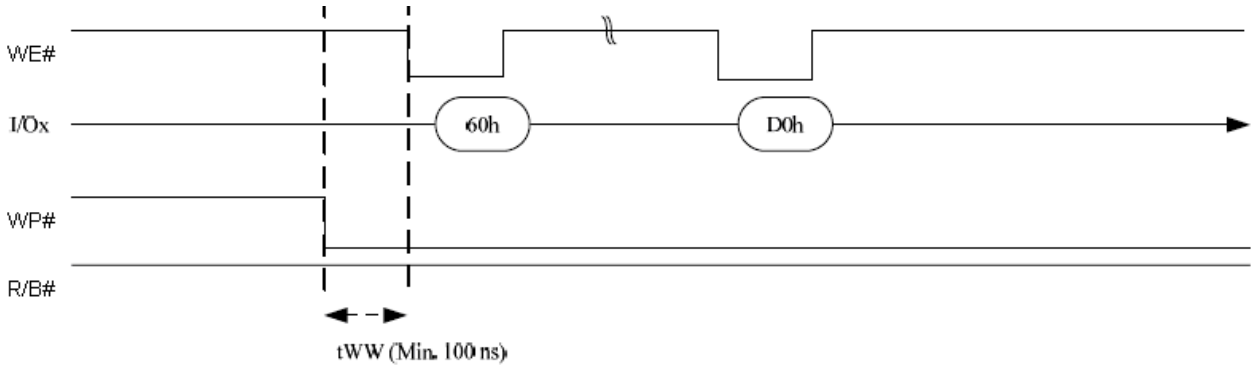



**Figure 36. Erase and Program Operations**

# Revisions List

| Revision No | Description | Date |
|---|---|---|
| A | Initial Release | 2013/09/30 |