Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

Eon products’ New Top Marking

cFeon

cFeon Top Marking Example:

cFeon

Part Number: XXXX-XXX
Lot Number: XXXXX
Date Code: XXXXX

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as an Eon product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

Eon continues to support existing part numbers beginning with “Eon” and “cFeon” top marking. To order these products, during the transition please specify “Eon top marking” or “cFeon top marking” on your purchasing orders.

For More Information

Please contact your local sales office for additional information about Eon memory solutions.

EN29LV640T/B
64 Megabit (8M x 8-bit / 4M x 16-bit) Flash Memory
Boot Sector Flash Memory, CMOS 3.0 Volt-only

FEATURES

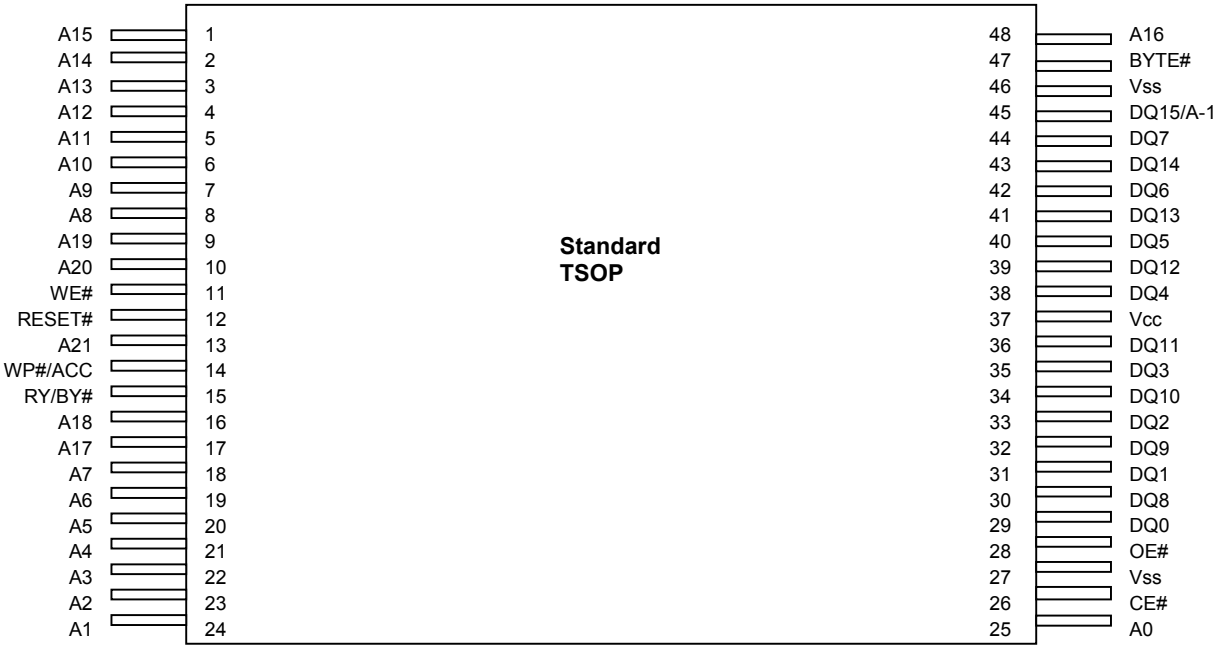
- Single power supply operation
  - Full voltage range: 2.7-3.6 volt read and write operations for battery-powered applications.
  - Regulated voltage range: 3.0-3.6 volt read and write operations for high performance 3.3 volt microprocessors.
- High performance
  - Full voltage range: access times as fast as 90 ns
  - Regulated voltage range: access times as fast as 70ns
- Low power consumption (typical values at 5 MHz)
  - 9 mA typical active read current
  - 20 mA typical program/erase current
  - Less than 1 μA current in standby or automatic sleep mode.
- Flexible Sector Architecture:
  - Eight 8-Kbyte sectors, One hundred and twenty-seven 32K-Word / 64K-byte sectors.
  - 8-Kbyte sectors for Top or Bottom boot.
  - Sector/Sector Group protection: Hardware locking of sectors to prevent program or erase operations within individual sectors
    Additionally, temporary Sector Group Unprotect allows code changes in previously locked sectors.
- High performance program/erase speed
  - Word program time: 8μs typical
  - Sector erase time: 100ms typical
  - Chip erase time: 16s typical
- JEDEC Standard compatible
- Standard DATA# polling and toggle bits feature
- Erase Suspend / Resume modes:
  Read and program another Sector during Erase Suspend Mode
- Support JEDEC Common Flash Interface (CFI).
- Low Vcc write inhibit < 2.5V
- Minimum 100K program/erase endurance cycles.
- RESET# hardware reset pin
  - Hardware method to reset the device to read mode.
- WP#/ACC input pin
  - Write Protect (WP#) function allows protection of outermost two boot sectors, regardless of sector protect status
  - Acceleration (ACC) function provides accelerated program times
- Package Options
  - 48-pin TSOP (Type 1)
  - 48 ball 6mm x 8mm TFBGA
- Industrial Temperature Range.

GENERAL DESCRIPTION

The EN29LV640T/B is a 64-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 8,388,608 bytes or 4,194,304 words. Any word can be programmed typically in 8μs. The EN29LV640T/B features 3.0V voltage read and write operation, with access times as fast as 70ns to eliminate the need for WAIT states in high-performance microprocessor systems.

The EN29LV640T/B has separate Output Enable (OE#), Chip Enable (CE#), and Write Enable (WE#) controls, which eliminate bus contention issues. This device is designed to allow either single Sector or full Chip erase operation, where each Sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.

CONNECTION DIAGRAMS



48-Ball TFBGA

Top View, Balls Facing Down

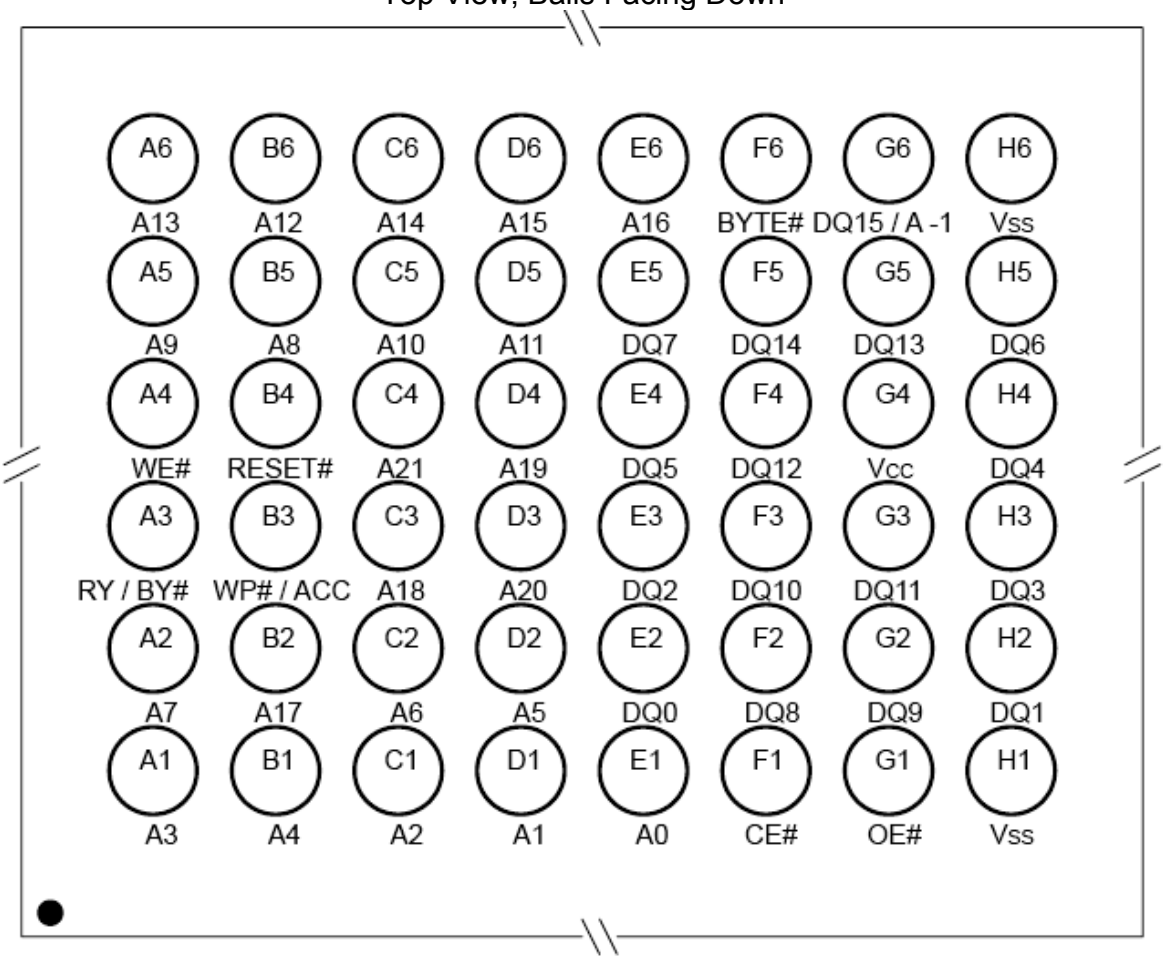
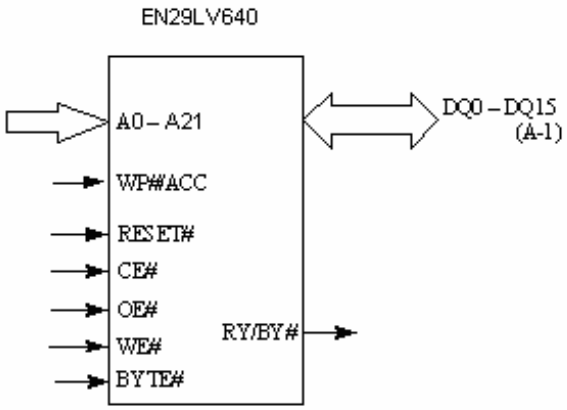


TABLE 1. PIN DESCRIPTION

Pin Name	Function
A0-A21	22 Address inputs
DQ0-DQ14	15 Data Inputs/Outputs
DQ15 / A-1	DQ15 (data input/output, in word mode), A-1 (LSB address input, in byte mode)
CE#	Chip Enable
OE#	Output Enable
WE#	Write Enable
WP#/ACC	Write Protect / Acceleration Pin
RESET#	Hardware Reset Pin
BYTE#	Byte/Word mode selection
RY/BY#	Ready/Busy Output
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground
NC	Not Connected to anything

LOGIC DIAGRAM



ORDERING INFORMATION

EN29LV640 T — 90 T I P

PACKAGING CONTENT
(Blank) = Conventional
P = RoHS compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
T = 48-pin TSOP
B = 48-Ball Thin Fine Pitch Ball Grid Array (TFBGA)
0.80mm pitch, 6mm x 8mm package

SPEED
70 = 70ns Regulated range 3.0V~3.6V
90 = 90ns

BOOT CODE SECTOR ARCHITECTURE
T = Top boot Sector
B = Bottom boot Sector

BASE PART NUMBER
EN = EON Silicon Solution Inc.
29LV = FLASH, 3V Read, Program and Erase
640 = 64 Megabit (8M x 8 / 4M x 16)

Table 2A. Top Boot Sector Address Tables (EN29LV640T)

Sector	A21 – A12	Sector Size (Kbytes / Kwords)	Address Range (h) Byte mode (x8)	Address Range (h) Word Mode (x16)
SA0	0000000xxx	64/32	000000–00FFFF	000000–007FFF
SA1	0000001xxx	64/32	010000–01FFFF	008000–00FFFF
SA2	0000010xxx	64/32	020000–02FFFF	010000–017FFF
SA3	0000011xxx	64/32	030000–03FFFF	018000–01FFFF
SA4	0000100xxx	64/32	040000–04FFFF	020000–027FFF
SA5	0000101xxx	64/32	050000–05FFFF	028000–02FFFF
SA6	0000110xxx	64/32	060000–06FFFF	030000–037FFF
SA7	0000111xxx	64/32	070000–07FFFF	038000–03FFFF
SA8	0001000xxx	64/32	080000–08FFFF	040000–047FFF
SA9	0001001xxx	64/32	090000–09FFFF	048000–04FFFF
SA10	0001010xxx	64/32	0A0000–0AFFFF	050000–057FFF
SA11	0001011xxx	64/32	0B0000–0BFFFF	058000–05FFFF
SA12	0001100xxx	64/32	0C0000–0CFFFF	060000–067FFF
SA13	0001101xxx	64/32	0D0000–0DFFFF	068000–06FFFF
SA14	0001110xxx	64/32	0E0000–0EFFFF	070000–077FFF
SA15	0001111xxx	64/32	0F0000–0FFFFF	078000–07FFFF
SA16	0010000xxx	64/32	100000–10FFFF	080000–087FFF
SA17	0010001xxx	64/32	110000–11FFFF	088000–08FFFF
SA18	0010010xxx	64/32	120000–12FFFF	090000–097FFF
SA19	0010011xxx	64/32	130000–13FFFF	098000–09FFFF
SA20	0010100xxx	64/32	140000–14FFFF	0A0000–0A7FFF
SA21	0010101xxx	64/32	150000–15FFFF	0A8000–0AFFFF
SA22	0010110xxx	64/32	160000–16FFFF	0B0000–0B7FFF
SA23	0010111xxx	64/32	170000–17FFFF	0B8000–0BFFFF
SA24	0011000xxx	64/32	180000–18FFFF	0C0000–0C7FFF
SA25	0011001xxx	64/32	190000–19FFFF	0C8000–0CFFFF
SA26	0011010xxx	64/32	1A0000–1AFFFF	0D0000–0D7FFF
SA27	0011011xxx	64/32	1B0000–1BFFFF	0D8000–0DFFFF
SA28	0011100xxx	64/32	1C0000–1CFFFF	0E0000–0E7FFF
SA29	0011101xxx	64/32	1D0000–1DFFFF	0E8000–0EFFFF
SA30	0011110xxx	64/32	1E0000–1EFFFF	0F0000–0F7FFF
SA31	0011111xxx	64/32	1F0000–1FFFFF	0F8000–0FFFFF
SA32	0100000xxx	64/32	200000–20FFFF	100000–107FFF
SA33	0100001xxx	64/32	210000–21FFFF	108000–10FFFF
SA34	0100010xxx	64/32	220000–22FFFF	110000–117FFF
SA35	0100011xxx	64/32	230000–23FFFF	118000–11FFFF
SA36	0100100xxx	64/32	240000–24FFFF	120000–127FFF
SA37	0100101xxx	64/32	250000–25FFFF	128000–12FFFF
SA38	0100110xxx	64/32	260000–26FFFF	130000–137FFF
SA39	0100111xxx	64/32	270000–27FFFF	138000–13FFFF

SA40	0101000xxx	64/32	280000–28FFFF	140000–147FFF
SA41	0101001xxx	64/32	290000–29FFFF	148000–14FFFF
SA42	0101010xxx	64/32	2A0000–2AFFFF	150000–157FFF
SA43	0101011xxx	64/32	2B0000–2BFFFF	158000–15FFFF
SA44	0101100xxx	64/32	2C0000–2CFFFF	160000–167FFF
SA45	0101101xxx	64/32	2D0000–2DFFFF	168000–16FFFF
SA46	0101110xxx	64/32	2E0000–2EFFFF	170000–177FFF
SA47	0101111xxx	64/32	2F0000–2FFFFF	178000–17FFFF
SA48	0110000xxx	64/32	300000–30FFFF	180000–187FFF
SA49	0110001xxx	64/32	310000–31FFFF	188000–18FFFF
SA50	0110010xxx	64/32	320000–32FFFF	190000–197FFF
SA51	0110011xxx	64/32	330000–33FFFF	198000–19FFFF
SA52	0110100xxx	64/32	340000–34FFFF	1A0000–1A7FFF
SA53	0110101xxx	64/32	350000–35FFFF	1A8000–1AFFFF
SA54	0110110xxx	64/32	360000–36FFFF	1B0000–1B7FFF
SA55	0110111xxx	64/32	370000–37FFFF	1B8000–1BFFFF
SA56	0111000xxx	64/32	380000–38FFFF	1C0000–1C7FFF
SA57	0111001xxx	64/32	390000–39FFFF	1C8000–1CFFFF
SA58	0111010xxx	64/32	3A0000–3AFFFF	1D0000–1D7FFF
SA59	0111011xxx	64/32	3B0000–3BFFFF	1D8000–1DFFFF
SA60	0111100xxx	64/32	3C0000–3CFFFF	1E0000–1E7FFF
SA61	0111101xxx	64/32	3D0000–3DFFFF	1E8000–1EFFFF
SA62	0111110xxx	64/32	3E0000–3EFFFF	1F0000–1F7FFF
SA63	0111111xxx	64/32	3F0000–3FFFFF	1F8000–1FFFFF
SA64	1000000xxx	64/32	400000–40FFFF	200000–207FFF
SA65	1000001xxx	64/32	410000–41FFFF	208000–20FFFF
SA66	1000010xxx	64/32	420000–42FFFF	210000–217FFF
SA67	1000011xxx	64/32	430000–43FFFF	218000–21FFFF
SA68	1000100xxx	64/32	440000–44FFFF	220000–227FFF
SA69	1000101xxx	64/32	450000–45FFFF	228000–22FFFF
SA70	1000110xxx	64/32	460000–46FFFF	230000–237FFF
SA71	1000111xxx	64/32	470000–47FFFF	238000–23FFFF
SA72	1001000xxx	64/32	480000–48FFFF	240000–247FFF
SA73	1001001xxx	64/32	490000–49FFFF	248000–24FFFF
SA74	1001010xxx	64/32	4A0000–4AFFFF	250000–257FFF
SA75	1001011xxx	64/32	4B0000–4BFFFF	258000–25FFFF
SA76	1001100xxx	64/32	4C0000–4CFFFF	260000–267FFF
SA77	1001101xxx	64/32	4D0000–4DFFFF	268000–26FFFF
SA78	1001110xxx	64/32	4E0000–4EFFFF	270000–277FFF
SA79	1001111xxx	64/32	4F0000–4FFFFF	278000–27FFFF
SA80	1010000xxx	64/32	500000–50FFFF	280000–287FFF
SA81	1010001xxx	64/32	510000–51FFFF	288000–28FFFF
SA82	1010010xxx	64/32	520000–52FFFF	290000–297FFF

SA83	1010011xxx	64/32	530000–53FFFF	298000–29FFFF
SA84	1010100xxx	64/32	540000–54FFFF	2A0000–2A7FFF
SA85	1010101xxx	64/32	550000–55FFFF	2A8000–2AFFFF
SA86	1010110xxx	64/32	560000–56FFFF	2B0000–2B7FFF
SA87	1010111xxx	64/32	570000–57FFFF	2B8000–2BFFFF
SA88	1011000xxx	64/32	580000–58FFFF	2C0000–2C7FFF
SA89	1011001xxx	64/32	590000–59FFFF	2C8000–2CFFFF
SA90	1011010xxx	64/32	5A0000–5AFFFF	2D0000–2D7FFF
SA91	1011011xxx	64/32	5B0000–5BFFFF	2D8000–2DFFFF
SA92	1011100xxx	64/32	5C0000–5CFFFF	2E0000–2E7FFF
SA93	1011101xxx	64/32	5D0000–5DFFFF	2E8000–2EFFFF
SA94	1011110xxx	64/32	5E0000–5EFFFF	2F0000–2F7FFF
SA95	1011111xxx	64/32	5F0000–5FFFFF	2F8000–2FFFFF
SA96	1100000xxx	64/32	600000–60FFFF	300000–307FFF
SA97	1100001xxx	64/32	610000–61FFFF	308000–30FFFF
SA98	1100010xxx	64/32	620000–62FFFF	310000–317FFF
SA99	1100011xxx	64/32	630000–63FFFF	318000–31FFFF
SA100	1100100xxx	64/32	640000–64FFFF	320000–327FFF
SA101	1100101xxx	64/32	650000–65FFFF	328000–32FFFF
SA102	1100110xxx	64/32	660000–66FFFF	330000–337FFF
SA103	1100111xxx	64/32	670000–67FFFF	338000–33FFFF
SA104	1101000xxx	64/32	680000–68FFFF	340000–347FFF
SA105	1101001xxx	64/32	690000–69FFFF	348000–34FFFF
SA106	1101010xxx	64/32	6A0000–6AFFFF	350000–357FFF
SA107	1101011xxx	64/32	6B0000–6BFFFF	358000–35FFFF
SA108	1101100xxx	64/32	6C0000–6CFFFF	360000–367FFF
SA109	1101101xxx	64/32	6D0000–6DFFFF	368000–36FFFF
SA110	1101110xxx	64/32	6E0000–6EFFFF	370000–377FFF
SA111	1101111xxx	64/32	6F0000–6FFFFF	378000–37FFFF
SA112	1110000xxx	64/32	700000–70FFFF	380000–387FFF
SA113	1110001xxx	64/32	710000–71FFFF	388000–38FFFF
SA114	1110010xxx	64/32	720000–72FFFF	390000–397FFF
SA115	1110011xxx	64/32	730000–73FFFF	398000–39FFFF
SA116	1110100xxx	64/32	740000–74FFFF	3A0000–3A7FFF
SA117	1110101xxx	64/32	750000–75FFFF	3A8000–3AFFFF
SA118	1110110xxx	64/32	760000–76FFFF	3B0000–3B7FFF
SA119	1110111xxx	64/32	770000–77FFFF	3B8000–3BFFFF
SA120	1111000xxx	64/32	780000–78FFFF	3C0000–3C7FFF
SA121	1111001xxx	64/32	790000–79FFFF	3C8000–3CFFFF
SA122	1111010xxx	64/32	7A0000–7AFFFF	3D0000–3D7FFF
SA123	1111011xxx	64/32	7B0000–7BFFFF	3D8000–3DFFFF
SA124	1111100xxx	64/32	7C0000–7CFFFF	3E0000–3E7FFF
SA125	1111101xxx	64/32	7D0000–7DFFFF	3E8000–3EFFFF

SA126	1111110xxx	64/32	7E0000–7EFFFF	3F0000–3F7FFF
SA127	1111111000	8/4	7F0000–7F1FFF	3F8000–3F8FFF
SA128	1111111001	8/4	7F2000–7F3FFF	3F9000–3F9FFF
SA129	1111111010	8/4	7F4000–7F5FFF	3FA000–3FAFFF
SA130	1111111011	8/4	7F6000–7F7FFF	3FB000–3FBFFF
SA131	1111111100	8/4	7F8000–7F9FFF	3FC000–3FCFFF
SA132	1111111101	8/4	7FA000–7FBFFF	3FD000–3FDFFF
SA133	1111111110	8/4	7FC000–7FDFFF	3FE000–3FEFFF
SA134	1111111111	8/4	7FE000–7FFFFF	3FF000–3FFFFF

Note: The address bus is A21:A-1 in byte mode where BYTE# = V_{IL}, or A21:A0 in word mode where BYTE# = V_{IH}.

Table 2B. Bottom Boot Sector Address Tables (EN29LV640B)

Sector	A21 – A12	Sector Size (Kbytes / Kwords)	Address Range (h) Byte mode (x8)	Address Range (h) Word Mode (x16)
SA0	0000000000	8/4	000000–001FFF	000000–000FFF
SA1	0000000001	8/4	002000–003FFF	001000–001FFF
SA2	0000000010	8/4	004000–005FFF	002000–002FFF
SA3	0000000011	8/4	006000–007FFF	003000–003FFF
SA4	0000000100	8/4	008000–009FFF	004000–004FFF
SA5	0000000101	8/4	00A000–00BFFF	005000–005FFF
SA6	0000000110	8/4	00C000–00DFFF	006000–006FFF
SA7	0000000111	8/4	00E000–00FFFF	007000–007FFF
SA8	0000001xxx	64/32	010000–01FFFF	008000–00FFFF
SA9	0000010xxx	64/32	020000–02FFFF	010000–017FFF
SA10	0000011xxx	64/32	030000–03FFFF	018000–01FFFF
SA11	0000100xxx	64/32	040000–04FFFF	020000–027FFF
SA12	0000101xxx	64/32	050000–05FFFF	028000–02FFFF
SA13	0000110xxx	64/32	060000–06FFFF	030000–037FFF
SA14	0000111xxx	64/32	070000–07FFFF	038000–03FFFF
SA15	0001000xxx	64/32	080000–08FFFF	040000–047FFF
SA16	0001001xxx	64/32	090000–09FFFF	048000–04FFFF
SA17	0001010xxx	64/32	0A0000–0AFFFF	050000–057FFF
SA18	0001011xxx	64/32	0B0000–0BFFFF	058000–05FFFF
SA19	0001100xxx	64/32	0C0000–0CFFFF	060000–067FFF
SA20	0001101xxx	64/32	0D0000–0DFFFF	068000–06FFFF
SA21	0001110xxx	64/32	0E0000–0EFFFF	070000–077FFF
SA22	0001111xxx	64/32	0F0000–0FFFFF	078000–07FFFF

SA23	0010000xxx	64/32	100000–10FFFF	080000–087FFF
SA24	0010001xxx	64/32	110000–11FFFF	088000–08FFFF
SA25	0010010xxx	64/32	120000–12FFFF	090000–097FFF
SA26	0010011xxx	64/32	130000–13FFFF	098000–09FFFF
SA27	0010100xxx	64/32	140000–14FFFF	0A0000–0A7FFF
SA28	0010101xxx	64/32	150000–15FFFF	0A8000–0AFFFF
SA29	0010110xxx	64/32	160000–16FFFF	0B0000–0B7FFF
SA30	0010111xxx	64/32	170000–17FFFF	0B8000–0BFFFF
SA31	0011000xxx	64/32	180000–18FFFF	0C0000–0C7FFF
SA32	0011001xxx	64/32	190000–19FFFF	0C8000–0CFFFF
SA33	0011010xxx	64/32	1A0000–1AFFFF	0D0000–0D7FFF
SA34	0011011xxx	64/32	1B0000–1BFFFF	0D8000–0DFFFF
SA35	0011100xxx	64/32	1C0000–1CFFFF	0E0000–0E7FFF
SA36	0011101xxx	64/32	1D0000–1DFFFF	0E8000–0EFFFF
SA37	0011110xxx	64/32	1E0000–1EFFFF	0F0000–0F7FFF
SA38	0011111xxx	64/32	1F0000–1FFFFF	0F8000–0FFFFF
SA39	0100000xxx	64/32	200000–20FFFF	100000–107FFF
SA40	0100001xxx	64/32	210000–21FFFF	108000–10FFFF
SA41	0100010xxx	64/32	220000–22FFFF	110000–117FFF
SA42	0100011xxx	64/32	230000–23FFFF	118000–11FFFF
SA43	0100100xxx	64/32	240000–24FFFF	120000–127FFF
SA44	0100101xxx	64/32	250000–25FFFF	128000–12FFFF
SA45	0100110xxx	64/32	260000–26FFFF	130000–137FFF
SA46	0100111xxx	64/32	270000–27FFFF	138000–13FFFF
SA47	0101000xxx	64/32	280000–28FFFF	140000–147FFF
SA48	0101001xxx	64/32	290000–29FFFF	148000–14FFFF
SA49	0101010xxx	64/32	2A0000–2AFFFF	150000–157FFF
SA50	0101011xxx	64/32	2B0000–2BFFFF	158000–15FFFF
SA51	0101100xxx	64/32	2C0000–2CFFFF	160000–167FFF
SA52	0101101xxx	64/32	2D0000–2DFFFF	168000–16FFFF
SA53	0101110xxx	64/32	2E0000–2EFFFF	170000–177FFF
SA54	0101111xxx	64/32	2F0000–2FFFFF	178000–17FFFF
SA55	0110000xxx	64/32	300000–30FFFF	180000–187FFF
SA56	0110001xxx	64/32	310000–31FFFF	188000–18FFFF
SA57	0110010xxx	64/32	320000–32FFFF	190000–197FFF
SA58	0110011xxx	64/32	330000–33FFFF	198000–19FFFF
SA59	0110100xxx	64/32	340000–34FFFF	1A0000–1A7FFF
SA60	0110101xxx	64/32	350000–35FFFF	1A8000–1AFFFF
SA61	0110110xxx	64/32	360000–36FFFF	1B0000–1B7FFF
SA62	0110111xxx	64/32	370000–37FFFF	1B8000–1BFFFF
SA63	0111000xxx	64/32	380000–38FFFF	1C0000–1C7FFF
SA64	0111001xxx	64/32	390000–39FFFF	1C8000–1CFFFF
SA65	0111010xxx	64/32	3A0000–3AFFFF	1D0000–1D7FFF

SA66	0111011xxx	64/32	3B0000–3BFFFF	1D8000–1DFFFF
SA67	0111100xxx	64/32	3C0000–3CFFFF	1E0000–1E7FFF
SA68	0111101xxx	64/32	3D0000–3DFFFF	1E8000–1EFFFF
SA69	0111110xxx	64/32	3E0000–3EFFFF	1F0000–1F7FFF
SA70	0111111xxx	64/32	3F0000–3FFFFF	1F8000–1FFFFF
SA71	1000000xxx	64/32	400000–40FFFF	200000–207FFF
SA72	1000001xxx	64/32	410000–41FFFF	208000–20FFFF
SA73	1000010xxx	64/32	420000–42FFFF	210000–217FFF
SA74	1000011xxx	64/32	430000–43FFFF	218000–21FFFF
SA75	1000100xxx	64/32	440000–44FFFF	220000–227FFF
SA76	1000101xxx	64/32	450000–45FFFF	228000–22FFFF
SA77	1000110xxx	64/32	460000–46FFFF	230000–237FFF
SA78	1000111xxx	64/32	470000–47FFFF	238000–23FFFF
SA79	1001000xxx	64/32	480000–48FFFF	240000–247FFF
SA80	1001001xxx	64/32	490000–49FFFF	248000–24FFFF
SA81	1001010xxx	64/32	4A0000–4AFFFF	250000–257FFF
SA82	1001011xxx	64/32	4B0000–4BFFFF	258000–25FFFF
SA83	1001100xxx	64/32	4C0000–4CFFFF	260000–267FFF
SA84	1001101xxx	64/32	4D0000–4DFFFF	268000–26FFFF
SA85	1001110xxx	64/32	4E0000–4EFFFF	270000–277FFF
SA86	1001111xxx	64/32	4F0000–4FFFFF	278000–27FFFF
SA87	1010000xxx	64/32	500000–50FFFF	280000–287FFF
SA88	1010001xxx	64/32	510000–51FFFF	288000–28FFFF
SA89	1010010xxx	64/32	520000–52FFFF	290000–297FFF
SA90	1010011xxx	64/32	530000–53FFFF	298000–29FFFF
SA91	1010100xxx	64/32	540000–54FFFF	2A0000–2A7FFF
SA92	1010101xxx	64/32	550000–55FFFF	2A8000–2AFFFF
SA93	1010110xxx	64/32	560000–56FFFF	2B0000–2B7FFF
SA94	1010111xxx	64/32	570000–57FFFF	2B8000–2BFFFF
SA95	1011000xxx	64/32	580000–58FFFF	2C0000–2C7FFF
SA96	1011001xxx	64/32	590000–59FFFF	2C8000–2CFFFF
SA97	1011010xxx	64/32	5A0000–5AFFFF	2D0000–2D7FFF
SA98	1011011xxx	64/32	5B0000–5BFFFF	2D8000–2DFFFF
SA99	1011100xxx	64/32	5C0000–5CFFFF	2E0000–2E7FFF
SA100	1011101xxx	64/32	5D0000–5DFFFF	2E8000–2EFFFF
SA101	1011110xxx	64/32	5E0000–5EFFFF	2F0000–2F7FFF
SA102	1011111xxx	64/32	5F0000–5FFFFF	2F8000–2FFFFF
SA103	1100000xxx	64/32	600000–60FFFF	300000–307FFF
SA104	1100001xxx	64/32	610000–61FFFF	308000–30FFFF
SA105	1100010xxx	64/32	620000–62FFFF	310000–317FFF
SA106	1100011xxx	64/32	630000–63FFFF	318000–31FFFF
SA107	1100100xxx	64/32	640000–64FFFF	320000–327FFF
SA108	1100101xxx	64/32	650000–65FFFF	328000–32FFFF

SA109	1100110xxx	64/32	660000–66FFFF	330000–337FFF
SA110	1100111xxx	64/32	670000–67FFFF	338000–33FFFF
SA111	1101000xxx	64/32	680000–68FFFF	340000–347FFF
SA112	1101001xxx	64/32	690000–69FFFF	348000–34FFFF
SA113	1101010xxx	64/32	6A0000–6AFFFF	350000–357FFF
SA114	1101011xxx	64/32	6B0000–6BFFFF	358000–35FFFF
SA115	1101100xxx	64/32	6C0000–6CFFFF	360000–367FFF
SA116	1101101xxx	64/32	6D0000–6DFFFF	368000–36FFFF
SA117	1101110xxx	64/32	6E0000–6EFFFF	370000–377FFF
SA118	1101111xxx	64/32	6F0000–6FFFFF	378000–37FFFF
SA119	1110000xxx	64/32	700000–70FFFF	380000–387FFF
SA120	1110001xxx	64/32	710000–71FFFF	388000–38FFFF
SA121	1110010xxx	64/32	720000–72FFFF	390000–397FFF
SA122	1110011xxx	64/32	730000–73FFFF	398000–39FFFF
SA123	1110100xxx	64/32	740000–74FFFF	3A0000–3A7FFF
SA124	1110101xxx	64/32	750000–75FFFF	3A8000–3AFFFF
SA125	1110110xxx	64/32	760000–76FFFF	3B0000–3B7FFF
SA126	1110111xxx	64/32	770000–77FFFF	3B8000–3BFFFF
SA127	1111000xxx	64/32	780000–78FFFF	3C0000–3C7FFF
SA128	1111001xxx	64/32	790000–79FFFF	3C8000–3CFFFF
SA129	1111010xxx	64/32	7A0000–7AFFFF	3D0000–3D7FFF
SA130	1111011xxx	64/32	7B0000–7BFFFF	3D8000–3DFFFF
SA131	1111100xxx	64/32	7C0000–7CFFFF	3E0000–3E7FFF
SA132	1111101xxx	64/32	7D0000–7DFFFF	3E8000–3EFFFF
SA133	1111110xxx	64/32	7E0000–7EFFFF	3F0000–3F7FFF
SA134	1111111xxx	64/32	7F0000–7FFFFF	3F8000–3FFFFF

Note: The address bus is A21:A-1 in byte mode where BYTE# = V_{IL}, or A21:A0 in word mode where BYTE# = V_{IH}.

PRODUCT SELECTOR GUIDE

Product Number		**EN29LV640T/B**	
Speed Option	Regulated Voltage Range: Vcc=3.0 – 3.6 V	**-70**	
	Full Voltage Range: Vcc=2.7 – 3.6 V		**-90**
Max Access Time, ns (t_{acc})		70	90
Max CE# Access, ns (t_{ce})		70	90
Max OE# Access, ns (t_{oe})		30	35

BLOCK DIAGRAM

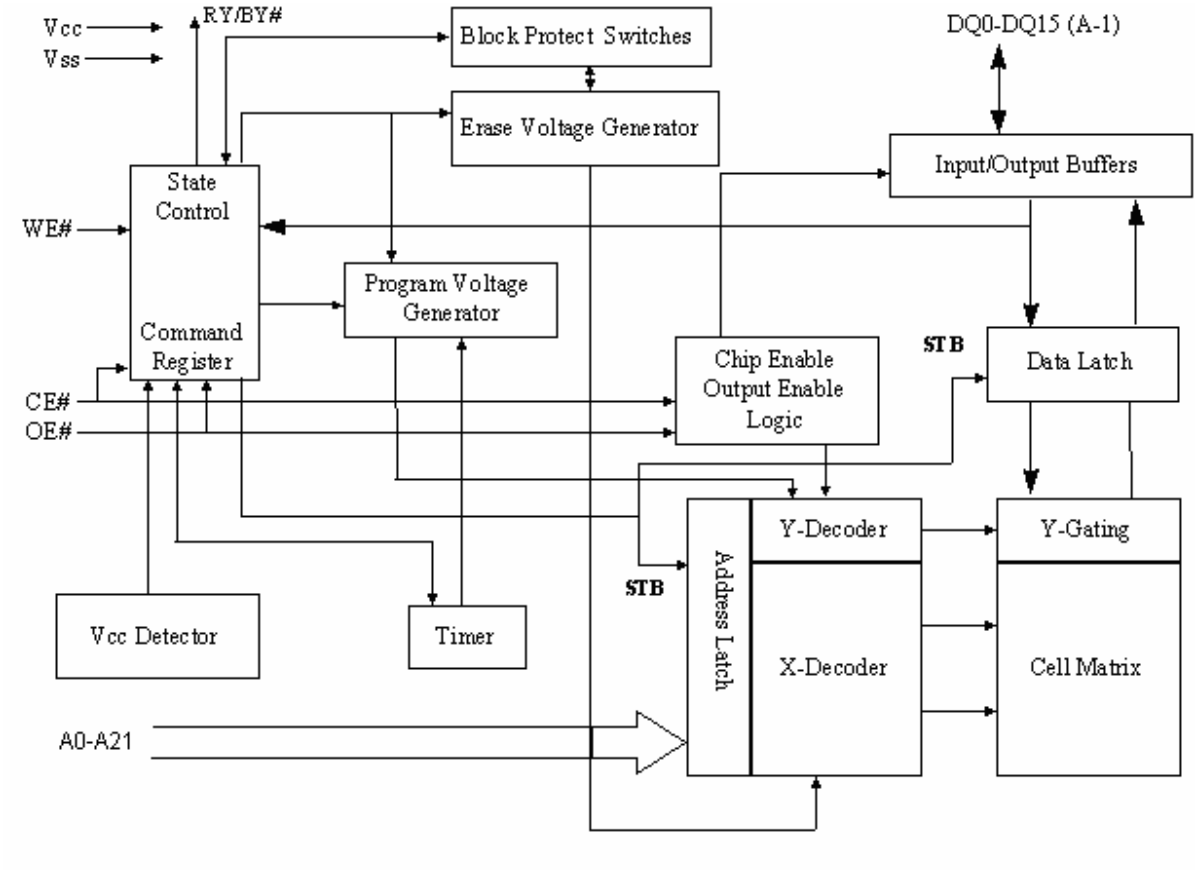


TABLE 3. OPERATING MODES

64M FLASH USER MODE TABLE

Operation	CE#	OE#	WE#	RESET #	WP#/ACC	A0-A21	DQ0-DQ7	DQ8-DQ15	
								BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8-DQ14= High-Z, DQ15 = A-1
Write	L	H	L	H	(Note 1)	A_{IN}	D_{IN}	D_{IN}	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	D_{IN}	D_{IN}	
CMOS Standby	V_{CC} ± 0.3V	X	X	V_{CC} ± 0.3V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector (Group) Protect	L	H	L	V_{ID}	L/H	SA, A6=L, A1=H, A0=L	(Note 2)	X	X
Sector Unprotect	L	H	L	V_{ID}	(Note 1)	SA, A6=H, A1=H, A0=L	(Note 2)	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 1)	A_{IN}	(Note 2)	(Note 2)	High-Z

L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} =V_{HH} =11 ± 0.5V = 10.5-11.5V, X=Don't Care (either L or H, but not floating), SA=Sector Addresses, D_{IN}=Data In, D_{OUT}=Data Out, A_{IN}=Address In

Notes:

1. If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP# / ACC = V_{IH}, the outermost boot sector protection depends on whether they were last protected or unprotected. If WP#/ACC = V_{HH}, all sectors will be unprotected.

2. Please refer to "Sector/Sector Group Protection & Chip Unprotection", Flowchart 7a and Flowchart 7b.

TABLE 4. Autoselect Codes (Using High Voltage, V_{ID})

64M FLASH MANUFACTURER/DEVICE ID TABLE

Description		CE#	OE#	WE#	A21 to A12	A11 to A10	A9[2]	A8	A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: Eon		L	L	H	X	X	V_{ID}	H[1]	X	L	X	L	L	X	1Ch
								L							7Fh
Device ID (top boot sector)	Word	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	22h	C9h
	Byte	L	L	H										X	C9h
Device ID (bottom boot sector)	Word	L	L	H	X	X	V_{ID}	X	X	L	X	L	H	22h	CBh
	Byte	L	L	H										X	CBh
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	X	L	X	H	L	X	01h (Protected)
														X	00h (Unprotected)

L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} =11 ± 0.5V, X=Don't Care (either L or H, but not floating!), SA=Sector Addresses

Note:

1. A8=H is recommended for Manufacturing ID check. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 = V_{ID} is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.

USER MODE DEFINITIONS

Word / Byte Configuration

The signal set on the BYTE# pin controls whether the device data I/O pins DQ15-DQ0 operate in the byte or word configuration. When the BYTE# Pin is set at logic '1', then the device is in word configuration, DQ15-DQ0 are active and are controlled by CE# and OE#.

On the other hand, if the BYTE# Pin is set at logic '0', then the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Standby Mode

The EN29LV640T/B has a CMOS-compatible standby mode, which reduces the current to < 1µA (typical). It is placed in CMOS-compatible standby when the CE# pin is at $V_{CC} \pm 0.5$. RESET# and BYTE# pin must also be at CMOS input levels. The device also has a TTL-compatible standby mode, which reduces the maximum V_{CC} current to < 1mA. It is placed in TTL-compatible standby when the CE# pin is at V_{IH}. When in standby modes, the outputs are in a high-impedance state independent of the OE# input.

Automatic Sleep Mode

The EN29LV640T/B has an automatic sleep mode, which minimizes power consumption. The devices will enter this mode automatically when the states of address bus remain stable for t_{acc} + 30ns. I_{CC4} in the DC Characteristics table shows the current specification. With standard access times, the device will output new data when addresses change.

Read Mode

The device is automatically set to reading array data after device power-up or hardware reset. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm

After the device accepts a Sector Erase Suspend command, the device enters the Sector Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Sector Erase Suspend mode, the system may once again read array data with the same exception. See "Sector Erase Suspend/Resume Commands" for more additional information.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high or while in the autoselect mode. See the "Reset Command" for additional details.

Output Disable Mode

When the OE# pin is at a logic high level (V_{IH}), the output from the EN29LV640T/B is disabled. The output pins are placed in a high impedance state.

Autoselect Identification Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (10.5 V to 11.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The “Command Definitions” table shows the remaining address bits that are don’t-care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See “Command Definitions” for details on using the autoselect mode.

Writing Command Sequences

To write a command or command sequence to program data to the device or erase data, the system has to drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. An erase operation can erase one sector or the whole chip.

The system can also read the autoselect codes by entering the autoselect mode, which need the autoselect command sequence to be written. Please refer to the “Command Definitions” for all the available commands.

RESET#: Hardware Reset

When RESET# is driven low for t_{RP}, all output pins are tristates. All commands written in the internal state machine are reset to reading array data.

Please refer to timing diagram for RESET# pin in “AC Characteristics”.

Sector/Sector Group Protection & Chip Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector. The hardware chip unprotection feature re-enables both program and erase operations in previously protected sectors. A sector group implies three or four adjacent sectors that would be protected at the same time. Please see the following tables which show the organization of sector groups.

There are two methods to enable this hardware protection circuitry. The first one requires only that the RESET# pin be at V_{ID} and then standard microprocessor timings can be used to enable or disable this feature. See Flowchart 7a and 7b for the algorithm and Figure. 12 for the timings.
When doing Chip Unprotect, all the unprotected sector groups must be protected prior to any unprotect write cycle.

The second method is for programming equipment. This method requires V_{ID} to be applied to both OE# and A9 pins and non-standard microprocessor timings are used. This method is described in a separate document named EN29LV640T/B Supplement, which can be obtained by contacting a representative of Eon Silicon Solution, Inc.

Top Boot Sector/Sector Group Organization Table (EN29LV640T) for (Un)Protection

Sector Group	Sectors	A21-A12	Sector Group Size
SG 0	SA 0-SA 3	00000XXXXX	64 Kbytes x 4
SG 1	SA 4-SA 7	00001XXXXX	64 Kbytes x 4
SG 2	SA 8-SA 11	00010XXXXX	64 Kbytes x 4
SG 3	SA 12-SA 15	00011XXXXX	64 Kbytes x 4
SG 4	SA 16-SA 19	00100XXXXX	64 Kbytes x 4
SG 5	SA 20-SA 23	00101XXXXX	64 Kbytes x 4
SG 6	SA 24-SA 27	00110XXXXX	64 Kbytes x 4
SG 7	SA 28-SA 31	00111XXXXX	64 Kbytes x 4
SG 8	SA 32-SA 35	01000XXXXX	64 Kbytes x 4
SG 9	SA 36-SA 39	01001XXXXX	64 Kbytes x 4
SG10	SA 40-SA 43	01010XXXXX	64 Kbytes x 4
SG11	SA 44-SA 47	01011XXXXX	64 Kbytes x 4
SG12	SA 48-SA 51	01100XXXXX	64 Kbytes x 4
SG13	SA 52-SA 55	01101XXXXX	64 Kbytes x 4
SG14	SA 56-SA 59	01110XXXXX	64 Kbytes x 4
SG15	SA 60-SA 63	01111XXXXX	64 Kbytes x 4
SG16	SA 64-SA 67	10000XXXXX	64 Kbytes x 4
SG17	SA 68-SA 71	10001XXXXX	64 Kbytes x 4
SG18	SA 72-SA 75	10010XXXXX	64 Kbytes x 4
SG19	SA 76-SA 79	10011XXXXX	64 Kbytes x 4
SG20	SA 80-SA 83	10100XXXXX	64 Kbytes x 4
SG21	SA 84-SA 87	10101XXXXX	64 Kbytes x 4
SG22	SA 88-SA 91	10110XXXXX	64 Kbytes x 4
SG23	SA 92-SA 95	10111XXXXX	64 Kbytes x 4
SG24	SA 96-SA 99	11000XXXXX	64 Kbytes x 4
SG25	SA100-SA103	11001XXXXX	64 Kbytes x 4
SG26	SA104-SA107	11010XXXXX	64 Kbytes x 4
SG27	SA108-SA111	11011XXXXX	64 Kbytes x 4
SG28	SA112-SA115	11100XXXXX	64 Kbytes x 4
SG29	SA116-SA119	11101XXXXX	64 Kbytes x 4
SG30	SA120-SA123	11110XXXXX	64 Kbytes x 4
SG31	SA124-SA126	1111100XXX 1111101XXX 1111110XXX	64 Kbytes x 3
SG32	SA127	1111111000	8 Kbytes
SG33	SA128	1111111001	8 Kbytes
SG34	SA129	1111111010	8 Kbytes
SG35	SA130	1111111011	8 Kbytes
SG36	SA131	1111111100	8 Kbytes
SG37	SA132	1111111101	8 Kbytes
SG38	SA133	1111111110	8 Kbytes
SG39	SA134	1111111111	8 Kbytes

Bottom Boot Sector/Sector Group Organization Table (EN29LV640B) for (Un)Protection

Sector Group	Sectors	A21-A12	Sector Group Size
SG39	SA134-SA131	11111XXXXX	64 Kbytes x 4
SG38	SA130-SA127	11110XXXXX	64 Kbytes x 4
SG37	SA126-SA123	11101XXXXX	64 Kbytes x 4
SG36	SA122-SA119	11100XXXXX	64 Kbytes x 4
SG35	SA118-SA115	11011XXXXX	64 Kbytes x 4
SG34	SA114-SA111	11010XXXXX	64 Kbytes x 4
SG33	SA110-SA107	11001XXXXX	64 Kbytes x 4
SG32	SA106-SA103	11000XXXXX	64 Kbytes x 4
SG31	SA102-SA 99	10111XXXXX	64 Kbytes x 4
SG30	SA 98-SA 95	10110XXXXX	64 Kbytes x 4
SG29	SA 94-SA 91	10101XXXXX	64 Kbytes x 4
SG28	SA 90-SA 87	10100XXXXX	64 Kbytes x 4
SG27	SA 86-SA 83	10011XXXXX	64 Kbytes x 4

SG26	SA 82-SA 79	10010XXXXX	64 Kbytes x 4
SG25	SA 78-SA 75	10001XXXXX	64 Kbytes x 4
SG24	SA 74-SA 71	10000XXXXX	64 Kbytes x 3
SG23	SA 70-SA 67	01111XXXXX	64 Kbytes x 4
SG22	SA 66-SA 63	01110XXXXX	64 Kbytes x 4
SG21	SA 62-SA 59	01101XXXXX	64 Kbytes x 4
SG20	SA 58-SA 55	01100XXXXX	64 Kbytes x 4
SG19	SA 54-SA 51	01011XXXXX	64 Kbytes x 4
SG18	SA 50-SA 47	01010XXXXX	64 Kbytes x 4
SG17	SA 46-SA 43	01001XXXXX	64 Kbytes x 4
SG16	SA 42-SA 39	01000XXXXX	64 Kbytes x 4
SG15	SA 38-SA 35	00111XXXXX	64 Kbytes x 4
SG14	SA 34-SA 31	00110XXXXX	64 Kbytes x 4
SG13	SA 30-SA 27	00101XXXXX	64 Kbytes x 4
SG12	SA 26-SA 23	00100XXXXX	64 Kbytes x 4
SG11	SA 22-SA 19	00011XXXXX	64 Kbytes x 4
SG10	SA 18-SA 15	00010XXXXX	64 Kbytes x 4
SG 9	SA 14-SA 11	00001XXXXX	64 Kbytes x 4
SG 8	SA 10-SA 8	0000011XXX 0000010XXX 0000001XXX	64 Kbytes x 3
SG 7	SA 7	0000000111	8 Kbytes
SG 6	SA 6	0000000110	8 Kbytes
SG 5	SA 5	0000000101	8 Kbytes
SG 4	SA 4	0000000100	8 Kbytes
SG 3	SA 3	0000000011	8 Kbytes
SG 2	SA 2	0000000010	8 Kbytes
SG 1	SA 1	0000000001	8 Kbytes
SG 0	SA 0	0000000000	8 Kbytes

Write Protect / Accelerated Program (WP# / ACC)

The WP#/ACC pin provides two functions. The Write Protect (WP#) function provides a hardware method of protecting the outermost two 8K-byte Boot Sector. The ACC function allows faster manufacturing throughput at the factory, using an external high voltage.

When WP#/ACC is Low, the device protects the outermost two 8K-byte Boot Sector; no matter the sectors are protected or unprotected using the method described in “Sector/Sector Group Protection & Chip Unprotection”, Program and Erase operations in these sectors are ignored.

When WP#/ACC is High, the device reverts to the previous protection status of the outermost two 8K-byte boot sector. Program and Erase operations can now modify the data in the two outermost 8K-byte Boot Sector unless the sector is protected using Sector Protection.

When WP#/ACC is raised to V_{HH} the memory automatically enters the Accelerated Program mode, this mode permit the system to skip the normal command unlock sequences and program byte/word locations directly to reduces the time required for program operation. When WP#/ACC returns to V_{IH} or V_{IL} normal operation resumes. The transitions from V_{IH} or V_{IL} to V_{HH} and from V_{HH} to V_{IH} or V_{IL} must be slower than tB_{VHHB}, see Figure 11.

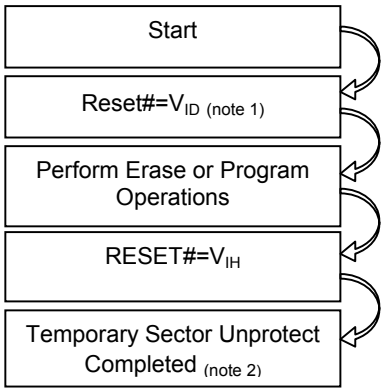
Note that the WP#/ACC pin must not be left floating or unconnected. In addition, WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming. It could cause the device to be damaged.

Never raise this pin to V_{HH} from any mode except Read mode. Otherwise the memory may be left in an indeterminate state.

A 0.1µF capacitor should be connected between the WP#/ACC pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Accelerated Program mode.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data while in-system. The Temporary Sector Unprotect mode is activated by setting the RESET# pin to VBIDB. During this mode, formerly protected sectors can be programmed or erased by simply selecting the sector addresses. Once VBIDB is removed from the RESET# pin, all the previously protected sectors are protected again. See accompanying flowchart and figure 10 for more timing details.



Notes:
1. All protected sectors are unprotected. (If WP#/ACC=V_{IL}, outermost boot sectors will remain protected.)
2. Previously protected sectors are protected again.

COMMON FLASH INTERFACE (CFI)

The common flash interface (CFI) specification outlines device and host systems software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data.

The system can read CFI information at the addresses given in Tables 5-8.In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode and the system can read CFI data at the addresses given in Tables 5–8. The system must write the reset command to return the device to the autoselect mode.

Table 5. CFI Query Identification String

Addresses (Word Mode)	Adresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 6. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	Vcc Min (write/erase) DQ7-DQ4: volt, DQ3 –DQ0: 100 millivolt
1Ch	38h	0036h	Vcc Max (write/erase) DQ7-DQ4: volt, DQ3 –DQ0: 100 millivolt
1Dh	3Ah	0000h	Vpp Min. voltage (00h = no Vpp pin present)
1Eh	3Ch	0000h	Vpp Max. voltage (00h = no Vpp pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N S
20h	40h	0000h	Typical timeout for Min, size buffer write 2^N S (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max timeout for full chip erase 2^N times typical (00h = not supported)

Table 7. Device Geometry Definition

Addresses (Word mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0017h	Device Size = 2^N bytes
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification of CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	007Eh 0000h 0000h 0001h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 8. Primary Vendor-specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0031h	Minor version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock 0 = Required, 1 = Not Required
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0004h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 01 = 29F040 mode, 02 = 29F016 mode, 03 = 29F400 mode, 04 = 29LV800A mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, 01 = Supported
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00A5h	Minimum ACC (Acceleration) Supply Voltage 00 = Not Supported, DQ7-DQ4 : Volts, DQ3-DQ0 : 100mV
4Eh	9Ch	00C5h	Maximum ACC (Acceleration) Supply Voltage 00 = Not Supported, DQ7-DQ4 : Volts, DQ3-DQ0 : 100mV
4Fh	9Eh	0002h/ 0003h	Top/Bottom Boot Sector Identifier 02h = Bottom Boot, 03h = Top Boot

Hardware Data protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes as seen in the Command Definitions table. Additionally, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by false system level signals during Vcc power up and power down transitions, or from system noise.

Low V_{CC} Write Inhibit

When Vcc is less than V_{LKO}, the device does not accept any write cycles. This protects data during Vcc power up and power down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until Vcc is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when Vcc is greater than V_{LKO}.

Write Pulse "Glitch" protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one. If CE#, WE#, and OE# are all logical zero (not recommended usage), it will be considered a read.

Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with CE# = V_{IL}, WE#= V_{IL} and OE# = V_{IH}, the device will not accept commands on the rising edge of WE#.

COMMAND DEFINITIONS

The operations of the device are selected by one or more commands written into the command register. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Definitions table (Table 9). Incorrect addresses, incorrect data values or improper sequences will reset the device to Read Mode.

Table 9. EN29LV640T/B Command Definitions

Command Sequence			Cycles	Bus Cycles											
				1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	xxx	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000	7F				
										100	1C				
		Byte		AAA		555		AAA		000	7F				
										200	1C				
	Device ID Top Boot	Word	4	555	AA	2AA	55	555	90	x01	22C9				
		Byte		AAA		555		AAA		x02	C9				
	Device ID Bottom Boot	Word	4	555	AA	2AA	55	555	90	x01	22CB				
		Byte		AAA		555		AAA		x02	CB				
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA) X02	00				
											01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Sector Erase Suspend			1	xxx	B0										
Sector Erase Resume			1	xxx	30										
CFI Query		Word	1	55	98										
		Byte		AA											

Address and Data values indicated are in hex. Unless specified, all bus cycles are write cycles
RA = Read Address: address of the memory location to be read. This is a read cycle.
RD = Read Data: data read from location RA during Read operation. This is a read cycle.
PA = Program Address: address of the memory location to be programmed. X = Don't-Care
PD = Program Data: data to be programmed at location PA
SA = Sector Address: address of the Sector to be erased or verified. Address bits A20-A12 uniquely select any Sector.

Notes:
1. The data is 00H for an unprotected sector/sector block and 01H for a protected sector/sector block.
2. The data is 88H for factory locked and 08H for not factory locked.

Reading Array Data

The device is automatically set to reading array data after power up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

Following a Sector Erase Suspend command, Sector Erase Suspend mode is entered. The system can read array data using the standard read timings from sectors other than the one which is being erase-suspended. If the system reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Sector Erase Suspend mode, the system may once again read array data with the same exception.

The Reset command must be issued to re-enable the device for reading array data if DQ5 goes high during an active program or erase operation or while in the autoselect mode. See next section for details on Reset.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't-care for this command.

The reset command may be written between the cycle sequences in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Sector Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the cycle sequences in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies in Sector Erase Suspend mode).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices ID codes, and determine whether or not a sector (group) is protected. The Command Definitions table shows the address and data requirements. This is an alternative to the method that requires V_{ID} on address bit A9 and is intended for commercial programmers.

Two unlock cycles followed by the autoselect command initiate the autoselect command sequence. Autoselect mode is then entered and the system may read at addresses shown in Table 9 any number of times, without needing another command sequence.

The system **must write the reset command** to exit the autoselect mode and return to reading array data.

Word / Byte Programming Command

The device can be programmed by byte or by word, depending on the state of the BYTE# Pin. Programming the EN29LV640T/B is performed by using a four-bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of CE# or WE#, whichever is last; data is latched on the rising edge of CE# or WE#, whichever is first.

Any commands written to the device during the program operation are ignored. Programming status can be checked by sampling data on DQ7 (DATA# polling) or on DQ6 (toggle bit). When the program operation is successfully completed, the device returns to read mode and the user can read the data programmed to the device at that address. Note that data can not be programmed from a “0” to a “1”. Attempting to do so may halt the operation and set DQ5 to “1”, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”. When programming time limit is exceeded, DQ5 will produce a logical “1” and a Reset command can return the device to Read mode.

Programming is allowed in any sequence across sector boundaries.

Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Chip Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Sector Erase Suspend command is valid. All other commands are ignored. If there are several sectors to be erased, Sector Erase Command sequences must be issued for each sector. That is, only **a sector address can be specified for each Sector Erase command**. Users must issue another Sector Erase command for the next sector to be erased after the previous one is completed.

When the Embedded Erase algorithm is completed, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Sector Erase Suspend / Resume Command

The Sector Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation. The Sector Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don’t-cares when writing the Sector Erase Suspend command.

When the Sector Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 μs to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. Normal read and write timings and command definitions apply. Please note that **Autoselect command sequence can not be accepted during Sector Erase Suspend**.

Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information. The Autoselect command is not supported during Sector Erase Suspend Mode.

The system must write the Sector Erase Resume command (address bits are don’t-care) to exit the sector erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Sector Erase Suspend command can be written after the device has resumed erasing.

WRITE OPERATION STATUS

DQ7: DATA# Polling

The EN29LV640T/B provides DATA# polling on DQ7 to indicate the status of the embedded operations. The DATA# Polling feature is active during the Word/Byte Programming, Sector Erase, Chip Erase, and Sector Erase Suspend. (See Table 10)

When the embedded programming is in progress, an attempt to read the device will produce the complement of the data written to DQ7. Upon the completion of the programming operation, an attempt to read the device will produce the true data written to DQ7. DATA# polling is valid after the rising edge of the fourth WE# or CE# pulse in the four-cycle sequence for program.

When the embedded Erase is in progress, an attempt to read the device will produce a “0” at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the “1” at the DQ7 output during the read cycles. For Chip Erase or Sector Erase, DATA# polling is valid after the rising edge of the last WE# or CE# pulse in the six-cycle sequence.

DATA# Polling must be performed at any address within a sector that is being programmed or erased and not a protected sector. Otherwise, DATA# polling may give an inaccurate result if the address used is in a protected sector.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable (OE#) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on the time the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operation and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 should be read on the subsequent read attempts.

The flowchart for DATA# Polling (DQ7) is shown on Flowchart 5. The DATA# Polling (DQ7) timing diagram is shown in Figure 6.

RY/BY#: Ready/Busy Status output

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or completed. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to Vcc.

In the output-low period, signifying Busy, the device is actively erasing or programming. This includes programming in the Erase Suspend mode. If the output is high, signifying the Ready, the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

DQ6: Toggle Bit I

The EN29LV640T/B provides a "Toggle Bit" on DQ6 to indicate the status of the embedded programming and erase operations. (See Table 10)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by active OE# or CE#) will result in DQ6 toggling between "zero" and "one". Once the embedded Program or Erase operation is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During Programming, the Toggle Bit is valid after the rising edge of the fourth WE# pulse in the four-cycle sequence. During Erase operation, the Toggle Bit is valid after the rising edge of the sixth WE# pulse for sector erase or chip erase.

In embedded programming, if the sector being written to is protected, DQ6 will toggles for about 2 μs, then stop toggling without the data in the sector having changed. In Sector Erase or Chip Erase, if all selected sectors are protected, DQ6 will toggle for about 100 μs. The chip will then return to the read mode without changing data in all protected sectors.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 7.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed. Since it is possible that DQ5 can become a 1 when the device has successfully completed its operation and has returned to read mode, the user must check again to see if the DQ6 is toggling after detecting a "1" on DQ5.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1." Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the output on DQ3 can be checked to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) When sector erase starts, DQ3 switches from "0" to "1". This device does not support multiple sector erase (continuous sector erase) command sequences so it is not very meaningful since it immediately shows as a "1" after the first 30h command. Future devices may support this feature.

DQ2: Erase Toggle Bit II

The "Toggle Bit" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to the following table to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section “DQ2: Toggle Bit” explains the algorithm. See also the “DQ6: Toggle Bit I” subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, after the initial two read cycles, the system determines that the toggle bit is still toggling. And the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

Write Operation Status

Operation		DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend Program	DQ7#	Toggle	0	N/A	N/A	0

Table 10. Status Register Bits

DQ	Name	Logic Level	Definition
7	DATA# POLLING	'1'	Erase Complete or erased sector in Sector Erase Suspend
		'0'	Erase On-Going
		DQ7	Program Complete or data of non-erased sector during Sector Erase Suspend
		DQ7#	Program On-Going
6	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Erase or Program On-going
		DQ6	Read during Sector Erase Suspend
		'-1-1-1-1-1-1-1-'	Erase Complete
5	TIME OUT BIT	'1'	Program or Erase Error
		'0'	Program or Erase On-going
3	ERASE TIME OUT BIT	'1'	Erase operation start
		'0'	Erase timeout period on-going
2	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Chip Erase, Sector Erase or Read within Erase-Suspended sector. (When DQ5=1, Erase Error due to currently addressed Sector or Program on Erase-Suspended sector
		DQ2	Read on addresses of non Erase-Suspend sectors

Notes:

DQ7: DATA# Polling: indicates the P/E status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6: Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

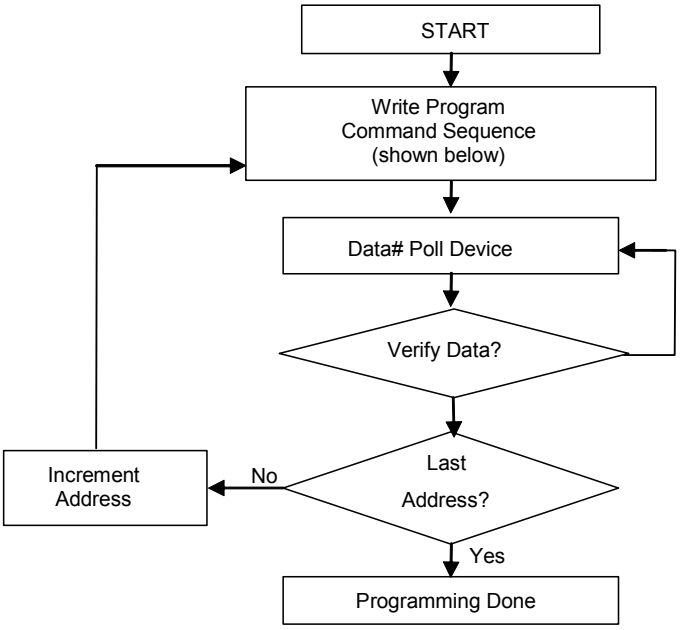
DQ5: Tim Out Bit: set to "1" if failure in programming or erase

DQ3: Sector Erase Command Timeout Bit: Operation has started. Only possible command is Erase suspend (ES).

DQ2: Toggle Bit: indicates the Erase status and allows identification of the erased Sector.

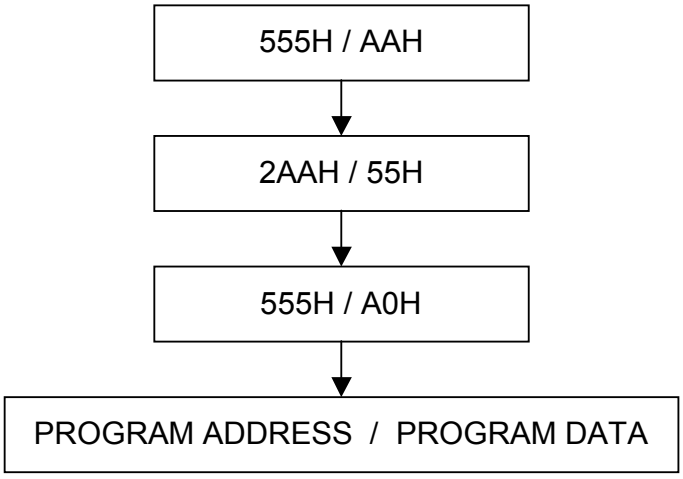
EMBEDDED ALGORITHMS

Flowchart 1. Embedded Program

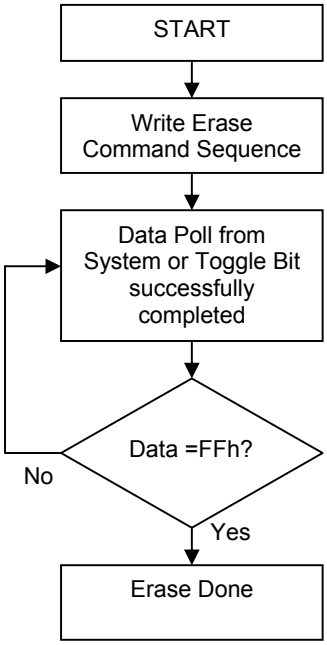


Flowchart 2. Embedded Program Command Sequence

(See the Command Definitions section for more information.)

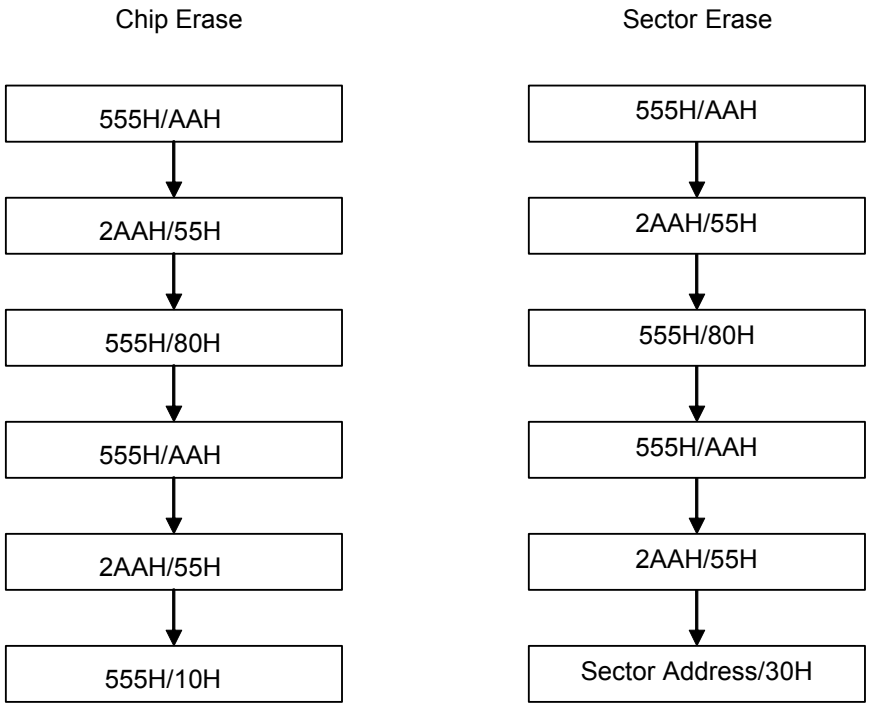


Flowchart 3. Embedded Erase

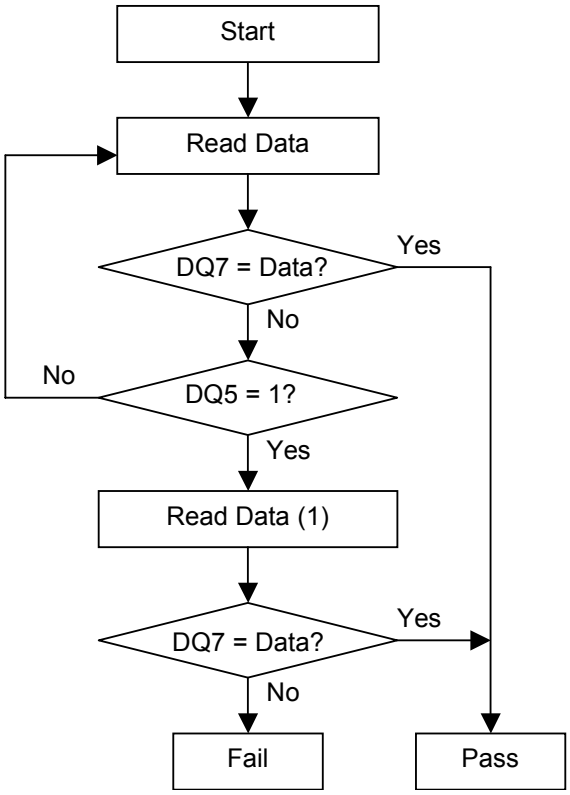


Flowchart 4. Embedded Erase Command Sequence

(See the Command Definitions section for more information.)

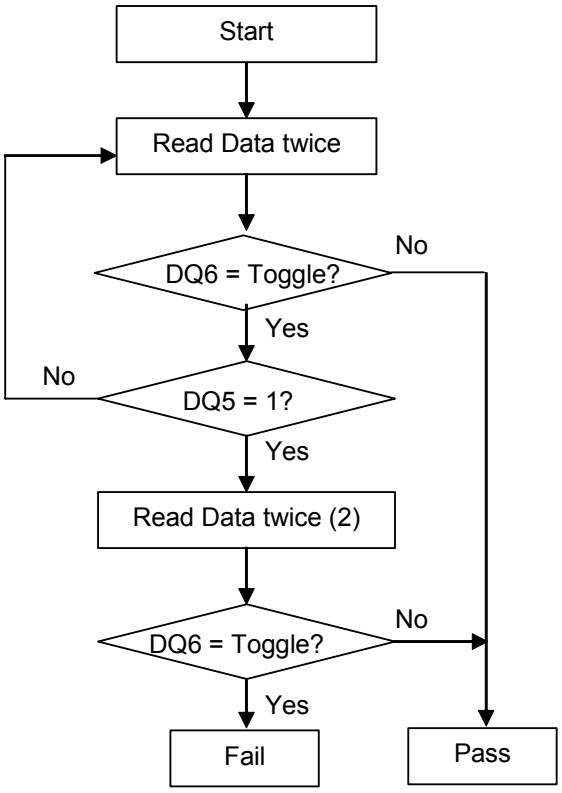


Flowchart 5. DATA# Polling Algorithm



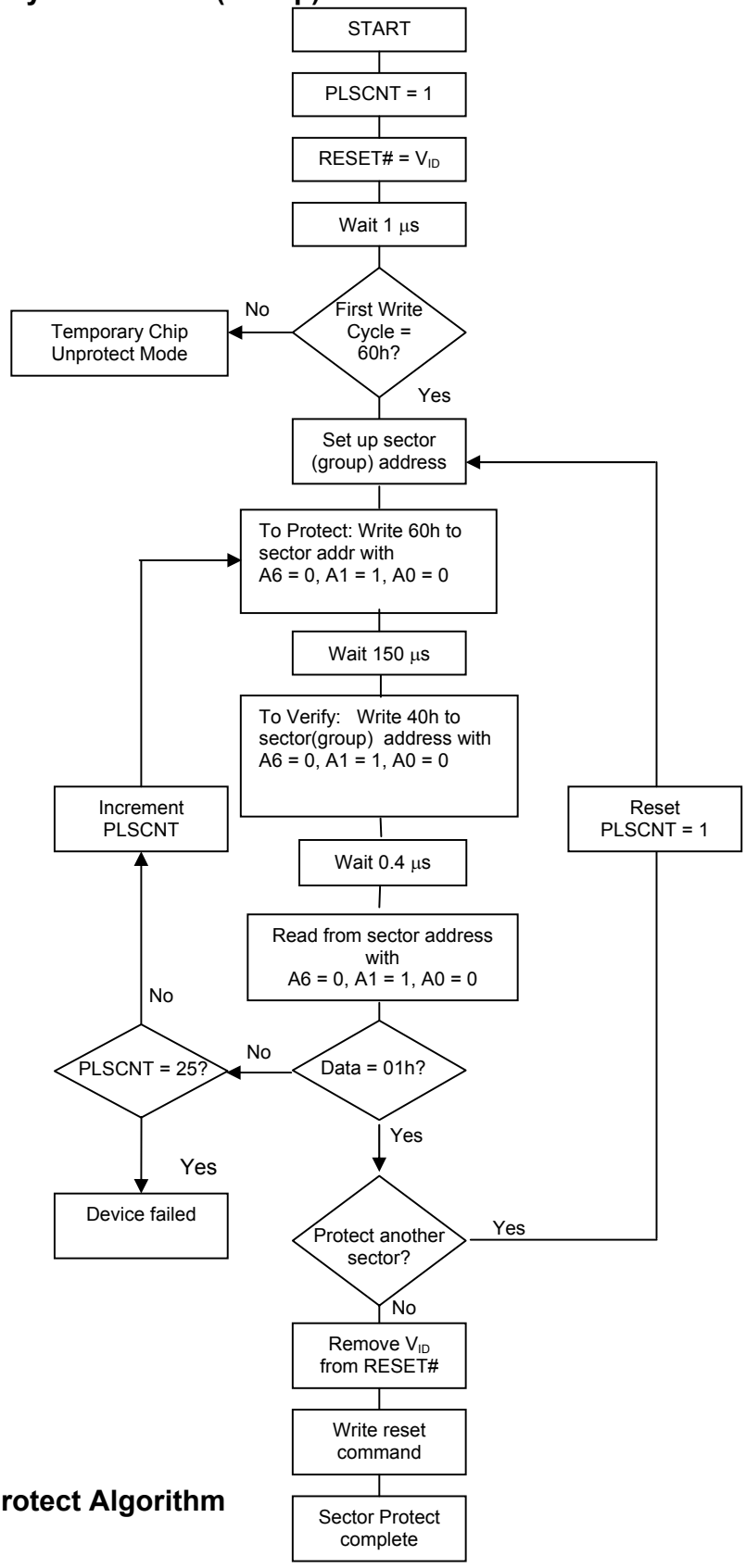
Notes:
(1) This second read is necessary in case the first read was done at the exact instant when the status data was in transition.

Flowchart 6. Toggle Bit Algorithm



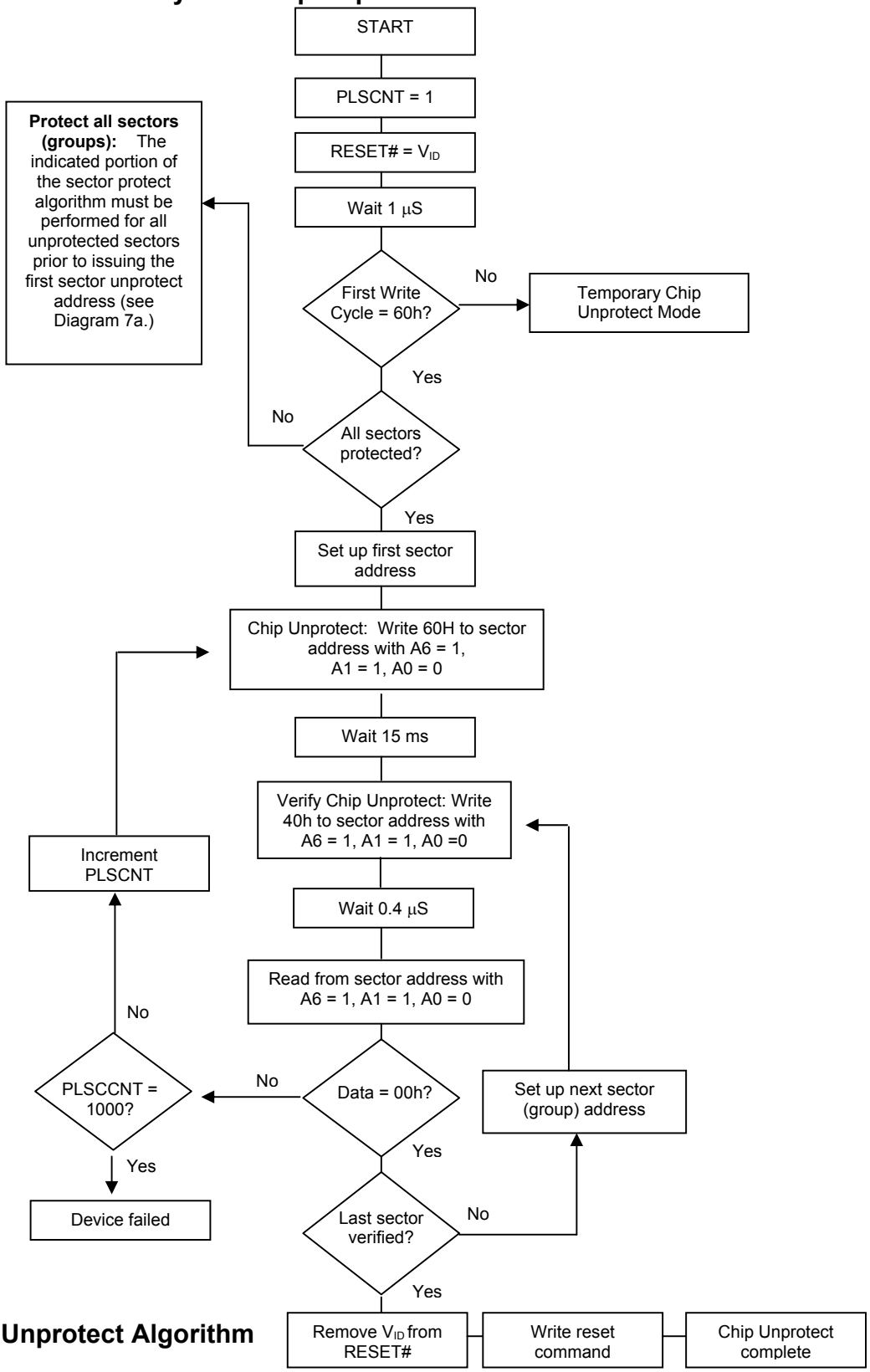
Notes:
(2) This second set of reads is necessary in case the first set of reads was done at the exact instant when the status data was in transition.

Flowchart 7a. In-System Sector (Group) Protect Flowchart



Sector Protect Algorithm

Flowchart 7b. In-System Chip Unprotect Flowchart



Chip Unprotect Algorithm

ABSOLUTE MAXIMUM RATINGS

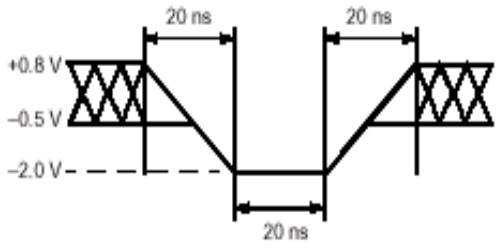
Parameter		Value	Unit
Storage Temperature		-65 to +150	℃
Plastic Packages		-65 to +125	℃
Ambient Temperature With Power Applied		-55 to +125	℃
Output Short Circuit Current[1]		200	mA
Voltage with Respect to Ground	A9, OE#, RESET# and WP#/ACC[2]	-0.5 to +11.5	V
	All other pins[3]	-0.5 to Vcc+0.5	V
	Vcc	-0.5 to + 4.0	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on A9, OE#, RESET# and WP#/ACC pins is –0.5V. During voltage transitions, A9, OE#, RESET# and WP#/ACC pins may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9, OE#, and RESET# is 11.5V which may overshoot to 12.5V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

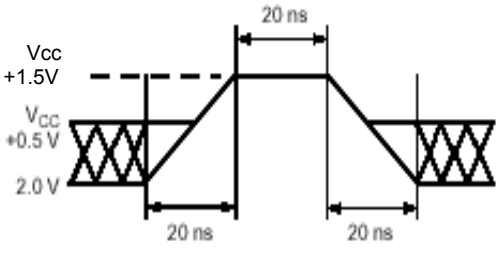
RECOMMENDED OPERATING RANGES[1]

Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	℃
Operating Supply Voltage Vcc	Full Voltage Range: 2.7 to 3.6V	V

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

DC Characteristics

Table 11. DC Characteristics

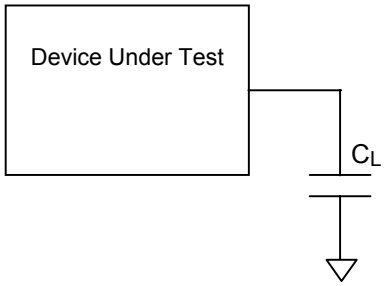
(T_a = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	0V≤ V_{IN} ≤ Vcc			±5	µA
I_{LO}	Output Leakage Current	0V≤ V_{OUT} ≤ Vcc			±5	µA
I_{CC1}	Supply Current (read) CMOS Byte	CE# = V_{IL} ; OE# = V_{IH} ; f = 5MHZ		9	16	mA
	(read) CMOS Word			9	16	mA
I_{CC2}	Supply Current (Program or Erase)	CE# = V_{IL}, OE# = V_{IH} , WE# = V_{IL}		20	30	mA
I_{CC3}	Supply Current (Standby - CMOS)	CE# = BYTE# = RESET# = Vcc ± 0.3V (Note 1)		1	5.0	µA
I_{CC4}	Reset Current	RESET# = Vss ± 0.3V		1	5.0	mA
I_{CC5}	Automatic Sleep Mode	V_{IH} = Vcc ± 0.3V V_{IL} = Vss ± 0.3V		1	5.0	uA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		0.7 x Vcc		Vcc ± 0.3	V
V_{HH}	#WP/ACC Voltage (Write Protect / Program Acceleration)		10.5		11.5	V
V_{ID}	Voltage for Autoselect or Temporary Sector Unprotect		10.5		11.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA			0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = -100 µA,	Vcc - 0.4V			V
V_{LKO}	Supply voltage (Erase and Program lock-out)		2.3		2.5	V

Notes:

1. BYTE# pin can also be GND ± 0.3V. BYTE# and RESET# pin input buffers are always enabled so that they draw power if not at full CMOS supply voltages.
2. Maximum I_{CC} specifications are tested with Vcc = Vcc max.

Test Conditions



Test Specifications

Test Conditions	-70	-90	Unit
Output Load Capacitance, C_L	30	100	pF
Input Rise and Fall times	5	5	ns
Input Pulse Levels	0.0-3.0	0.0-3.0	V
Input timing measurement reference levels	1.5	1.5	V
Output timing measurement reference levels	1.5	1.5	V

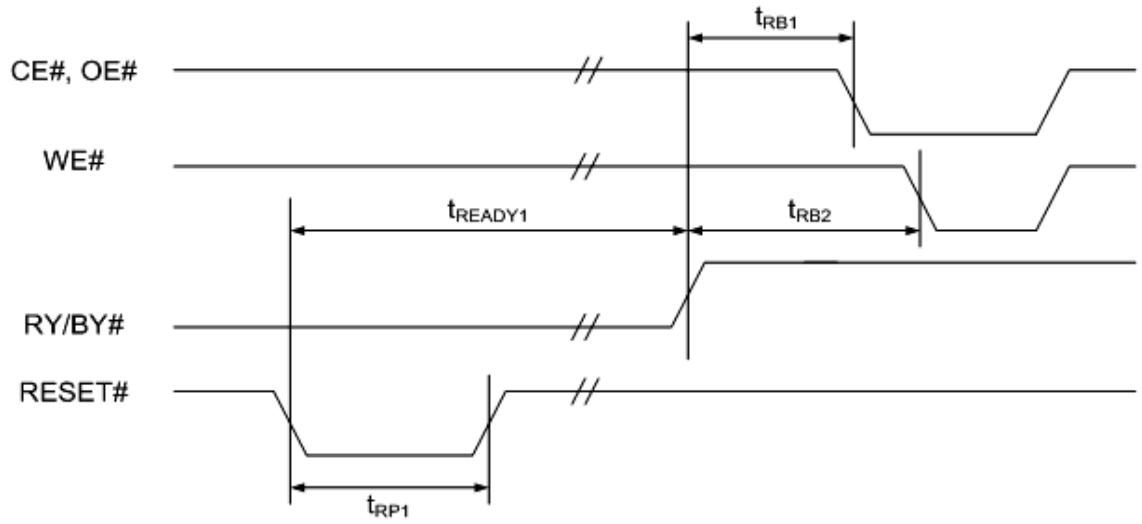
AC CHARACTERISTICS

Hardware Reset (RESET#)

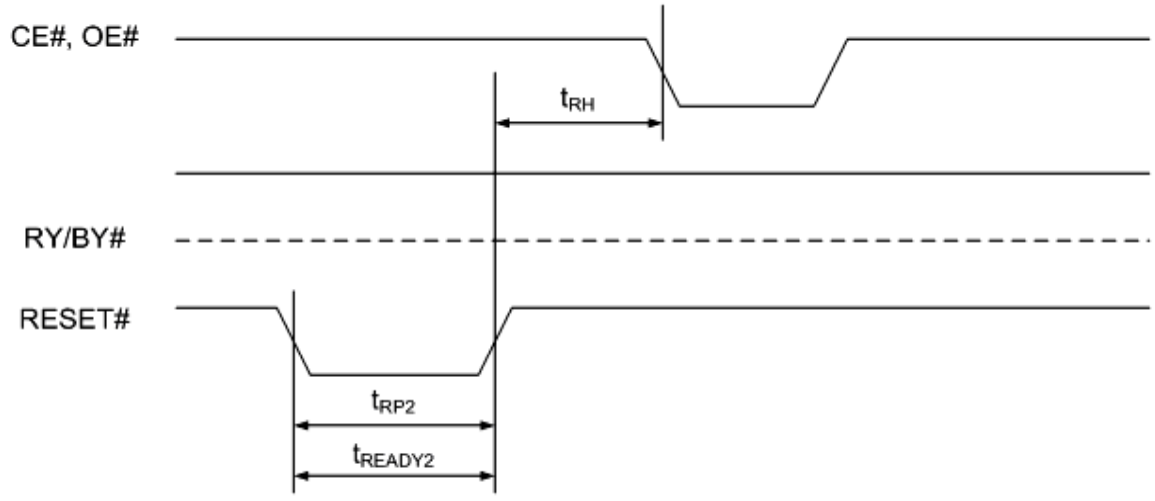
Parameter Std	Description	Test Setup	Speed		Unit
			-70	-90	
t_{RP1}	RESET# Pulse Width (During Embedded Algorithms)	Min	10		us
t_{RP2}	RESET# Pulse Width (NOT During Embedded Algorithms)	Min	500		ns
t_{RH}	Reset# High Time Before Read	Min	50		ns
t_{RB1}	RY/BY# Recovery Time (to CE#, OE# go low)	Min	0		ns
t_{RB2}	RY/BY# Recovery Time (to WE# go low)	Min	50		ns
t_{READY1}	Reset# Pin Low (During Embedded Algorithms) to Read or Write	Max	20		us
t_{READY2}	Reset# Pin Low (NOT During Embedded Algorithms) to Read or Write	Max	500		ns

Figure 1. AC Waveforms for RESET#

Reset# Timings



Reset Timing during Embedded Algorithms



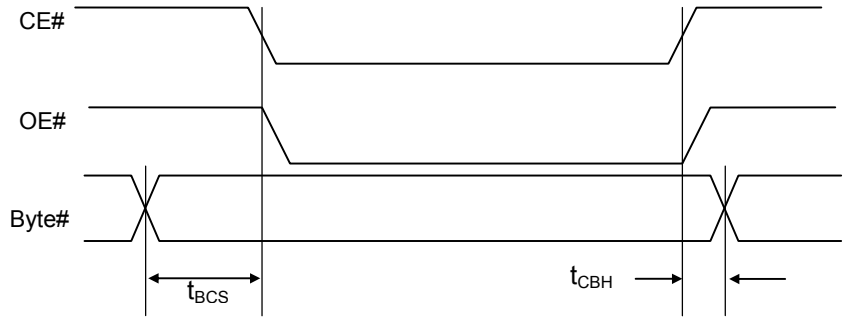
Reset Timing NOT during Embedded Algorithms

AC CHARACTERISTICS

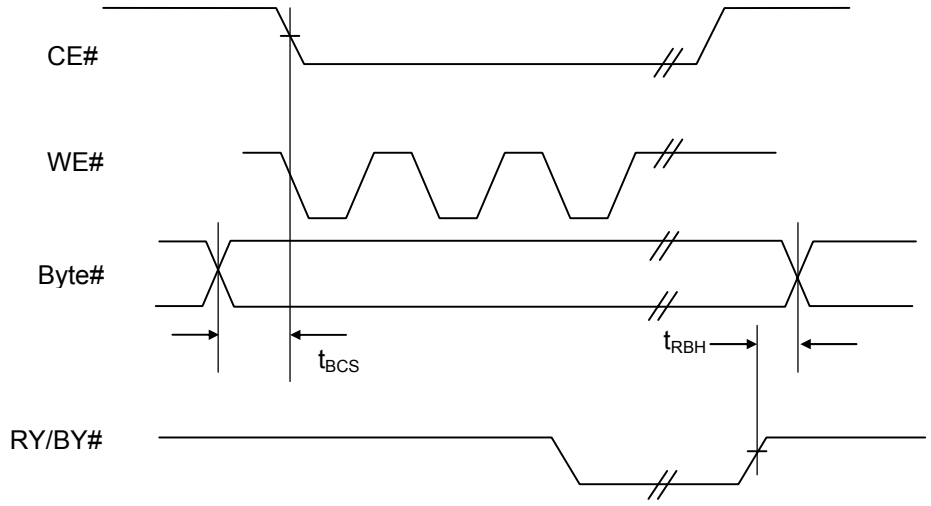
Word / Byte Configuration (BYTE#)

Std Parameter	Description		Speed		Unit
			-70	-90	
t_{BCS}	BYTE# to CE# switching setup time	Min	0	0	ns
t_{CBH}	CE# to BYTE# switching hold time	Min	0	0	ns
t_{RBH}	RY/BY# to BYTE# switching hold time	Min	0	0	ns

Figure 2. AC Waveforms for BYTE#



Byte# timings for Read Operations



Byte #timings for Write Operations

Note: Switching BYTE# pin not allowed during embedded operations

AC CHARACTERISTICS

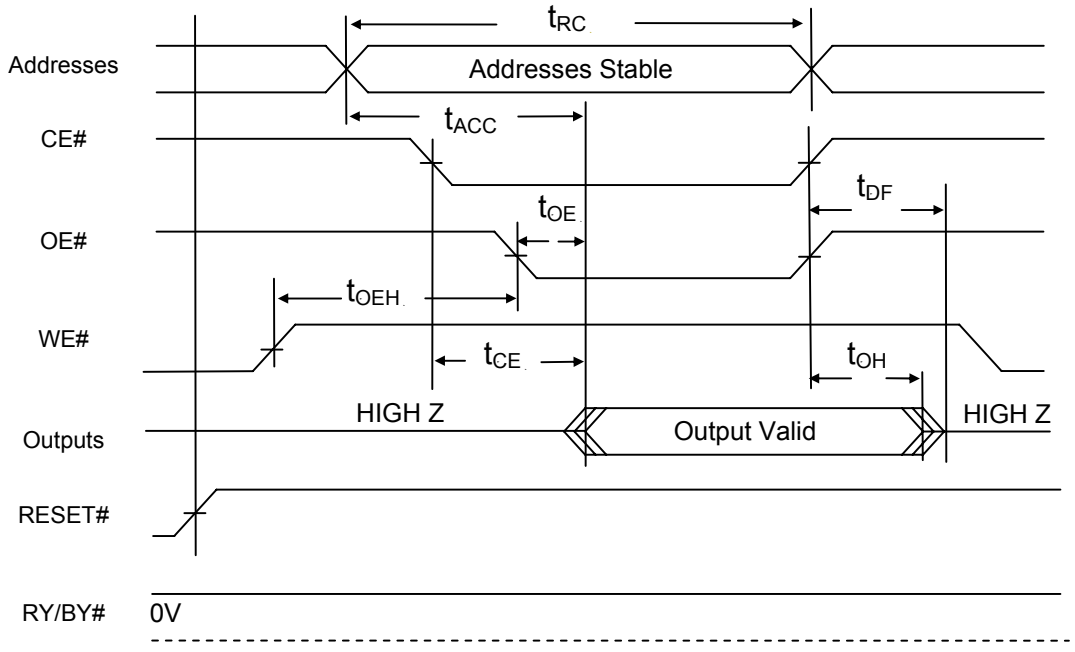
Table 12. Read-only Operations Characteristics

Parameter Symbols		Description		Test Setup		Speed Options		
JEDEC	Standard					-70	-90	Unit
t_{AVAV}	t_{RC}	Read Cycle Time			Min	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay		OE# = V_{IL}	Max	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z			Max	20	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z			Max	20	20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, whichever occurs first			Min	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read		Min	0	0	ns
			Toggle and Data# Polling		Min	10	10	ns

Notes:
1. High Z is Not 100% tested.
2. For - 70 Vcc = 3.0V – 3.6V Output Load: 30pF
   Input Rise and Fall Times: 5ns Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level, Input and Output: 1.5 V

   -90: Vcc = 2.7V – 3.6V Output Load: 100 pF
   Input Rise and Fall Times: 5 ns Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level, Input and Output: 1.5 V

Figure 3. AC Waveforms for READ Operations



AC CHARACTERISTICS

Table 13. Write (Erase/Program) Operations

Parameter Symbols		Description			Speed Options		
JEDEC	Standard				-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	30	40	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write (OE# High to WE# Low)		Min	0	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	45	45	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	20	25	ns
t_{WHW1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	8	8	µs
			Word	Typ	8	8	
t_{WHW1}	t_{WHWH1}	Accelerated Programming Operation (Word AND Byte Mode) (Note 2)		Typ	7	7	µs
t_{WHW2}	t_{WHWH2}	Erase Operation (Note 2)	Sector	Typ	0.1	0.1	s
			Chip	Typ	16	16	s
	t_{VHH}	V_{HH} Rise and Fall Time		Min	250	250	ns
	t_{VCS}	Vcc Setup Time		Min	50	50	µs
	t_{RB}	Recovery Time from RY/BY#		Min	0	0	ns
	t_{BUSY}	WE# High to RY/BY# Low		Max	70	90	ns

Notes:
1. Not 100% tested.
2. See Erase and Programming Performance for more information.

AC CHARACTERISTICS

Table 14. Write (Erase/Program) Operations

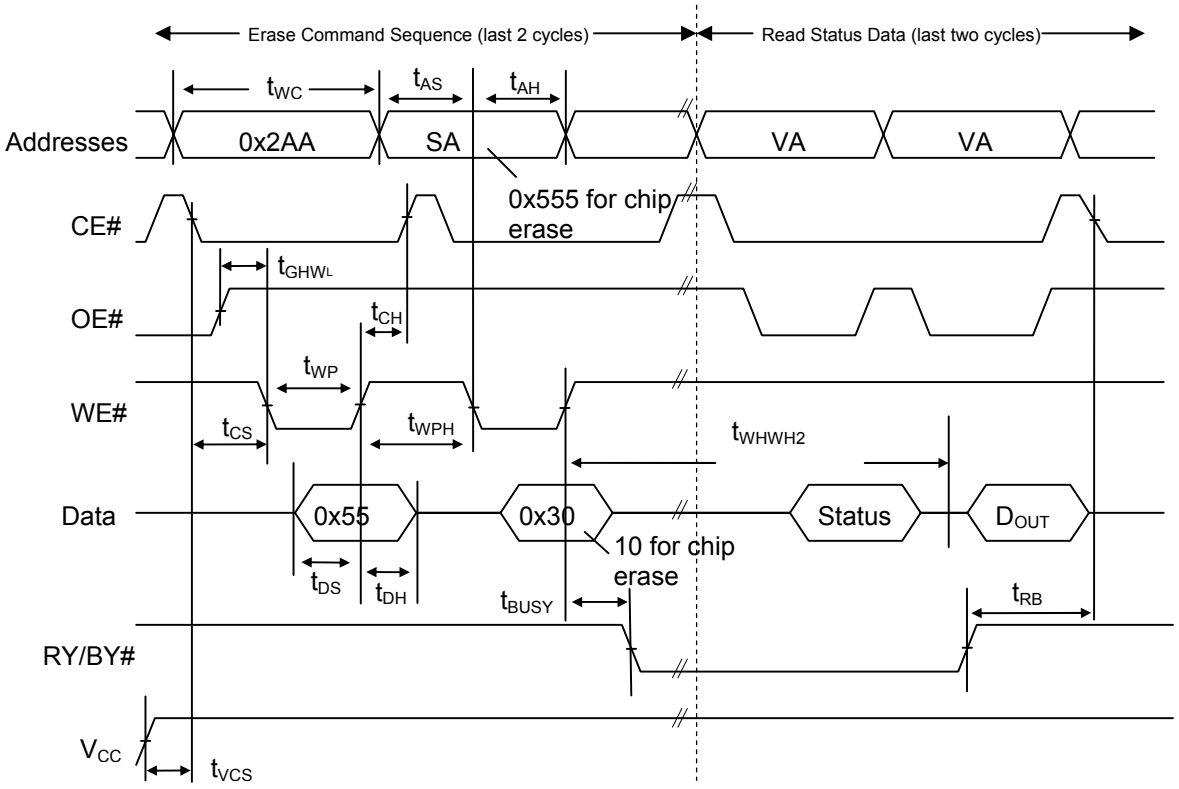
Alternate CE# Controlled Writes

Parameter Symbols		Description			Speed Options		
JEDEC	Standard				-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30	40	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time before Write (OE# High to CE# Low)		Min	0	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35	45	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	20	20	ns
t_{WHW1}	t_{WHWH1}	Programming Operation	Byte	Typ	8	8	µs
		(Note 2)	Word	Typ	8	8	
t_{WHW1}	t_{WHWH1}	Accelerated Programming Operation (Word AND Byte Mode) (Note 2)		Typ	7	7	µs
t_{WHW2}	t_{WHWH2}	Erase Operation	Sector	Typ	0.1	0.1	s
		(Note 2)	Chip	Typ	16	16	s
	t_{RB}	Recovery Time from RY/BY#		Min	0	0	ns

Notes:
1. Not 100% tested.
2. See Erase and Programming Performance for more information.

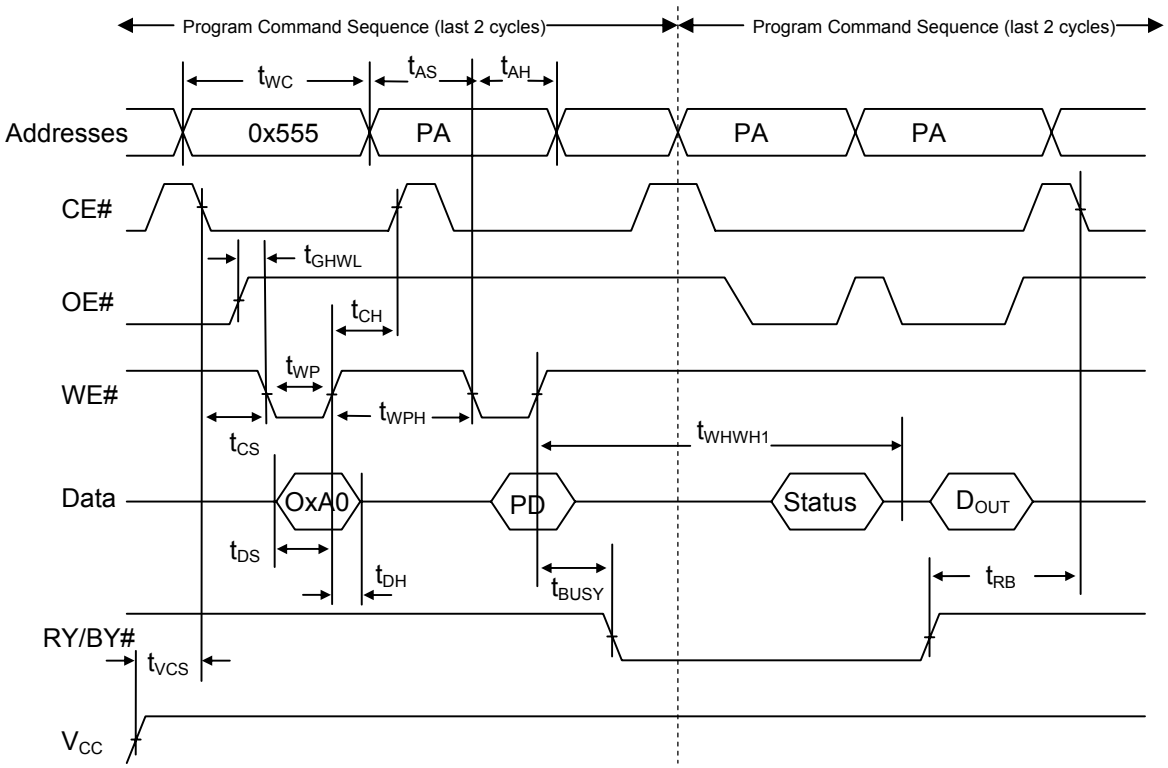
AC CHARACTERISTICS

Figure 4. AC Waveforms for Chip/Sector Erase Operations Timings



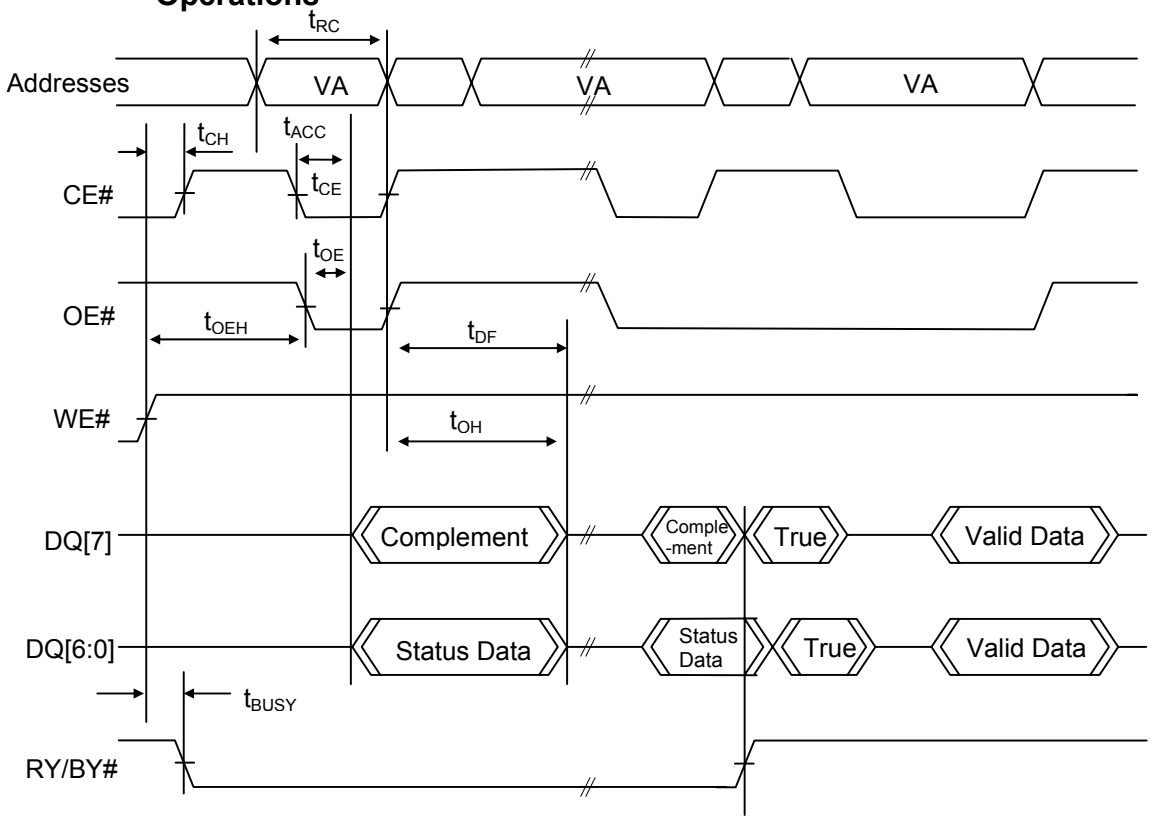
Notes:
1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, D_{out}=true data at read address.
2. V_{cc} shown only to illustrate t_{vcs} measurement references. It cannot occur as shown during a valid command sequence.

Figure 5. Program Operation Timings



Notes:
1. PA=Program Address, PD=Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown in order to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 6. AC Waveforms for /DATA Polling During Embedded Algorithm Operations



Notes:

1. VA=Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

Figure 7. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

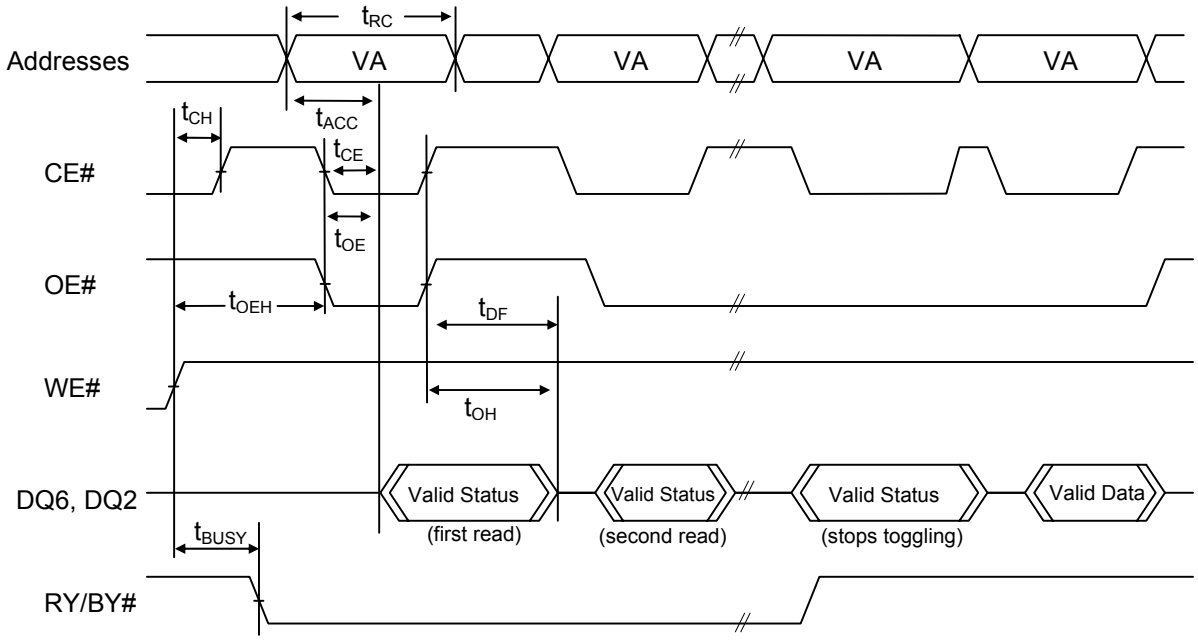
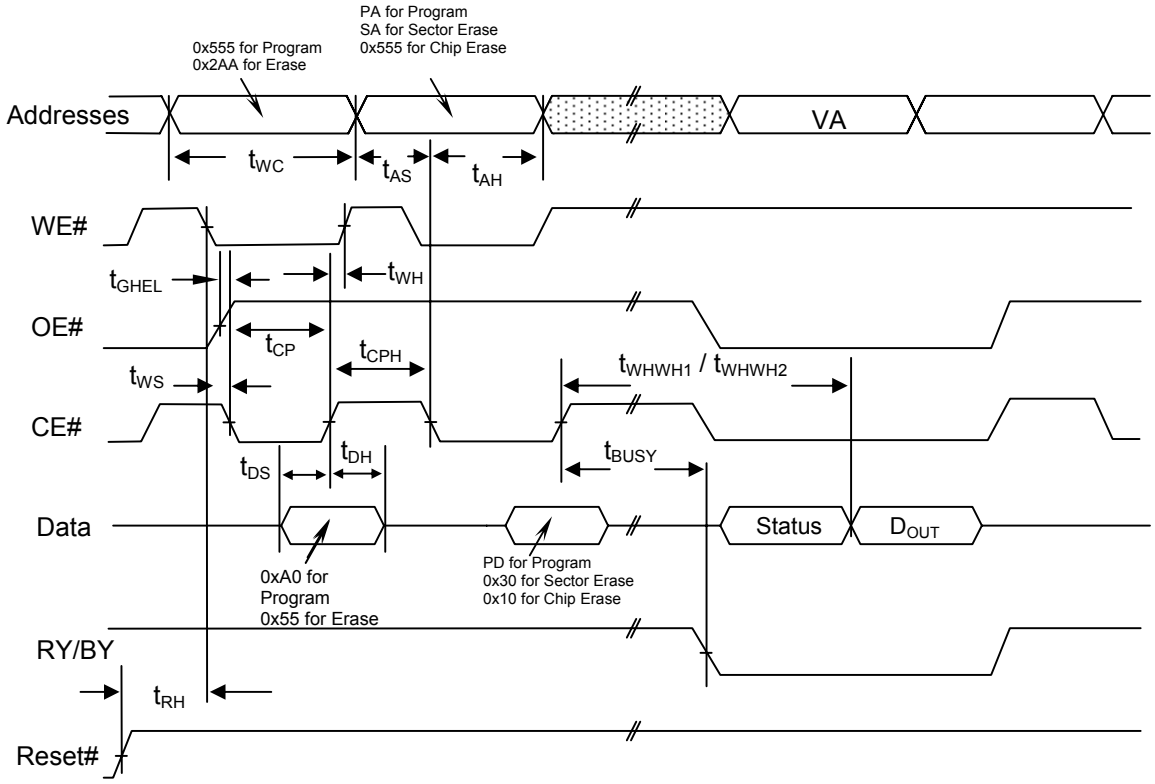


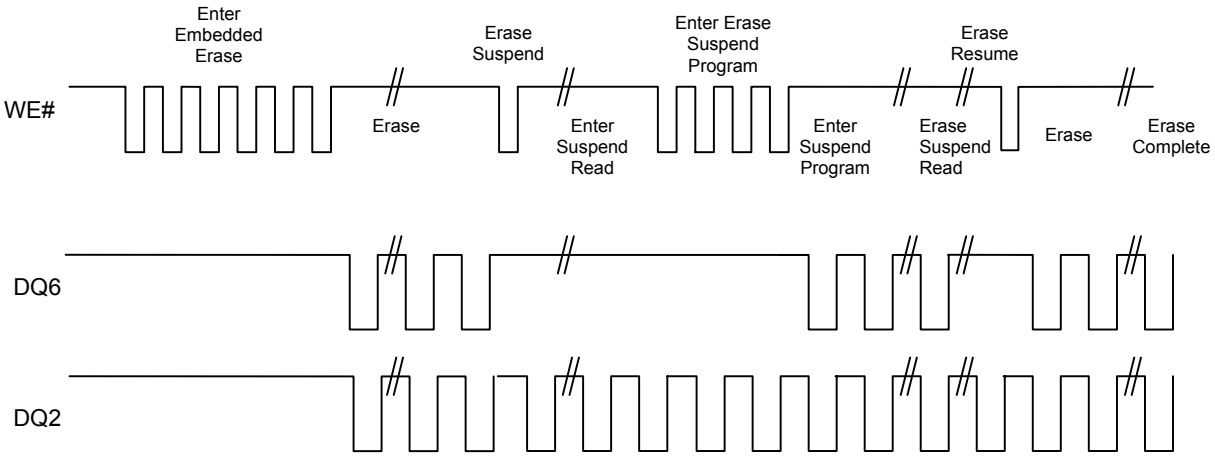
Figure 8. Alternate CE# Controlled Write Operation Timings



Notes:

PA = address of the memory location to be programmed.
PD = data to be programmed at byte address.
VA = Valid Address for reading program or erase status
D_{out} = array data read at VA
Shown above are the last two cycles of the program or erase command sequence and the last status read cycle RESETt# shown to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

Figure 9. DQ2 vs. DQ6



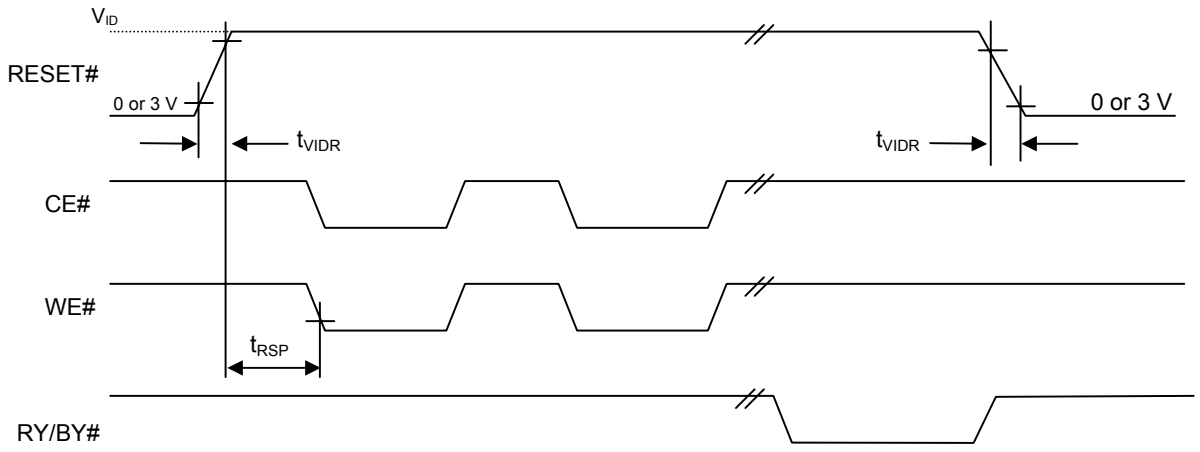
AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter Std	Description		Speed Option		Unit
			-70	-90	
t_{VIDR}	V_{ID} Rise and Fall Time	Min	500		ns
t_{VIHH}	V_{HH} Rise and Fall Time	Min	500		ns
t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4		µs

Notes: t_{RSP} is Not 100% tested.

Figure 10. Temporary Sector Unprotect Timing Diagram



AC CHARACTERISTICS

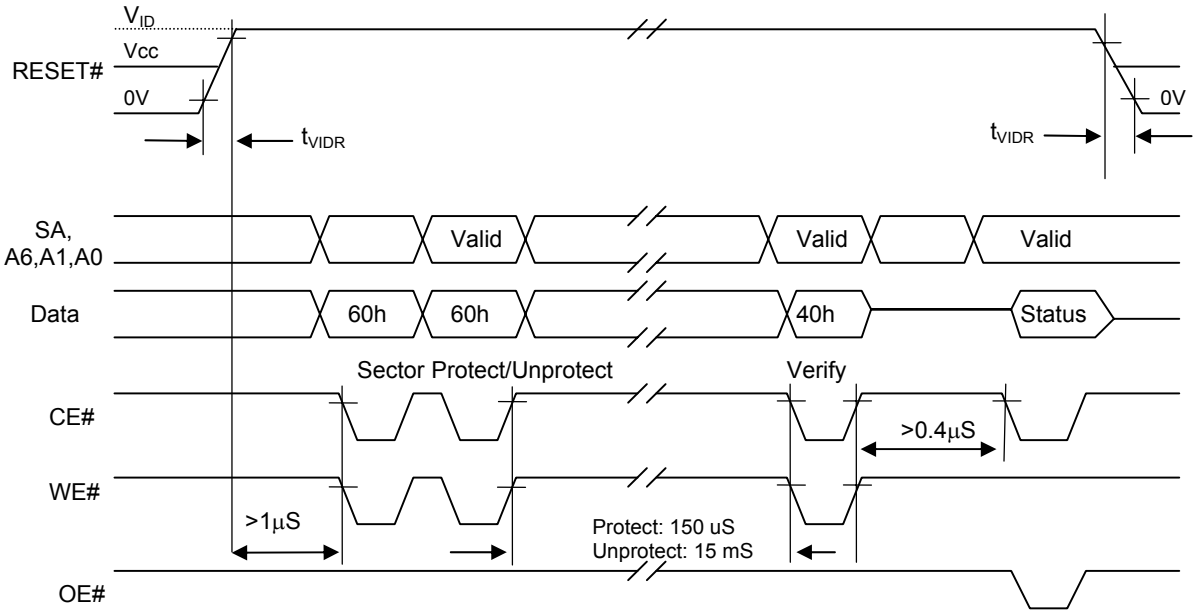
Write Protect / Accelerated Program

Figure 11. Accelerated Program Timing Diagram

AC CHARACTERISTICS

Sector (Group) Protect and Chip Unprotect

Figure 12. Sector (Group) Protect and Chip Unprotect Timing Diagram



Notes:

Use standard microprocessor timings for this device for read and write cycles.
For Sector (Group) Protect, use A6=0, A1=1, A0=0. For Chip Unprotect, use A6=1, A1=1, A0=0.

ERASE AND PROGRAM PERFORMANCE

Parameter		Limits			Comments
		Typ	Max	Unit	
Sector Erase Time		0.1	2	sec	Excludes 00h programming prior to erasure
Chip Erase Time		16	140	sec	
Byte Programming Time		8	200	µs	Excludes system level overhead
Word Programming Time		8	200	µs	
Accelerated Byte/Word Program Time		7	120	µs	
Chip Programming Time	Byte	67.2	201.6	sec	
	Word	33.6	100.8	sec	
Erase/Program Endurance		100K		Cycles	Minimum 100K cycles

Note: Typical Conditions are room temperature, 3V and checkboard pattern programmed.

48-PIN TSOP PACKAGE CAPACITANCE

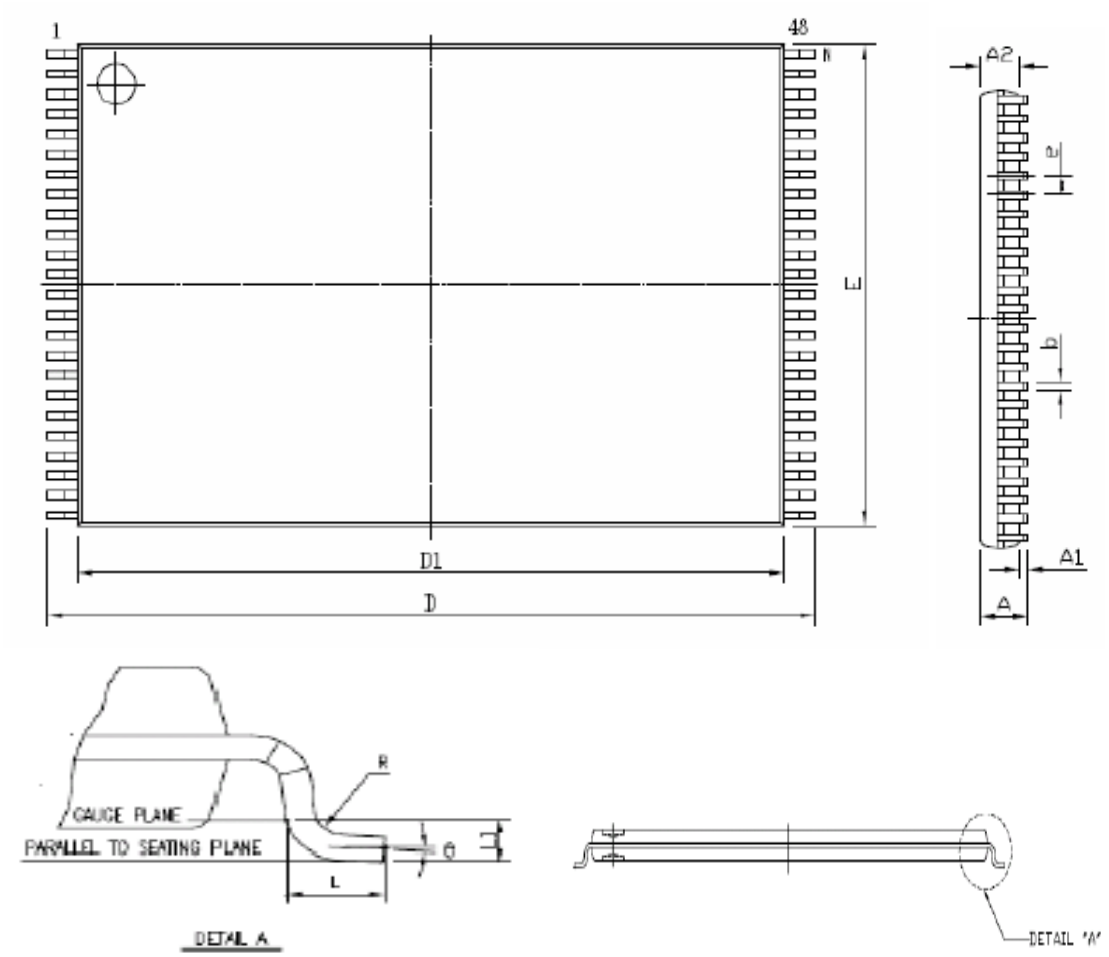
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Note: Test conditions are Temperature = 25°C and f = 1.0 MHz.

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

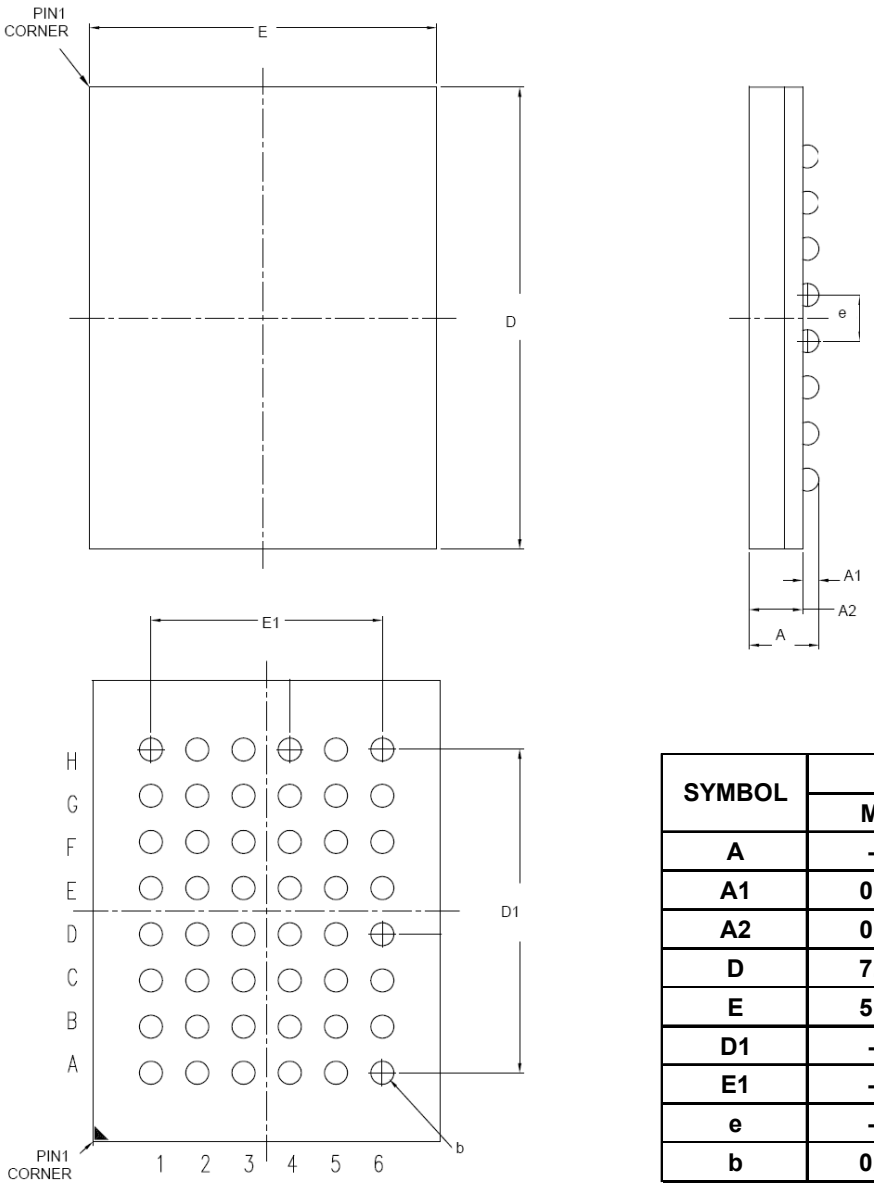
FIGURE 13. 48L TSOP 12mm x 20mm package outline



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.20
A1	0.05	- - -	0.15
A2	0.95	1.00	1.05
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.9	12.00	12.10
e	- - -	0.50	- - -
b	0.17	0.22	0.27
L	0.5	0.60	0.70
L1	- - -	0.25	- - -
R	0.08	- - -	0.20
θ	0^0	3^0	5^0

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm at the pkg ends, 0.25 mm between leads.

FIGURE 14. 48L TFBGA 6mm x 8mm package outline



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.30
A1	0.23	0.29	- - -
A2	0.84	0.91	- - -
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	- - -	5.60	- - -
E1	- - -	4.00	- - -
e	- - -	0.80	- - -
b	0.35	0.40	0.45

Note : 1. Coplanarity: 0.1 mm

Revisions List

Revision No	Description	Date
A	Initial Release	2007/3/13
B	1. Move the feature of SECURED SILICON SECTOR. 2. Change the notes for 70 ns products from Vcc = 2.7V – 3.6V to Vcc = 3.0V – 3.6V at Table 12. Read-only Operations Characteristics on page 40.	2007/05/16
C	1. Add the t_{BUSY} description in Table 13. Write (Erase/Program) Operations on page 41. 2. Correct the Figure 5. Program Operation Timings on page 44. 3. Update 48 pin TSOP-I package outline on page 50. 4. Correct the 48 Ball package thickness from 1.2 mm to 1.3 mm on page 51. 5. Remove C grade option of temperature range on page 1 and page 4.	2008/06/17
D	1. Add the 64 Ball TFBGA package and connection diagrams information on page 1, 3, 5 and 53. 2. Delete t_{OES} in page 41. 3. Modify AC Waveforms for READ Operations on page 41. 4. Add t_{RB} on page 42, 43.	2008/08/27
E	1. Add Eon products' New top marking "cFeon" information on page 1. 2. Modify Table 8 addresses 4Eh data from 00B5h to 00C5h on page 23.	2009/01/09
F	1. Update Erase and Program performance on page 2 and 51. 2. Modify P = Pb free to P = RoHS compliant on page 6. 3. Remove Unlock Bypass, Unlock Bypass Program, and Unlock Bypass Reset commands from Table 9 on page 25. 4. Remove description of Unlock Bypass from version E. 5. Modify Table 10 Status Register Bits DQ5 from ERROE BIT to TIME OUT BIT on page 31. 6. Modify Storage Temperature from "-65 to + 125" to "-65 to +150" on page 37 7. Modify I_{OH} from -100mA to -100µA on page 38 8. Modify Test Conditions illustration on page 39. 9. Update Hardware Reset (RESET#) table and Figure 1. AC Waveforms for RESET# on page 40 10. Update Table 13. Write (Erase/Program) Operations on page 43. 11. Update Table 14. Write (Erase/Program) Operations on page 44 12. Update Figure 4. AC Waveforms for Chip/Sector Erase Operations Timings on page 45 13. Update Figure 8. Alternate CE# Controlled Write Operation Timings on page 48 14. Remove the Latch up Characteristics Table from version E.	2009/03/13
G	1. Correct typo in Table 13, " t_{BUSY} " from Min. to Max on page 43.	2009/03/30
H	1. Correct typo for 70 ns products from Vcc = 2.7V – 3.6V to Vcc = 3.0V – 3.6V on page 2, 6, 13 and 42. 2. Remove 64 ball 11mm x 13mm TFBGA package information from version G	2009/04/20