EN332S/T

Dual-Channel SDI Rx on EX-SDI

Version 1.93
Apr. 2020

Document Revision History

Version	Date	Description	Modified by
1.0	16.07.08.	Initial release	DR Lee
1.1	16.08.03.	Overall revised	MS Kim
1.2	16.08.09.	Pin map changed	MS Kim
1.3	16.08.11.	Added CDM	NR Kim
1.4	16.09.23.	IRQ_* removed, GPO* added, Power consumption added	MS Kim
1.5	17.01.25	Support EX-SDI 4K - 1.485Gbps bandwidth added	HJ Kang
1.6	17.03.20	The channel coding of 4M changed	MS Kim
1.7	17.05.10	EX-SDI 4K Power consumption added	HJ Kang
1.8	17.05.17	Reg. schematic modify	DR Lee
1.9	17.07.12	SDI Output Level added	MS Kim
1.91	17.10.27	POD amended (Center Ground Pad)	MS Kim
1.92	17.10.31	ESD level added	MS Kim
1.93	20.04.22	Ambient Temperature changed	MS Kim

Document Description

This document describes the features and registers of EN332S/T

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Contents

1. General Description & Features

1.1. General Description

The EN332S/T device is a dual channel SDI receiver targeted for long reach performance with EX-SDI technology. The EX-SDI is a visually lossless codec for Long Reach Solution, reducing transmission bandwidth carried on existing cable such as coax cable and UTP cable.

Especially the EX-SDI V2.0 technology allows transmission distance to achieve 500m or more on RG59 cable with 135Mbps SDI-based encoding.

In addition to increasing the distance, the EX-SDI TDM supports multiplexing (or de-multiplexing) multi-channel up to eight channels over a single of coax cable at 1.485Gbps bandwidth.

For cost effectiveness, it highly integrates cable equalizers, de-serializers, audio de-embedder, and UCC-modulator dissipating low power consumption. It also features various output such as Frame-interleaving, Byte-interleaving and multiplexed format for H/W efficiency.

1.2. Features

Functions

- Supports EX-SDI V1.0/2.0 and EX-TDM
  - EX-SDI V2.0 - 135Mbps bandwidth
  - EX-SDI V1.0 - 270Mbps bandwidth
  - EX-SDI 3G - 270Mbps bandwidth
  - EX-SDI 4K - 1.485Gbps bandwidth
  - EX-TDM - 1.485Gbps bandwidth
  - HD-SDI, 3G-SDI
- Supports multi formats
  - 720p 24/25/30/50/60
  - 1080p 24/25/30/50/60
  - 1080i 50/60, 1536p 20
  - 1/1.001 Fractional FPS
- Supports 16-bit(non-multiplexed) or 8-bit(multiplexed) input mode (EN332T only)
- Supports only 8-bit(multiplexed) output mode
- Supports HDcctv1.0, SMPTE 292
- One SDI Tx loop-through among 2channel input SDI
- EX-SDI Decoder for long reach
  - 500m over RG59 at EX-SDI V2.0
  - 300m over 3C-2V at EX-SDI V2.0
- STREAM ID extracting (HDcctv 1.0)
- CRC, Line no. correction
- Auto detection of HD-SDI and EX-SDI
- Auto Image format detection
- Support Frame-Interleaving or Byte-Interleaving
- Audio/Video Pattern generator
- Audio de-embedder
- UCC modulator from 0.5MHz~10MHz
- Virtual wire for UCC, UART generator
- I2S interface for external DAC
- I2C Host interface

Power Management

- 1.8V or 3.3V I/O
- 1.2V Core Power

Operating Frequency

- Max. 148.5MHz

Operating Ambient Temperature

- -20˚C ~ +70˚C

Power consumption

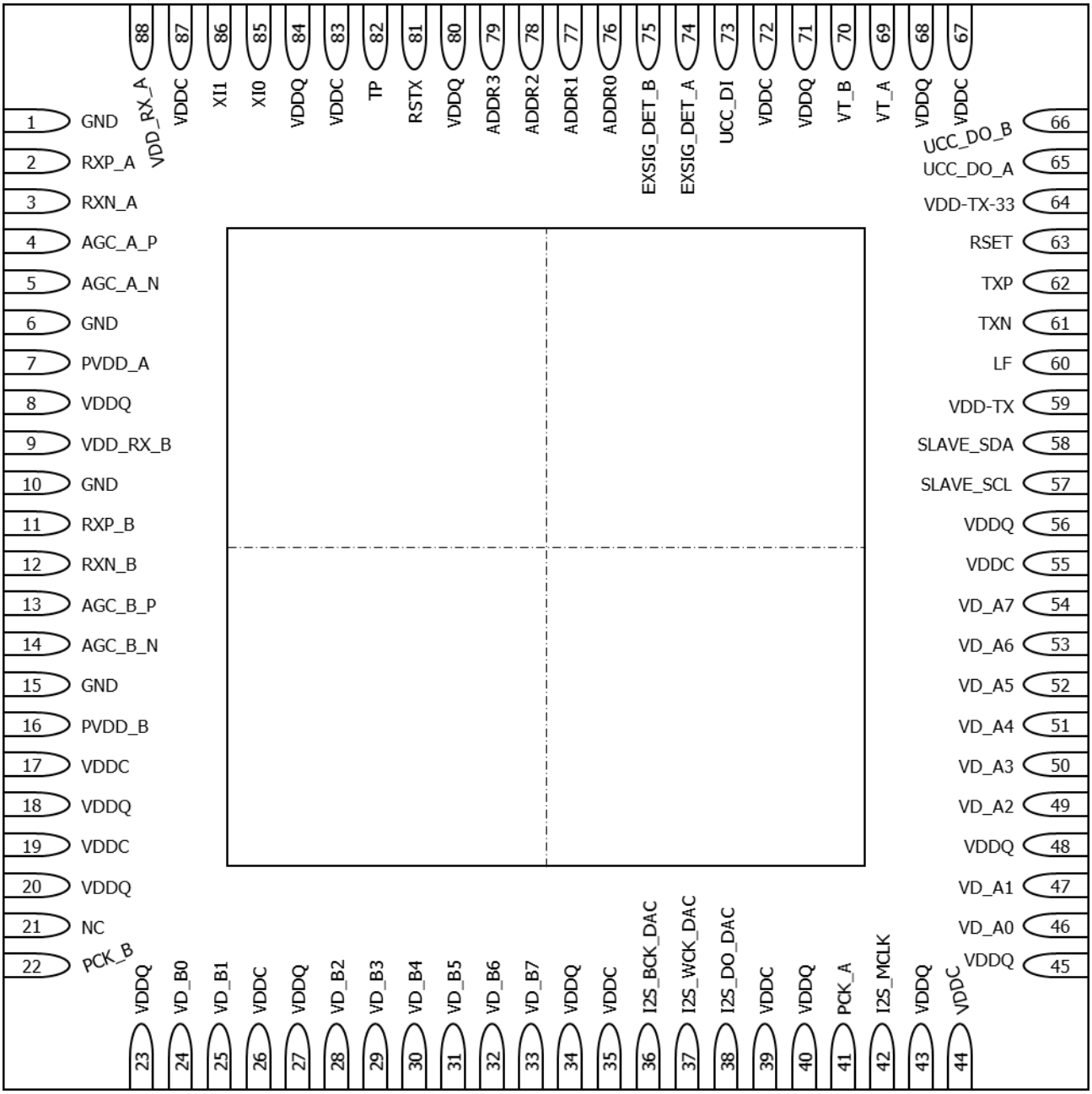
- TBD mW (HD-SDI mode)
- TBD mW (EX-SDI mode)

Package

- 88LGA 10mm x 10mm

2. Pin Diagram

[Top view]



3. I/O Information

No.	Name	I/O	Category	Description
81	RSTX	I	System	Global Reset (Active Low)
85	XI0	I		System clock (27MHz)
86	XI1	I		Audio source clock (24.576MHz)
82	TP	I		Test pin (Pull down)
76	GPO0 / ADDR0	IO	Device ID	Slave I2C device ID / General Purpose Output (PIN strapped with I2C Slave address, See '*11. I2C Interface*')
77	GPO1 / ADDR1	IO		
78	ADDR2	IO		Slave I2C device ID (PIN strapped with I2C Slave address, See '*11. I2C Interface*')
79	ADDR3	IO		
57	SLAVE_SCL	IO	Slave I2C	I2C data for host interface
58	SLAVE_SDA	IO		I2C clock for host interface(pull-up)
2	RXP_A	A	RX SDI Port A	SDI Rx PHY differential (-) input
3	RXN_A	A		SDI Rx PHY differential (+) input
4	AGC_A_P	A		Automatic positive gain control of SDI Rx
5	AGC_A_N	A		Automatic negative gain control of SDI Rx
11	RXP_B	A	RX SDI Port B	SDI Rx PHY differential (-) input
12	RXN_B	A		SDI Rx PHY differential (+) input
13	AGC_B_P	A		Automatic positive gain control of SDI Rx
14	AGC_B_N	A		Automatic negative gain control of SDI Rx
61	SDIN	A	TX SDI	SDI differential (-) output
62	SDIP	A		SDI differential (+) output
60	LF	A		Loop filter
63	RSET	A		HD-SDI output amplitude. 750Ω resistor needs to be located between RSET pin and VDD_TX_33 on a board.
41	PCK_A	O	Video Data Port A	Clock of video data
46	VD_A0	IO		Input/output video data bit0
47	VD_A1	IO		Input/output video data bit1
49	VD_A2	IO		Input/output video data bit2
50	VD_A3	IO		Input/output video data bit3
51	VD_A4	IO		Input/output video data bit4
52	VD_A5	IO		Input/output video data bit5
53	VD_A6	IO		Input/output video data bit6
54	VD_A7	IO		Input/output video data bit7
22	PCK_B	IO	Video Data Port B	Clock of video data
24	VD_B0	IO		Input/output video data bit0
25	VD_B1	IO		Input/output video data bit1
28	VD_B2	IO		Input/output video data bit2
29	VD_B3	IO		Input/output video data bit3
30	VD_B4	IO		Input/output video data bit4

31	VD_B5	IO		Input/output video data bit5
32	VD_B6	IO		Input/output video data bit6
33	VD_B7	IO		Input/output video data bit7
73	UCC_DI	I	UCC	Upstream modulation
65	UCC_DO_A	O		Upstream modulation output of video A
66	UCC_DO_B	O		Upstream modulation output of video B
69	VT_A	IO	Virtual Wire	Source input channel A of virtual wire for UCC
70	VT_B	IO		Source input channel B of virtual wire for UCC
74	EXSIG_DET_A	I	External Signal detect	Signal detection of external EQ A
75	EXSIG_DET_B	I		Signal detection of external EQ B
42	I2S_MCLK	O	Audio Interface	Serial audio master clock
37	I2S_WCK_DAC	IO		Serial audio DAC word clock
36	I2S_BCK_DAC	IO		Serial audio DAC bit clock
38	I2S_DO_DAC	O		Serial audio DAC data output
59	VDD_TX	P	TX SDI	Digital power of SDI Tx
64	VDD_TX_33	P		Analog 3.3V power of SDI Tx
-	VDDC	P	Core Power	17, 19, 26, 35, 39, 44, 55, 67, 72, 83, 87
-	VDDQ	P	IO Power	8, 18, 20, 23, 27, 34, 40, 43, 45, 48, 56, 68, 71, 80, 84
21	N.C.	-	N.C	
89	GND	P	Ground	Exposure Pad

4. Block Diagram

The EN332S/T consists of Analog SerDes part and Digital part. Analog parts have adaptive equalizers, clock data recovery and PLL. Digital parts have descrambler, TRS searcher, word align, ANC extraction and EX-SDI decoder. Especially video formatter can make two type interleaving output, Frame-interleaving and Byte-interleaving, for low-end backend device.

For special function, UCC modulator is integrated for making adjustable frequency-modulation applicable to an external UCC filter circuit. .

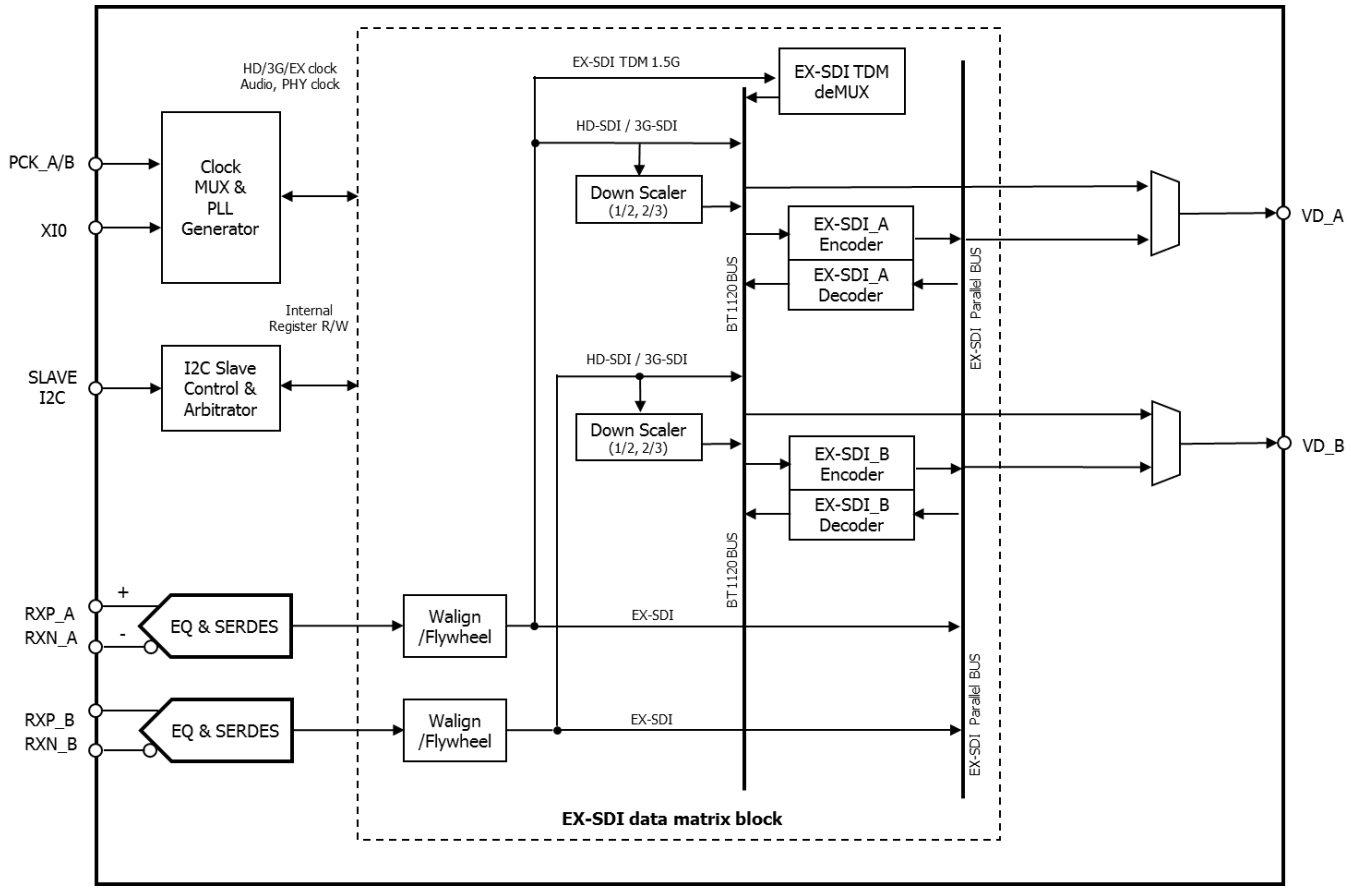


Figure 4-1. EN332S block diagram

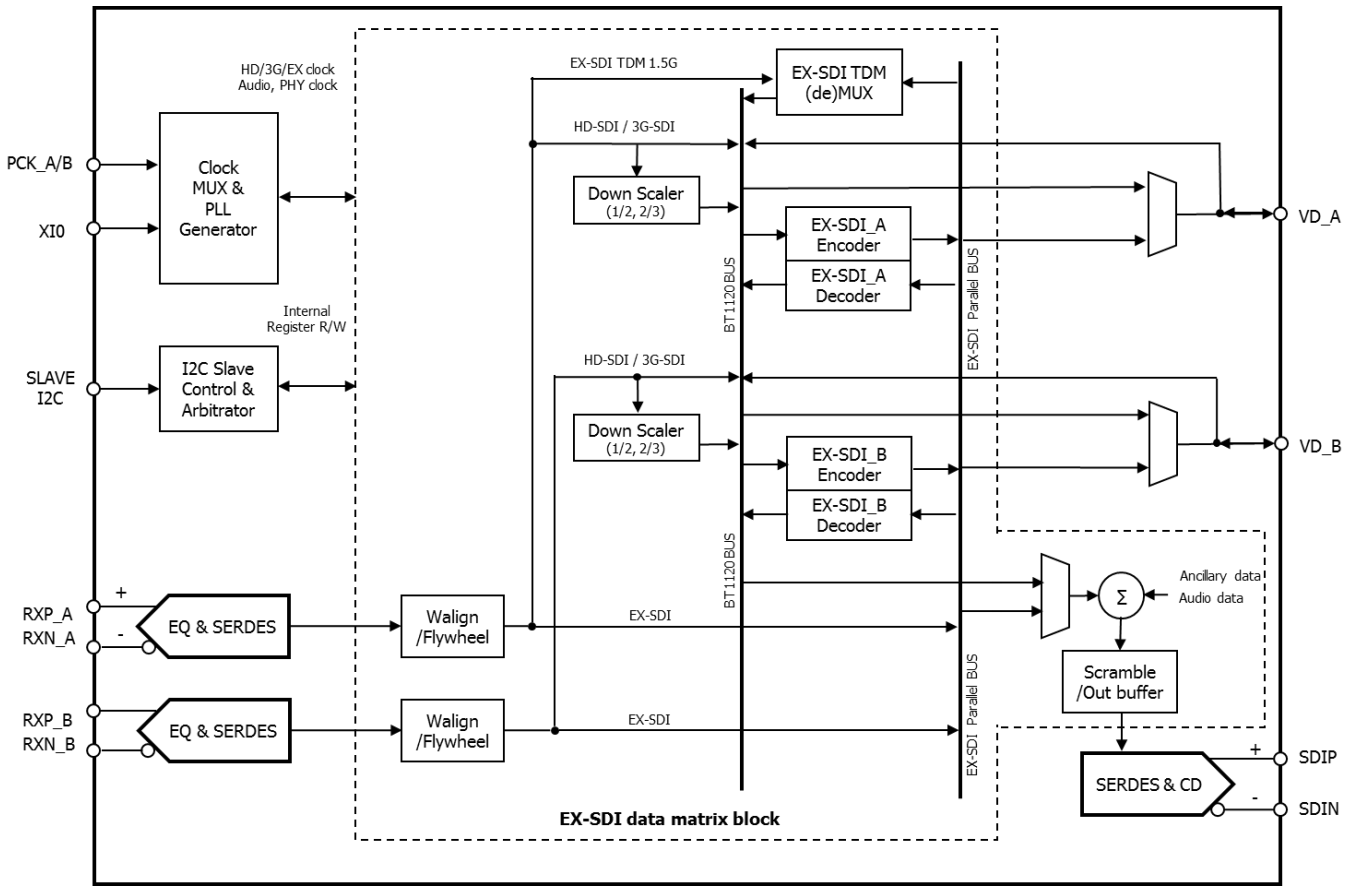


Figure 4-2. EN332T block diagram

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

(I/O Power : 1.8V, 3.3V Wide Range)

Symbol	Parameter	Rating		Unit
VDDC	DC Core Voltage	1.08	1.32	V
VIN	DC Input Voltage(1.8V)	1.65	1.95	V
	DC Input Voltage(3.3V)	3.0	3.6	V
VOUT	DC Output Voltage(1.8V)	1.65	1.95	V
	DC Output Voltage(3.3V)	3.0	3.6	V
latch	Latch-up Current	±100		mA
TSTG	Storage Temperature	-40 ~ 125		℃

5.2. Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
VDDC	DC Core Voltage	1.2 ± 0.12	V
VIN	DC Input Voltage(1.8V)	1.8 ± 0.18	V
	DC Input Voltage(3.3V)	3.3 ± 0.33	V
VOUT	DC Output Voltage(1.8V)	1.8 ± 0.18	V
	DC Output Voltage(3.3V)	3.3 ± 0.33	V
TOPR	Operating Temperature	-20 to 70	℃
TSTG	Storage Temperature	-40 to 125	℃

5.3. Static characteristics

	Level			Unit
	Pin	Target	Ref.	
Human Body Model	All	±2,000 ↑		V
Charged Device Model	All	±500 ↑		

5.4. DC Electrical Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
	Analog	VDD_RX_A/B	AV_{DD2}		-9%	1.2	+9%	V
		VDD_TX	AV_{DD3}		-9%	1.2	+9%	V
		VDD_TX_33	AV_{DD4}		-9%	3.3	+9%	V
		PVDD_A/B	AV_{DD5}		-9%	1.2	+9%	V
	Digital	VDDQ	DV_{DD0}		-9%	1.8, 3.3	+9%	V
		VDDC	DV_{DC}		-9%	1.2	+9%	V
Digital input voltage			V_{IH2}		0.7 DV_{DD0}		4	V
			V_{IL2}		-0.3		0.3 DV_{DD0}	V
Digital output voltage			V_{OH2}		DV_{DD1}-0.2			V
			V_{OL2}				0.2	V
Serial input Voltage (Common)		RXP_A/B, RXN_A/B	V_{CMI}			1.2		V
Serial output Voltage		SDIP, SDIN	V_{SDO}	RSET=750Ω with 75Ω load (HD-SDI)	-10%	800[1)]	+10%	mVp-p

Notes :

1. The voltage level, 800mV may vary depending on specific PCB design, components and the related registers.

5.5. AC Electrical Characteristics

5.5.1. Input characteristics

5.5.1.1. Main reference clock

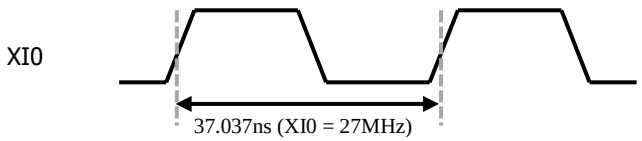


Figure 5-1. XI0 clock timing diagram

5.5.1.2. Video output characteristics

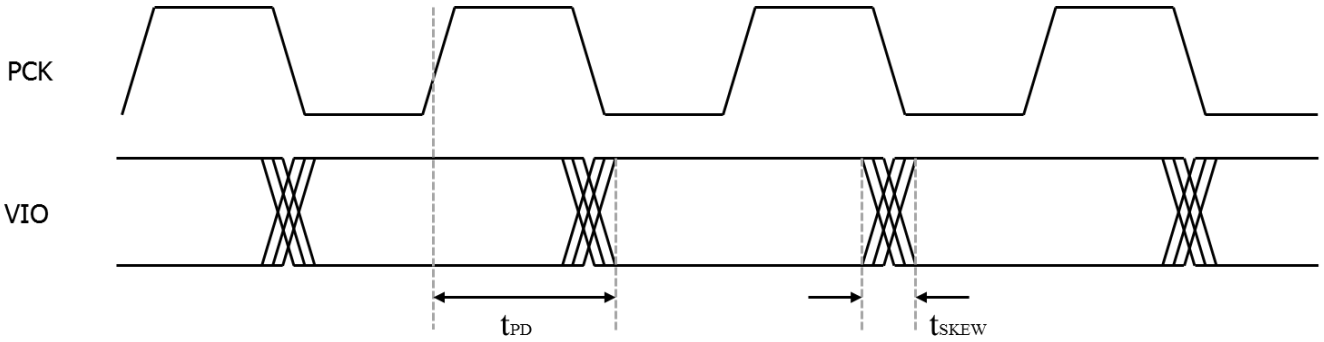


Figure 5-2. Parallel data output timing diagram

Interface	Symbol	Definition	MIN.		MAX.		Unit
			VD_A	VD_B	VD_A	VD_B	
HD 30p SDR 8bit@148.5MHz	t_{PD}	PCLK to Data	3.99	3.98	5.02	5.03	ns
	t_{SKEW}	Skew	0.05	0.08	0.13	0.19	ns
HD 60p DDR 8bit@148.5MHz	t_{PD}	PCLK to Data	0.57	0.67	1.42	1.72	ns
	t_{SKEW}	Skew	0.04	0.07	0.07	0.18	ns
HD 30p TDM(2CH) DDR 8bit@148.5MHz	t_{PD}	PCLK to Data	2.42	-	2.19	-	ns
	t_{SKEW}	Skew	0.07	-	0.12	-	ns
4K SDR mode 16bit@297MHz	t_{PD}	PCLK to Data	2.42		0.07		ns
	t_{SKEW}	Skew	0.11		0.16		ns
4K DDR mode 16bit@148.5MHz	t_{PD}	PCLK to Data	0.65		1.99		ns
	t_{SKEW}	Skew	0.09		0.11		ns

5.5.1.3. Audio output characteristics

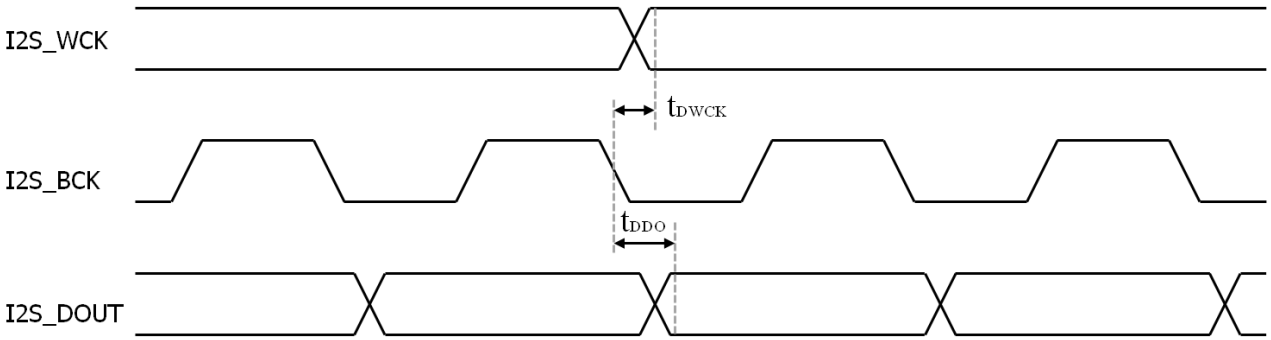


Figure 5-3. Audio I2S timing diagram

Symbol	Definition	min	max	Unit
t_{DWCK}	I2S_WCK delay			ns
t_{DDO}	I2S_DOUT delay			ns

6. Power on sequence

The recommended EN332S/T power-up reset timing is summarized in the following figure and table.

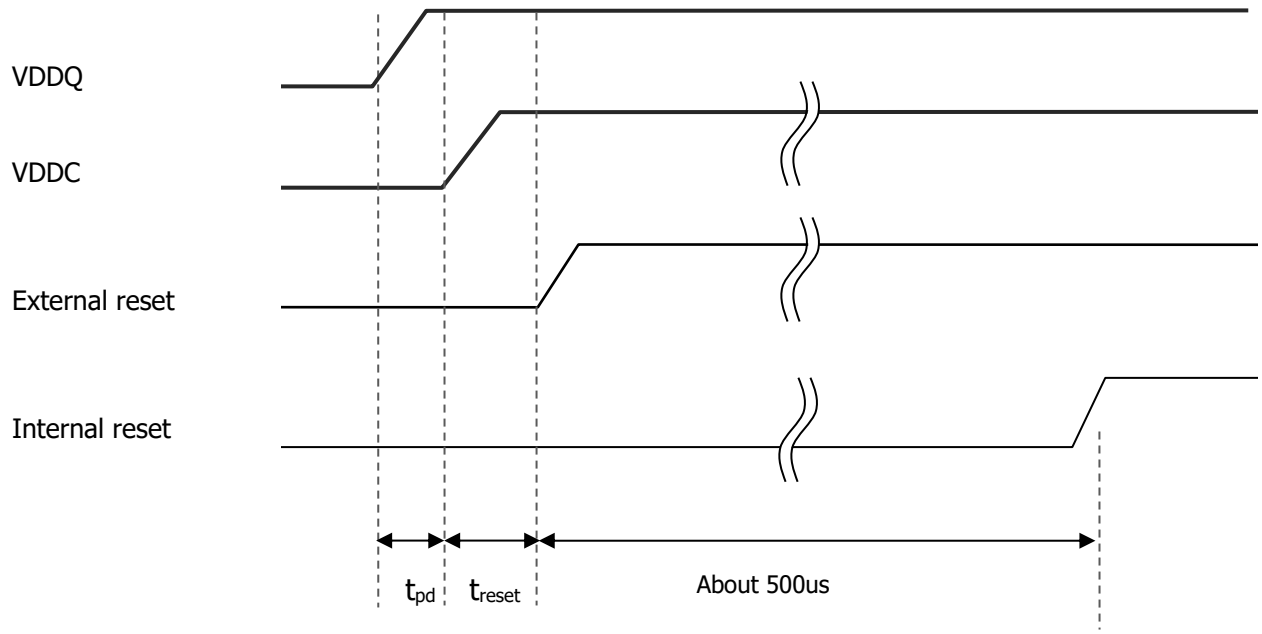


Figure 6-1. Reset sequence timing diagram

Pin strap-ins (GPO0/ ADDR0, GPO1/ ADDR1, ADDR2, ADDR3) are latched during power-up or reset.
After all powers are stable, the EN332S/T's slave address is configured from Pin strap-ins during reset sequence.
It is recommended to keep these pins not connected to any pins except pull-up (or pull-down) to avoid pin-collision, which can result in I2C errors.

Timing Parameter	Description	Min	Typ	Max	unit
t_{pd}	From VDDQ to VDDC	10	-	-	us
t_{reset}	From stable power to reset	1	-	-	us

7. Power consumption

	VD Output Mode (bit)	VDDQ (mA)	VDDC (mA)	VDD-RX (mA)	PVDD (mA)	VDD-TX (mA)	VDD-TX-33 (mA)	Total (mW)
		3.3V	1.2V	1.2V	1.2V	1.2V	3.3V	
HD-SDI	8	150	70	40	15	10	1.4	661.62
	8 TDM	130	70					595.62
EX-SDI 1.0/2.0	8	150	82					676.02
	8 TDM	130	82					610.02
EX-SDI 3G/ EX-SDI 4M	8	180	110	45	20			820.62
EX-SDI 4K	16	180	150					868.62

8. Clock Structure

Clock Name	Max. Freq.	Description
XI0	27MHz	Global clock input
XI1	24.576MHz	Audio source clock
PCKO_x	148.5MHz	VIDEO clock
SLAVE_SCL	100kHz	Slave I2C clock input
MASTER_SCL	100kHz	Slave I2C clock input
I2S_BCK_DAC	3MHz	Audio I2S BCK(I/O)
I2S_WCK_DAC	48kHz	Audio I2S WCK(I/O)

9. Functional Overview

9.1. SDI Input

The EN332/T is a quad SDI receiver. It integrated four cable equalizers, CDR, De-serializer, Audio extraction and UCC modulators.

The four equalizers reconstruct attenuated SDI signal, whose frequency presents from 135Mbps and 2.98Gbps. It also features strong DC restoration to overcome stress patterns such as pathological pattern designated in RP 178, which has a poor ratio of 'ones' to 'zeros'.

This is compliant to SMPTE292, SMPTE259 and HDcctv.

9.2. EX-SDI

Generally achievable distance is in inverse proportion to transmission rate. With RG59 cable, transmission distance is approximately 330m in 270Mbps, 160m in 1.485Gbps and 100m in 2.98Gbps.

EX-SDI V1.0 supports only 270Mbps–transmission with 20% image compression. This makes HD-SDI (1.485Gbsp data rate) go over 300m and go over low-end cable.

Moreover, since EX-SDI V2.0 supports not only 270Mbps but also 135Mbps, transmission distance is much longer than V1.0. The expected reach is over 500m with RG59 cable. Furthermore it's helpful to reduce difficulties to use low-end cable such UTP and 3C-2V.

EX-SDI is a visually lossless codec based on JPEG standard. It's processing is simple as shown below figure.

It is composed of compress codec, domain conversion and codec rate controller.

Codec controller controls compression rate while studying optimal point of buffer. Optimal point is where total amount of compressed data is as much as empty buffer size by outputting data in buffer.

Therefore image quality relies on this controller. The PSNR is normally 40dB and more in normal source.

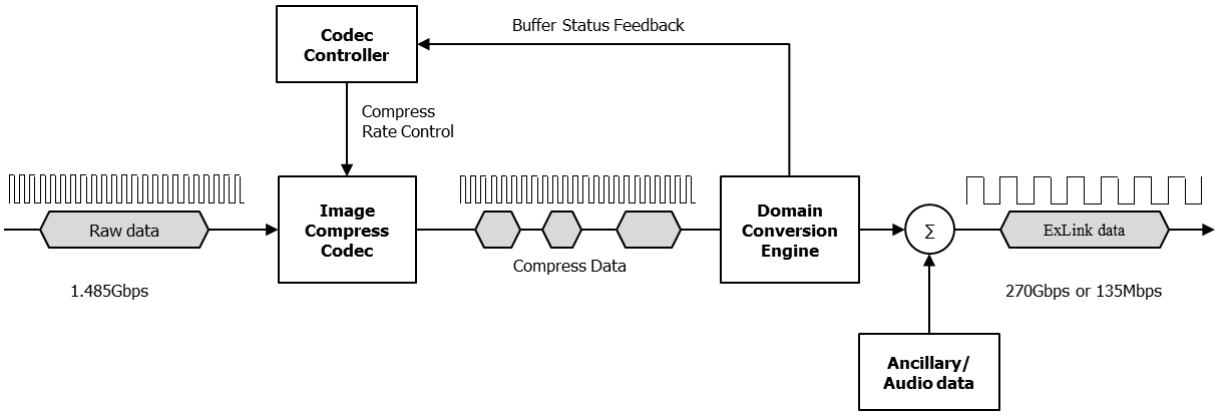


Figure 9-1. EX-SDI compress sequence

9.3. Virtual wire for UCC (Upstream Communication Channel)

UCC is a function to control a camera in DVR side over Coax cable remotely.

The EN332S/T has a UCC modulator inside, which can modulate commonly used control signals (UART, Pelco…) with 0.5MHz ~ 10MHz carrier frequency. With an associated UCC filter, modulated data can go upstream to the camera over coax cable while video data is going downstream from the camera.

In addition, it has UART generator in itself. It can make maximum 16byte serial UART data and outputting it to UCC modulator module.

(Please see UCC guide document for more details)

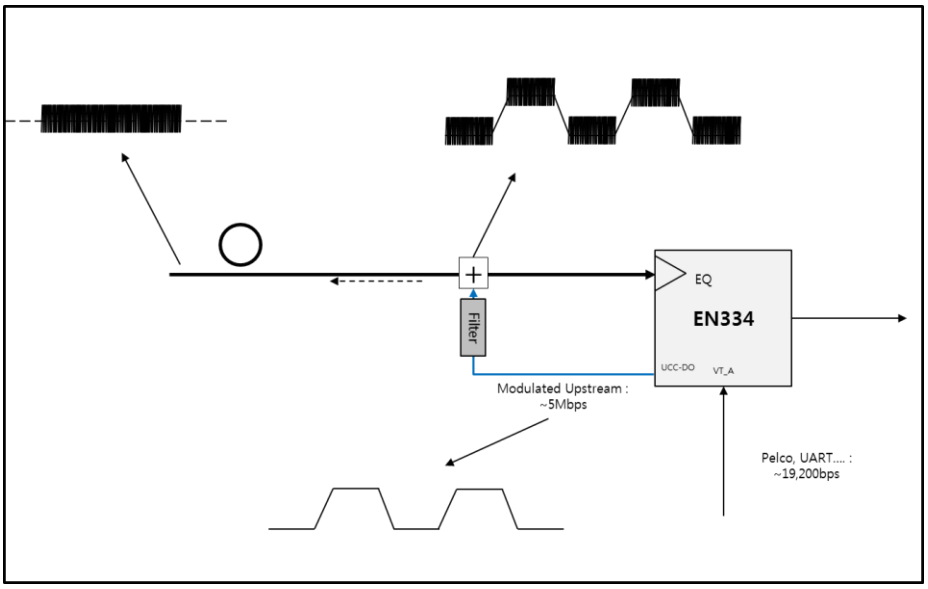


Figure 9-2. UCC transmit operation

9.4. Signal detector

The Signal Detector indicates the status of Serial Input Data, which is the combination of internal CDR status and SDI decoder.

After power on, it comes down to "zero", a low signal, which turns into "one", when SDI stream comes in and SDI decoder is activated. It also can be "zero" when signal is gone or stuck to either zero or one without transitions.

In addition to internal SD (signal detector), an external equalizer's SD, called as CD or SD in 15# pin, is read through I2C of EN332S/T if it is connected to EXSIG_DET_* pin.

(Please see 4.Video Format Identification in application note for more details)

9.5. Channel coding

The SDI standard defines scrambled NRZ as a channel coding. Scrambling signal makes it statistically likely to have a low DC content for easier handling and have a greater number of transitions for easier clock recovery without any bit redundancy (Polynomial G1(X) = $X^9 + X^4 + 1$, G2(X) = X + 1).

In order to convert available signal from SDI to parallel data, NRZI-to-NRZ and descrambling processing must be applied before main processing.

The traditional scrambling method used in SDI has a few advantages like no redundancy and polarity-free. Although under normal condition the scrambled data has high transition with an even ratio of ones to zeros, some scrambled status meets too challenging conditions for the receiver to reconstruct SDI signal.

For more reliable communication, EX-SDI 2.0 adopted 8B/10B instead of the scrambled NRZ, even though it has 2 bit redundancy. This helps to achieve DC-balance to reduce the risk of data miss-acquisition in CDR of a receiver side.

Mode	Data rate (bps)	Signal Encoding	Polarity free
HD-SDI	1.485G	Scrambled NRZ	O
3G-SDI	2.98G	Scrambled NRZ	O
EX-SDI V1.0	270M	Scrambled NRZ	O
EX-SDI V2.0	135M	8b/10b[1)]	X
EX-SDI 3G/4M	270M	8b/10b[1)]	X
EX-SDI 4K	1.485G	Scrambled NRZ	O
EX-SDI TDM	1.485G	8b/10b NRZ	O

Note[1)]: EN332S/T is input polarity-switchable, but it's controlled manually.

Table 9-1. Signal encoding and Polarity

9.6. Word alignment

The SDI stream has seven different types of packet with theirs specific identification code as listed in Table 9-1. After de-serializing and de-scrambling, the data flow into word alignment module to be aligned according to their origin. The word alignment module consist of both SMPTE compliant aligner and EX-SDI aligner.

The SMPTE aligner try to extract and detect TRS ID defined in SMPTE, and EX-SDI aligner is detecting its own TRS code embedded in data stream.

These complexity and the number of the mode make the external MCU take long time to detect input mode, which can be optimized according to the number of the activated mode.

9.7. Video format detector

The EN332S/T supports various video formats as well as the defined in SMPTE.

The video detector module identifies the format of the incoming video data, and extracts information as listed below.

- Total horizontal pixel in a line
- Total vertical line in a frame
- Interlace or Progress
- Frame rate (1 or 1000/1001)
- EX-SDI and HD-SDI

The above information is updated to the resisters to be accessed by MCU.

9.8. CRC detector and Counting

The CRC is an error-detecting code used in a digital network. The HD-SDI uses line-based CRC calculated every line, and EX-SDI has the packet-based CRC calculated every EX-SDI packet. Each packet has a different length and size according to the compressed quantity.

The EN332S/T extracts CRC value from the specific position (i.e. every EAV in HD-SDI, every end of packet in EX-SDI), while it re-generates a new CRC value from incoming data. When the extracted one and the re-generated one is the same, CRC counter keep the previous counter, otherwise when they are different, the counter increases.

The CRC is commonly used to check channel integrity to make sure of error free.

In instance, 10^{-12} BER (Bit Error Rate) is mandatory required for some certification in HDcctv alliance. It means that CRC error must not happen for about 15 minutes in HD-SDI. (About 7 minutes in 3G-SDI)

9.9. Ancillary data detector (STREAM ID)

In HD-SDI, The EN332S/T can extract ancillary datum, carried on the downstream SDI, up to 16(16 x 10bit), whose position is changed by adjusting vertical and horizontal position in Y (Luma) stream. (Generally the position is Line 8 to ensure that the Ancillary data is inserted after the switch line (Line 7))

In EX-SDI, the ancillary position is not adjustable, since the ancillary data is embedded to the specific position between the EX-SDI packets.

After extracting, 16 word registers are updated automatically every frame. The registers should be referred according to the result of input mode detector since the EX-SDI and HD-SDI have independent registers.

(Please see the application note for more details)

9.10. Pattern generator

The EN332S/T has a flexible video pattern generator that makes up to 4096x2160 format as well as HD format with the associated data clock and TRS. The pattern types can be configured by control registers belonging to each channel.

In addition to video, the frequency and amplitude - adjustable Sine wave can be generated for audio test pattern replacing SDI embedded audio.

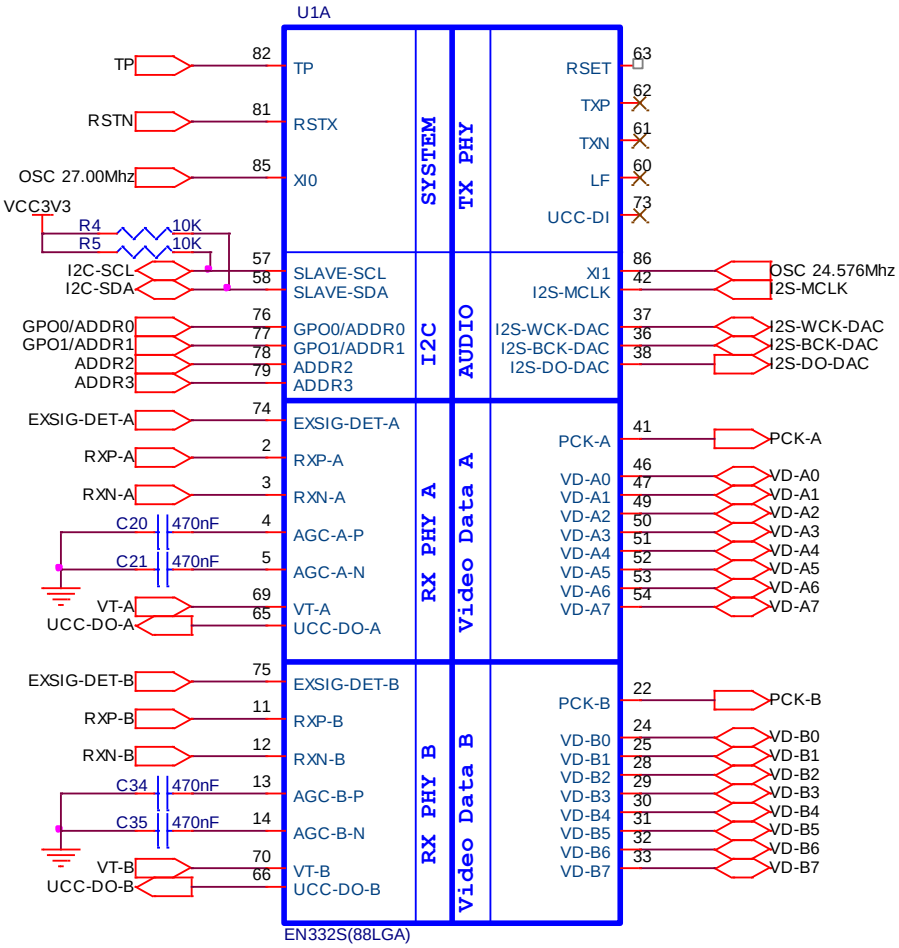
9.11. Video output formatting

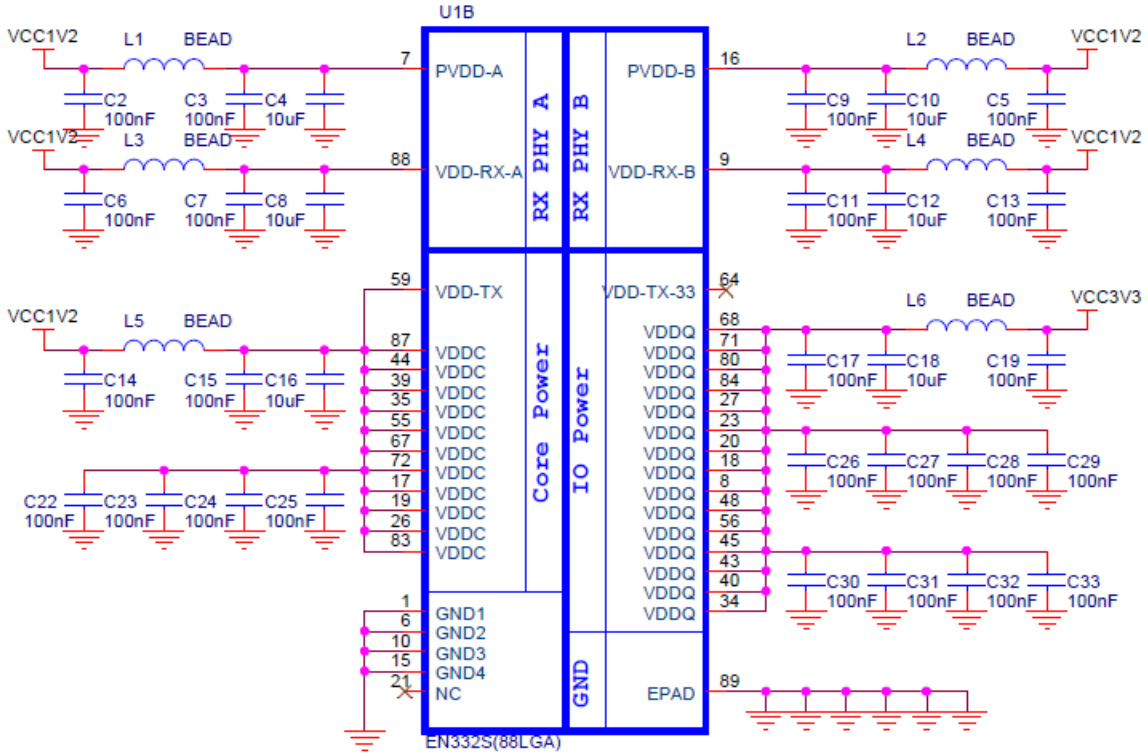
The EN332S/T supports various video output interface as well as standard BT.1120 outputs.

VO interface	Source format	PCK speed (MHz)	Data Rate (Mbps)
Four 8-bit interfaces	720 60p, 1080 30p	148.5	148.5
	1080 60p, 1440p(4M)	148.5(DDR)	297
Two 16-bit interfaces	2160 25p/30p (4K)	148.5(DDR), 297(SDR)	297
Two TDM 8-bit interfaces	720 60p, 1080 30p	148.5(DDR)	297

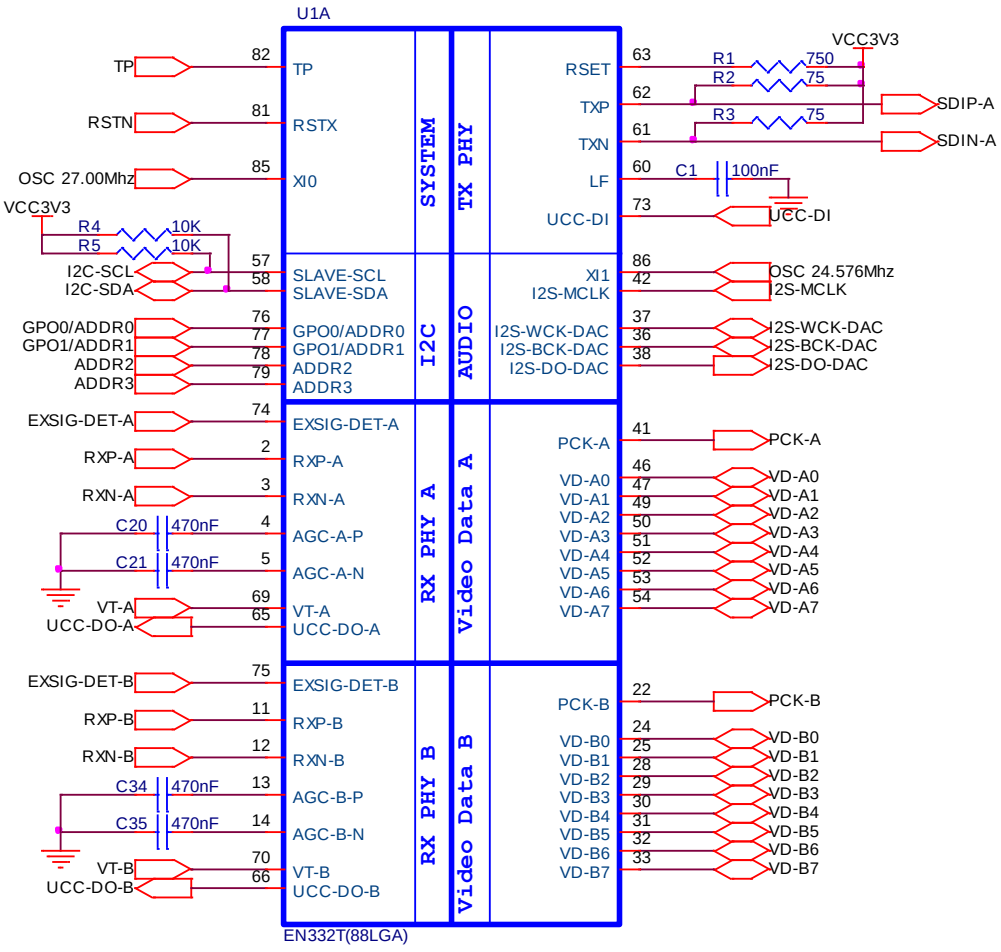
10. Application schematic

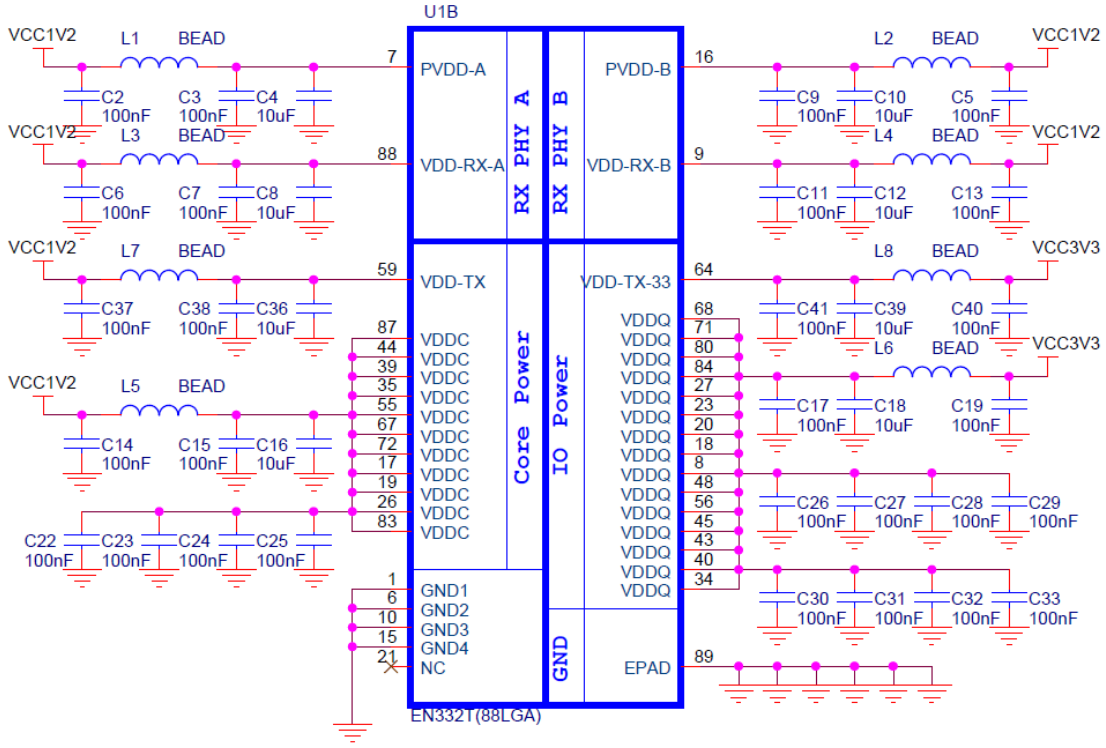
10.1. EN332S schematic



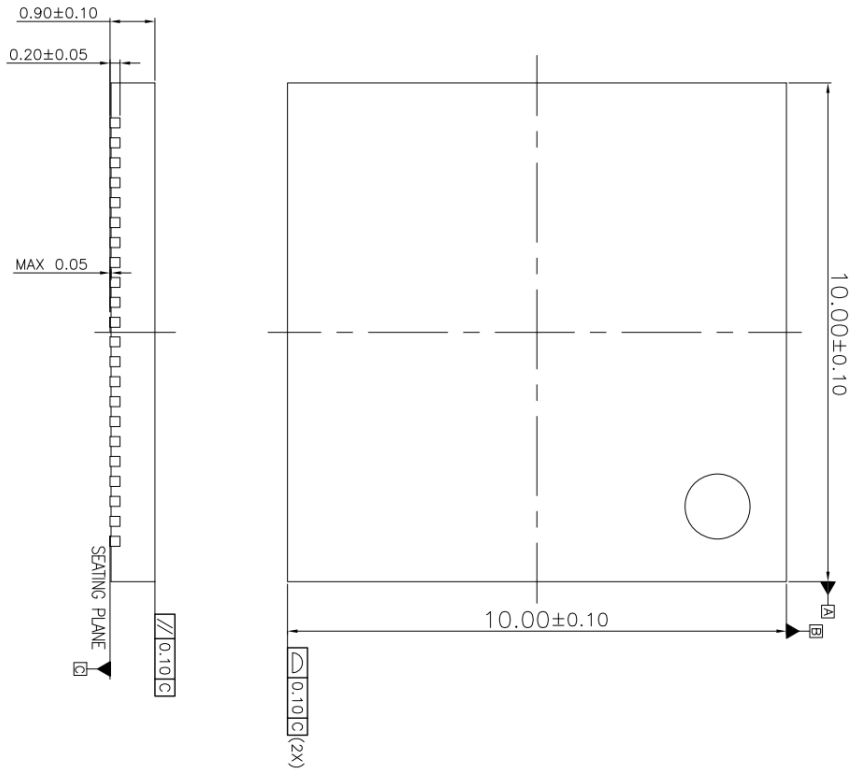


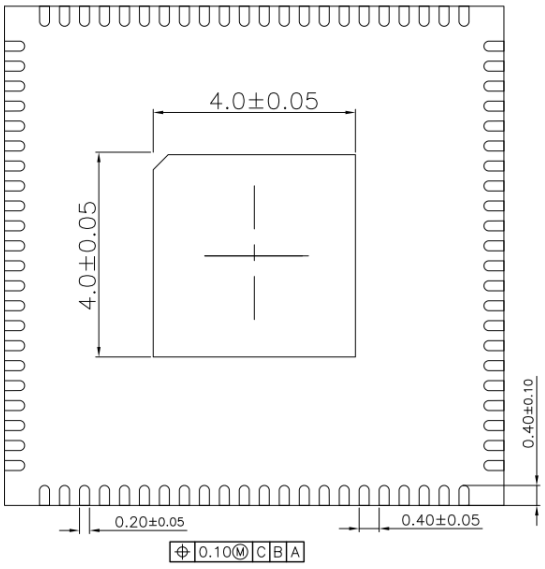
10.2. EN332T schematic





11. Package dimension





NOTE:
1. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION.