# EN870

## Digital Camera Processor

**Version 1.1**
**Apr, 2020**

# Revision History

| Version | Date | Description | Modified by |
|---|---|---|---|
| 1.0 | 2019.11.07. | Initial release. | MS.KIM |
| 1.1 | 2020.04.21. | Ambient Temperature changed | MS.KIM |
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# Document Description

This is the document to describe a feature and register which is applied to EN870.

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# 1. General Descriptions & Features

## 1.1 General Descriptions

The EN870 camera processor for security camera system. The main features include Wide Dynamic Range (WDR), Adaptive Contrast Enhancer, 3D Noise Reduction, auto AE/AF/AWB control, digital zoom and built-in EX-SDI. This is an SDI transceiver that targets SDI long distance with EX-SDI technology and has a high performance DAC, which includes an analog HD encoder, so you can transmit all kinds of analog HD without dedicated chipsets.

## 1.2 Features

**Image Signal Processing**

- Advanced RGB Interpolator for High Resolution
- Wide Dynamic Range compensation (WDR)
  - ✓ 2 page frame/line WDR for ~2M sensor
- Adaptive Digital Noise Reducer 2D / 3D
- Adaptive Contrast Enhancer (ACE)
- Histogram equalizer for De-fog
- Lens Shading Compensation
- Digital Zoom (~2M)
- Digital Down scaler : 1080p to 720p
- Defect Detection & Correction
- Optical detector (AE, AWB, sAF)
- Edge enhancement
- Gamma Correction
- Hue Controller (8-Way)
- High Light Masking
- Flip / Mirror / Still
- Box OSD (32ea, solid effects, auto zoom)
- Polygon Privacy Masking (8ea, auto zoom)
- Font OSD (Scalable 16x24 font, Styling, Half)
- Adaptive Lighting control
- Logic PWM Output
- External Flash Memory Controller
- External Audio AD/DA interface

**EX-SDI**

- EX-SDI v1.0/v2.0/v2.1
- UCC (upstream communication channel)
- PoC (Power over Coaxial)

**Image Output Mode**

- Parallel out : BT.1120, BT656
- Built-in EX-SDI PHY
- Built-in DAC (for HD analog)
  - ✓ CVBS: NTSC, PAL (960H)
  - ✓ HD analog

**Sensor Interface**

- 1M~2M CMOS sensor
- LVDS (8CH) / HiSPi / MIPI Interface (8lane)
- Master / Slave mode
- Frame Rate
  - ✓ 1.0M: Max. 120p
  - ✓ 2.0M: Max. 60p

**Multimedia Features**

- On-chip ADC (3ch mux type)
- On-chip MCU (EX-RISC 1.0)
  - ✓ 32bit processor (Max 148.5 MHz)
  - ✓ Embedded Program SRAM (128Kbyte)
  - ✓ 16Kbyte (I) + 8Kbyte (D) cache
  - ✓ Timer, UART, SPI, PWM, Watchdog timer, GPIO (32ea), IIC

**Power Management**

- 1.8V / 3.3V I/O Power
- 1.2V / 2.5V / 3.3V Analog Power
- 1.2V Core Power

**Operating Frequency**

- Max. 148.5MHz – ISP / MCU
- Max. 180MHz – DDR SDRAM

**Operating Ambient Temperature**

- -20˚C ~ +85˚C

**Package**

- 144 ball FBGA 10mm x 10mm

## 2. Pin Diagram

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | HSI | GPIO 21 | GPIO 23 | GPIO 25 | YO3 | YO7 | DCKO _C | CO3 | CO7 | GPIO 7 | GPIO 6 | GPIO 19 |
| B | VSI | GPIO 20 | GPIO 22 | GPIO 24 | YO2 | YO6 | DCKO_Y | CO2 | CO6 | GPIO 4 | GPIO 5 | GPIO 18 |
| C | TP1 | GPIO 12 | MCKO | GPIO 3 | YO1 | YO5 | YO9 | CO1 | CO5 | CO9 | GPIO 14 | GPIO 17 |
| D | TP0 | RSTX | NC | GPIO 2 | YO0 | YO4 | YO8 | CO0 | CO4 | CO8 | GPIO 13 | GPIO 16 |
| E | XI2 | TP2 | VDDC | GPIO 1 | AGND_ SDR | VDDQ_ SS | VDDQ_ BT | VDDQ_ BT | AGND_ SDT | AVDD_S DT33 | RX0 | SDITP |
| F | NC | NC | AVDD_ LV33 | GPIO0 | NC | VDDC | GND | GND | XI1 | AVDD_ SDT | TX0 | SDITM |
| G | NC | NC | AVDD_ LV | VDDQ | VDDO_ ICIO | VDDC | GND | AVDD_ DAC | XI0 | AVDD_ PLL | GPIO 15 | UCCDI |
| H | LVD2N | LVD2P | LVD0N | LVD0P | VDDC | VDDC | GND | SFDQ0 | SFCKO | VDDQ | AGND | COAX |
| J | LVD3N | LVD3P | LVD1N | LVD1P | VDDC | VDDC | GND | SFDQ1 | SFCSN | VDDC | REXTD | COMP |
| K | LVD4N | LVD4P | LVCLKN | LVCLKP | GPIO 10 | GPIO 8 | GND | SFDQ2 | SFDQ3 | VDDC | DAC_ VREF | CVBS |
| L | LVD6N | LVD6P | LVD5N | LVD5P | GPIO 11 | GPIO 9 | GND | GND | GND | VDDQ_ DDR | ADC0 | ADCI2 |
| M | LVD7N | LVD7P | GPIO 26 | GPIO 27 | GPIO 28 | GPIO 29 | GPIO 30 | GPIO 31 | GND | VDDQ_ DDR | ADC_ VREF | ADCI1 |

Figure 2-1. EN870 Pin Diagram (Top View)

# 3. I/O Information

## 3.1. Pin Description

| No. | Pin Name | I/O | Function | |
|---|---|---|---|---|
| D2 | RSTX | I | System Reset | |
| G9 | XI0 | I | System Clock 0 | |
| F9 | XI1 | I | System Clock 1 | |
| E1 | XI2 | I | System Clock 2 | |
| D1 | TP0 | I | Test Pin 0 | |
| C1 | TP1 | I | Test Pin 1 | |
| E2 | TP2 | I | Test Pin 2 | |
| B1 | VSI | I | Vertical Sync in/output for sensor | |
| A1 | HSI | I | Horizontal Sync in/output for sensor | |
| C3 | MCKO | I | Sensor Operating clock | |
| H4 | LVD0P | I | Sub-LVDS positive lane 0 | CSI-2 positive lane 0 |
| H3 | LVD0N | I | Sub-LVDS negative lane 0 | CSI-2 negative lane 0 |
| J4 | LVD1P | I | Sub-LVDS positive lane 1 | CSI-2 positive lane 1 |
| J3 | LVD1N | I | Sub-LVDS negative lane 1 | CSI-2 negative lane 1 |
| H2 | LVD2P | I | Sub-LVDS positive lane 2 | CSI-2 positive lane 2 |
| H1 | LVD2N | I | Sub-LVDS negative lane 2 | CSI-2 negative lane 2 |
| J2 | LVD3P | I | Sub-LVDS positive lane 3 | CSI-2 positive lane 3 |
| J1 | LVD3N | I | Sub-LVDS negative lane 3 | CSI-2 negative lane 3 |
| K2 | LVD4P | I | Sub-LVDS positive lane 4 | CSI-2 positive lane 4 |
| K1 | LVD4N | I | Sub-LVDS negative lane 4 | CSI-2 negative lane 4 |
| L4 | LVD5P | I | Sub-LVDS positive lane 5 | CSI-2 positive lane 5 |
| L3 | LVD5N | I | Sub-LVDS negative lane 5 | CSI-2 negative lane 5 |
| L2 | LVD6P | I | Sub-LVDS positive lane 6 | CSI-2 positive lane 6 |
| L1 | LVD6N | I | Sub-LVDS negative lane 6 | CSI-2 negative lane 6 |
| M2 | LVD7P | I | Sub-LVDS positive lane 7 | CSI-2 positive lane 7 |
| M1 | LVD7N | I | Sub-LVDS negative lane 7 | CSI-2 negative lane 7 |
| K4 | LVCLKP | I | Sub-LVDS positive clock | CSI-2 positive clock |
| K3 | LVCLKN | I | Sub-LVDS negative clock | CSI-2 negative clock |
| D5 | VD0 | O | Video Data0 | **Mode A(20bit)**<br>VD19:10 = Luma9:0<br>VD9:0 = Chroma9:0<br><br>**Mode B(20bit)**<br>VD19:10 = Chroma9:0<br>VD9:0 = Luma9:0<br><br>*For 16bit, two LSB of Luma/Chroma is ignored. |
| C5 | VD1 | O | Video Data1 | |
| B5 | VD2 | O | Video Data2 | |
| A5 | VD3 | O | Video Data3 | |
| D6 | VD4 | O | Video Data4 | |
| C6 | VD5 | O | Video Data5 | |
| B6 | VD6 | O | Video Data6 | |
| A6 | VD7 | O | Video Data7 | |

| | | | | |
|---|---|---|---|---|
| D7 | VD8 | O | Video Data8 | **Mode C(10bit)**<br>VD19:10 =Multiplexed Luma/Chroma<br><br>**Mode D(10bit)**<br>VD9:0 =Multiplexed Luma/Chroma<br><br>*For 8bit, two LSB of Multiplexed Luma/Chroma is ignored.<br><br>***Mode is configured by S/W setting.**<br>***Both PCK_A and PCK_B can be used in any mode.**<br>***Bit reversal is possible.** |
| C7 | VD9 | O | Video Data9 | |
| B7 | PCK_A | O | Video Data Clock A | |
| D8 | VD10 | O | Video Data10 | |
| C8 | VD11 | O | Video Data11 | |
| B8 | VD12 | O | Video Data12 | |
| A8 | VD13 | O | Video Data13 | |
| D9 | VD14 | O | Video Data14 | |
| C9 | VD15 | O | Video Data15 | |
| B9 | VD16 | O | Video Data16 | |
| A9 | VD17 | O | Video Data17 | |
| D10 | VD18 | O | Video Data18 | |
| C10 | VD19 | O | Video Data19 | |
| A7 | PCK_B | O | Video Data Clock B | |
| E12 | SDITP | O | EX-SDI serial data positive output | |
| F12 | SDITM | O | EX-SDI serial data negative output | |
| G1 | NC | | | |
| G2 | NC | | | |
| F1 | NC | | | |
| F2 | NC | | | |
| H12 | COAX | O | External control signal input via CVBS | |
| K12 | CVBS | O | DAC output for CVBS (or HD-Analog) | |
| K11 | DAC_VREF | I/O | Voltage reference | |
| J12 | COMP | O | A capacitor with 0.01uF is connected between COMP and ground | |
| J11 | REXTD | I/O | A resistor with 200ohm is connected between REXTD and ground. | |
| G12 | UCCDI | I | UCC input | |
| D3 | NC | | | |
| E11 | RX0 | I | UART receive input | |
| F11 | TX0 | O | UART transmit output | |
| L11 | ADC0 | I | Internal ADC input 0 | |
| M12 | ADC1 | I | Internal ADC input 1 | |
| L12 | ADC2 | I | Internal ADC input 2 | |
| M11 | ADC_VREF | I | ADC voltage reference input, 0.01xADC_VREF < ADC0~2 < 0.99xADC_VREF | |
| H8 | SFDQ0 | I/O | External serial flash data 0 | |
| J8 | SFDQ1 | I/O | External serial flash data 1 | |
| K8 | SFDQ2 | I/O | External serial flash data 2 | |
| K9 | SFDQ3 | I/O | External serial flash data 3 | |
| J9 | SFCSN | O | External serial flash chip select output | |
| H9 | SFCKO | O | External serial flash clock output | |
| F4 | GPIO0 | I/O | General purpose IO | SPI-CS (sensor I/F) |

| | | | | | |
|---|---|---|---|---|---|
| E4 | GPIO1 | I/O | General purpose IO | SPI-MOSI (sensor I/F) | I2C-SDA (sensor I/F) |
| D4 | GPIO2 | I/O | General purpose IO | SPI-CK (sensor I/F) | I2C-SCL (sensor I/F) |
| C4 | GPIO3 | I/O | General purpose IO | SPI-MISO (sensor I/F) | |
| B10 | GPIO4 | I/O | General purpose IO | I2C-SCL | |
| B11 | GPIO5 | I/O | General purpose IO | I2C-SDA | |
| A11 | GPIO6 | I/O | General purpose IO | PWM0 | CAP0 |
| A10 | GPIO7 | I/O | General purpose IO | PWM1 | CAP1 |
| K6 | GPIO8 | I/O | General purpose IO | SPI-CS | |
| L6 | GPIO9 | I/O | General purpose IO | SPI-MOSI | |
| K5 | GPIO10 | I/O | General purpose IO | SPI-CK | |
| L5 | GPIO11 | I/O | General purpose IO | SPI-MISO | |
| C2 | GPIO12 | I/O | General purpose IO | PWM2 | CAP2 |
| D11 | GPIO13 | I/O | General purpose IO | External IRQ 0 | |
| C11 | GPIO14 | I/O | General purpose IO | RXD1 | |
| G11 | GPIO15 | I/O | General purpose IO | TXD1 | |
| D12 | GPIO16 | I/O | General purpose IO | I2S Audio in | |
| C12 | GPIO17 | I/O | General purpose IO | I2S MCK | |
| B12 | GPIO18 | I/O | General purpose IO | I2S WCK | |
| A12 | GPIO19 | I/O | General purpose IO | I2S BCK | |
| B2 | GPIO20 | I/O | General purpose IO | PWM3 | CAP3 |
| A2 | GPIO21 | I/O | General purpose IO | PWM4 | CAP4 |
| B3 | GPIO22 | I/O | General purpose IO | PWM5 | CAP5 |
| A3 | GPIO23 | I/O | General purpose IO | External IRQ 1 | |
| B4 | GPIO24 | I/O | General purpose IO | HSO for parallel output | |
| A4 | GPIO25 | I/O | General purpose IO | VSO for parallel output | |
| M3 | GPIO26 | I/O | General purpose IO | DENO for parallel output | |
| M4 | GPIO27 | I/O | General purpose IO | FLDO for parallel output | |
| M5 | GPIO28 | I/O | General purpose IO | | |
| M6 | GPIO29 | I/O | General purpose IO | | |
| M7 | GPIO30 | I/O | General purpose IO | | |
| M8 | GPIO31 | I/O | General purpose IO | | |
| E3<br>F6<br>G6<br>H5<br>H6<br>J5<br>J6<br>J10<br>K10 | VDDC | P | Core power 1.2V | | |
| E6 | VDDQ_SS | P | Sensor I/F IO power 1.8V | | |
| E7<br>E8 | VDDQ_BT | P | BT-1120 IO power 3.3V | | |
| G4 | VDDQ | P | Normal IO power 3.3V | | |

| | | | |
|---|---|---|---|
| H10 | | | |
| G5 | VDDQ_ICIO | P | ICIO power 3.3V |
| L10<br>M10 | VDDQ_DDR | P | DDR IO power 1.8V |
| G10 | AVDD_PLL | P | PLL PHY power 1.2V |
| F10 | AVDD_SDT | P | SDI-TX PHY power 1.2V |
| F5 | NC | | |
| G3 | AVDD_LV | P | LVDS/MIPI PHY power 1.2V |
| G8 | AVDD_DAC | P | DAC PHY power 2.5V |
| F3 | AVDD_LV33 | P | LVDS/MIPI PHY power 3.3V |
| E10 | AVDD_SDT33 | P | SDI-TX PHY power 3.3V |
| F7<br>F8<br>G7<br>H7<br>J7<br>K7<br>L7<br>L8<br>L9<br>M9 | GND | P | Digital Ground |
| H11 | AGND | P | Analog Ground |
| E9 | AGND_SDT | P | SDI-TX Analog Ground |
| E5 | AGND_SDR | P | SDI-TX Analog Ground |

## 3.2. I/O Power Information

| Power Name | I/O | Related IO | Voltage |
|---|---|---|---|
| VDDQ_SS | P | HSI, VSI, MCKO, GPIO0, GPIO1, GPIO2, GPIO3 | 1.8V |
| VDDQ | P | GPIO4~19,Tx0, SFCKO, SFCSN, SFDQ0~3 | 3.3V |
| VDDQ_BT | P | DCKO_Y, DCKO_C, YO0~9, CO0~9 | 3.3V |
| AVDD_DAC | P | CVBS | 2.5V |
| AVDD_LV33 | P | LVD0P~ LVD9P, LVD0N ~ LVD9N, LVDCKP, LVDCKN | 3.3V |
| AVDD_SDT33 | P | SDITP, SDITM | 3.3V |
| VDDQ_ICIO | P | GPIO20~31 | 3.3V |

Table 3-1. Power information

# 4. Block Diagram

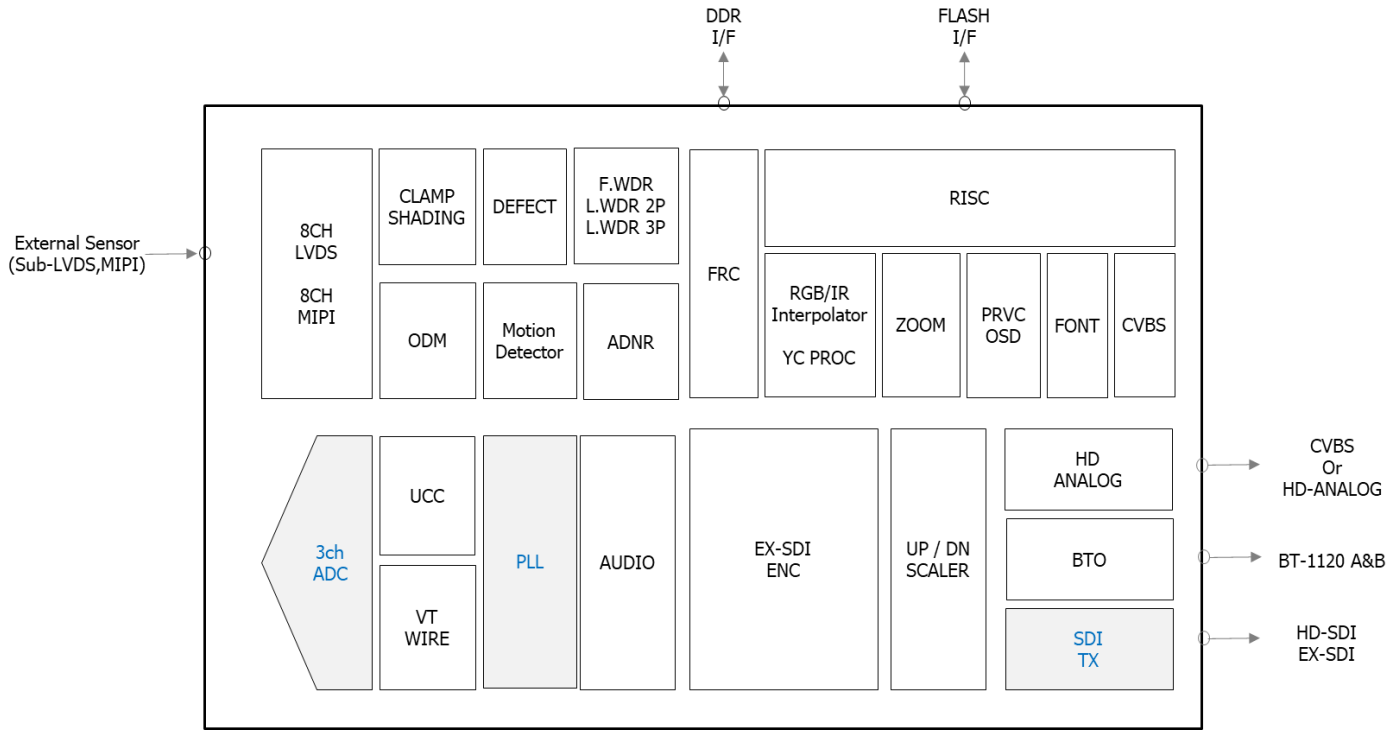



Figure 4-1. Block diagram

CMOS Image sensor has RGB Bayer structure, so the input image must be RGB Bayer structured format (resolution 1-2Mpixel). The output from the DSP has three forms: Embedded EX-SDI as Main output, Digital YC (4:2:2) output, and CVBS Analog output is the other.

DSP consists of Pre-Processor, Post-Processor and CPU.

1. Pre Processor performs Digital Clamping, Defect Correction, and Shading Compensation and then performs WDR and then 2D/3D DNR. The DNR output image is then sent to Post-Processor.
   In addition, AE, AF, AWB Optical Detector for feature and motion detection function are also performed.

2. Post Processor uses DDR SDRAM to transmit images to next stage. SDRAM is used to provide synchronization between Pre Processor and Post Processor. The Digital Zoom function is also performed together.

3. Post Processor consists of RGB Interpolator, Y / C Processor, OSD (Privacy, Font, and Test). In addition, it also consists of Timing Generator which controls the output timing.

This module also includes EX-SDI TX/RX, Video Encoder, DAC, Sub-LVDS, ADC and PLL, etc.

# 5. VD port

EN870`s VD port is a 20bit parallel data bus. Basically it follows SMPTE292m standard as well as BT.656.

The VD port is so flexible – Y/C swapping, Bit Reverse – to get an efficient H/W design.

Maximum speed of VD port is 148.5Mbps with 148.5MHz clock (2M@60p 20bit SDR mode).

Data Stream Y

| Y' 1278 | Y' 1279 | EAV (3FFh) | EAV (000h) | EAV (000h) | EAV (XYZ) | LN0 | LN1 | CRC0 | CRC1 | Optional ancillary data space | SAV(3FFh) | SAV(000h) | SAV(000h) | SAV(XYZ) | Y' 0 | Y' 1 | Y' 2 | Y' 3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Data Stream C

| $C'_B$ 639 | $C'_R$ 639 | EAV (3FFh) | EAV (000h) | EAV (000h) | EAV (XYZ) | LN0 | LN1 | CRC0 | CRC1 | Optional ancillary data space | SAV(3FFh) | SAV(000h) | SAV(000h) | SAV(XYZ) | $C'_B$ 0 | $C'_R$ 0 | $C'_B$ 1 | $C'_R$ 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Figure 5-1. BT1120 20bit data stream

Data Stream Y/C

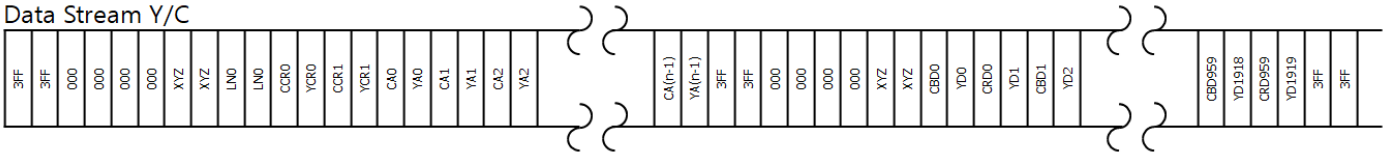



Figure 5-2. BT1120 10bit multiplexed data stream

YC port supported output mode is as follows

- Single rate clock 74.25MHz, Y data 10bit, C data 10bit (
- Single rate clock 148.5MHz, YC data 10bit
- Single rate clock 148.5MHz, Y data 10bit, C data 10bit
- Dual rate clock 148.5MHz, YC data 10bit
- Dual rate clock 148.5MHz, Y data 10bit, C data 10bit

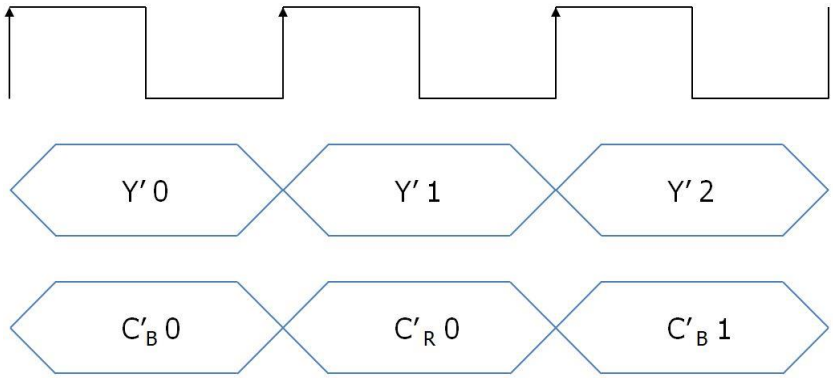



Figure 5-3. Single rate 74.25MHz clock, Y 10bit, C 10bit

The above waveform is a normal BT1120 waveform of 1080p30.

- 1.485Gbps, 74.25MHz, 20bit

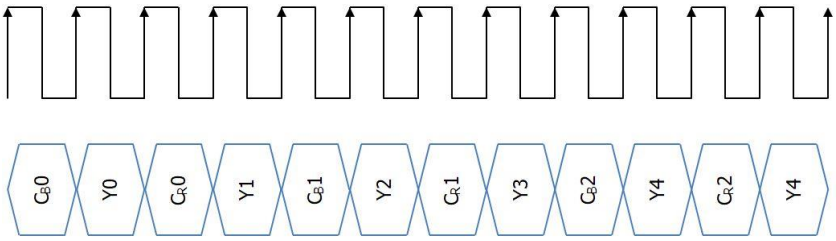



Figure 5-4. Single rate clock 148.5MHz, YC data 10bit

The above waveform is a 1080p30 Multiplexed BT1120 waveform.

- 1.485 Gbps, 148.5 MHz, 10 bit

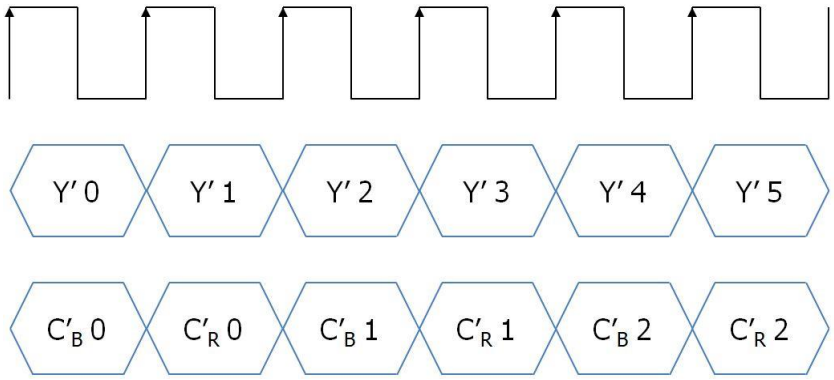



Figure 5-5. Single rate clock 148.5MHz, Y data 10bit, C data 10bit

The upper waveform is Normal BT1120 waveform of 1080p60.

- 2.97 Gbps, 148.5 MHz, 20 bit

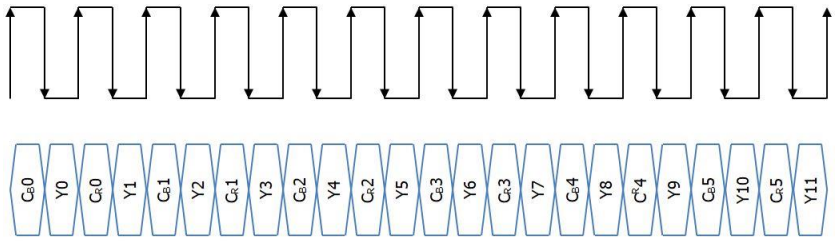



Figure 5-6. Dual rate clock 148.5MHz, YC data 10bit

The upper waveform is a multiplexed BT1120 waveform of 1080p60.

- 2.97Gbps, 148.5MHz DDR, 10bit

# 6. Function Description

## 6.1. RGB Interpolator

This function converts RGB Bayer Pattern to 3 channel RGB. The most important goal of this function is to correct unknown pixel. For this, it is including the following features internally.

- Diagonal frequency compensation Filter
- Minimize mosaic pattern

## 6.2. Wide Dynamic Range compensation (WDR)

This is the ability to expand the dynamic range. This function uses alternative exposure time control method.

- Dual shutter image fusion (Max. 90dB)
- Line by Line WDR (Max. 120dB)
- Based on Bayer pattern
- Spatial adaptive gamma correction

## 6.3. Digital Noise Reducer (2D/3D)

This feature removes noise in images (temporal domain). Temporal noise is reduced by 3D filter using frame memory. Especially,

- 2D noise reducer
- 3D noise reducer
- Based on Bayer pattern

## 6.4. Adaptive Contrast Enhancer (ACE)

This function is a local adaptive contrast enhancement. It uses a histogram analysis and tone mapping method in pixel domain.

- Individual histogram equalization
- Temporal IIR filter
- Adjustable with input image level

## 6.5. Lens Shading Compensation

This function compensates shading effect caused by lens. It uses 2D shading table for compensation.

## 6.6. Defect Detection & Correction

This function corrects the defect of image at run-time. It supports only auto modes.

- Defect Detection method
  Auto detection
  Manual detection: with memory (depth: 1024pixels)
- Edge adaptive defect correction

## 6.7. Optical detector (AE, AF, AWB)

This function detects optical characteristics.

- AE Detector
  Detection Window: 6ea
  Integration of Luminance result and pixel counter in each window
  Histogram of input image (variable detection level)
  Limitation of integration through Clip/Slice control
- AF Detector (for motorized semi AF)
  Detection Window: 1ea
  Integration of the Band Pass Filter output of image and counter in window
  Line Peak and pixel counter
  Noise Slice
  BPF: FIR filter
- AWB Detector
  Detection Window: 1ea

White Zone Detector: Color Map method
Integration of each R, G, B and pixel counter
Counter of saturated Pixels

## 6.8. Edge enhancement

This function enhances the edges of image for sharpness.

- Adjustment edge gain/threshold/limit
- Control negative/positive edge
- Noise slicing and detection of high frequency edge

## 6.9. Gamma Correction

- Gamma control point : 16 point
- 2 gamma tables are controlled at the same time.
- Fixed point on X-axis
- Control each Y/C

## 6.10. Hue Controller

This function adjusts the hue of image.

- Direction gain control with 8 directions
- Hue control with 8 directions

## 6.11. Pseudo Color Suppression

This function has the ability to suppress the color.

- High light color suppression
- Low light color suppression
- Edge color suppression

## 6.12. High Light Masking

This is the ability to mask the high light zone with specific color & level.

## 6.13. Box OSD (32ea, solid effects)

- OSD quantity : 32ea
- Blending effect : 4step
- Box border : solid effects
- Auto zoom position function

## 6.14. Font OSD

This function displays MENU for camera.

- Font size: 16 x 24 pixel (Max. 341 characters)
- Scaling of each H,V
- Line return, page return
- Blending effects with 4 steps
- 4 font color palettes
- Adjustment of character space
- Supports half character size

## 6.15. Motion Object Detector

This function detects the moving objects in image

- Detecting resolution: 32x32 pixels
- Detecting object size: Variable

## 6.16. External Audio Interface

EN870 supports external audio interface, I2S in / output

- I2S Decoder/Encoder

# 7. CPU Specification

## 7.1. CPU General Description

The CPU in this device is operated with an external flash memory. It supports the quad type serial flash memory.

## 7.2. CPU Features

High-performance, low-power 32-bit Ex-RISC 1.0 processor

32-bits Ex-RISC 1.0 Architecture
- Instructions compatible with Ex-RISC 1.0 processor
- Max. 148.5 MHz
- 7 stage pipelines including branch prediction and pre-fetch units
- 32 GPRs
- 16 KB instruction cache, 8 KB data cache

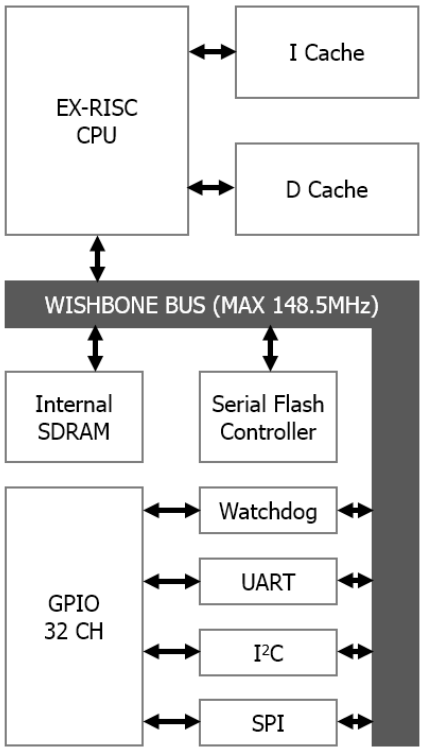
Embedded Memory
- 32 KB internal SRAM x 4

Special Function
- Serial flash memory access
- Support quad, single data access

Peripherals
- 2ch UART
- 32ch GPIO with second function
- 2ch I2C controller
- 2ch SPI
- 6ch timer with PWM output
- 32bit counter Watchdog function

Operating frequency
- Max. 148.5 MHz

## 7.3. CPU Block Diagram




## 7.4. Address map

| Address | Function |
|---|---|
| 0xF0000000 | Serial flash controller |
| 0xF1000000 | UART controller |
| 0xF2000000 | GPIO controller |
| 0xF3000000 | I2C controller |
| 0xF4000000 | SPI0 controller |
| 0xF5000000 | SPI1 controller |
| 0xF6000000 | TIMER / PWM controller |
| 0xF7000000 | Watchdog timer controller |

Table 7-1. Table Internal CPU memory map

# 8. Electrical Characteristics

## 8.1. Absolute Maximum Ratings

(I/O Power: 1.8V / 3.3V)

| Symbol | Parameter | Rating | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| VDDC | DC Internal Voltage | 1.08 | 1.2 | 1.32 | V |
| VIN | DC Input Voltage(1.8V) | 1.62 | 1.8 | 1.98 | V |
| | DC Input Voltage(3.3V) | 2.97 | 3.3 | 3.63 | V |
| VOUT | DC Output Voltage(1.8V) | 1.62 | 1.8 | 1.98 | V |
| | DC Output Voltage(3.3V) | 2.97 | 3.3 | 3.63 | V |
| Latch | Latch-up Current | ±100 | | | mA |

## 8.2. Recommended Operating Conditions

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| VDDC | DC Internal Voltage | 1.2V±0.12 | V |
| VIN | DC Input Voltage(1.8V) | 1.8V±0.18 | V |
| | DC Input Voltage(3.3V) | 3.3V±0.33 | V |
| VOUT | DC Output Voltage(1.8V) | 1.8V±0.18 | V |
| | DC Output Voltage(3.3V) | 3.3V±0.33 | V |
| TOPR | Operating Ambient Temperature | -20 ~ 85 | ℃ |
| TSTG | Storage Temperature | -40 ~ 125 | ℃ |

## 8.3. Static Characteristics

| | Level | | | Unit | Note |
|---|---|---|---|---|---|
| | Pin | Target | Ref. | | |
| Human Body Model | All | ±2,000 ↑ | | V | |
| Charged Device Model | All | ±500 ↑ | | V | |

## 8.4. DC Electrical Characteristics

| Item | | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| | | AVDD_SDT | $AVDD_{SDT}$ | | 1.08 | 1.2 | 1.32 | V |
| | | AVDD_SDT33 | $AVDD_{SDT33}$ | | 2.97 | 3.3 | 3.63 | V |
| | | AVDD_PLL | $AVDD_{PLL}$ | | 1.08 | 1.2 | 1.32 | V |
| | | AVDD_LV | $AVDD_{LV}$ | | 1.08 | 1.2 | 1.32 | V |
| | | AVDD_LV33 | $AVDD_{LV33}$ | | 2.97 | 3.3 | 3.63 | V |
| | | AVDD_DAC | $AVDD_{DAC}$ | | 2.25 | 2.5 | 2.75 | V |
| | Digital | VDDQ | VDDQ | | 2.97 | 3.3 | 3.63 | V |
| | | VDDQ_BT | $VDDQ_{BT}$ | | 1.62/2.97 | 1.8/3.3 | 1.98/3.63 | V |
| | | VDDQ_SS | $VDDQ_{SS}$ | | 1.62 | 1.8 | 1.98 | V |
| | | VDDQ_DDR | $VDDQ_{DDR}$ | | 1.62 | 1.8 | 1.98 | V |
| | | VDDC | VDDC | | 1.08 | 1.2 | 1.32 | V |
| | | VDDQ_ICIO | $VDDQ_{ICIO}$ | | 2.97 | 3.3 | 3.63 | V |
| Digital input voltage | | LVD0P~LVD7P<br>LVD0N~LVD7N<br>LVDCKP<br>LVDCKN | $\triangle V_{LCM}$ | | -25 | | 25 | mV |
| | | | $\triangle V_{LD}$ | | -25 | | 25 | mV |
| | | | $V_{LD}$ | | 100 | 150 | 200 | mV |
| | | | $Z_{dif}$ | | 98 | 100 | 102 | Ω |
| | | | $V_{LCM}$ | | 0.8 | 0.9 | 1 | V |
| | | RSTX, XI0, XI1, XI2,<br>TP0~2, GPIO4~19, RX0,<br>SFDQ0~3, UCCDI, COAX | VIH | | 0.7 VDDQ | | 4 | V |
| | | | VIL | | -0.3 | | 0.3 VDDQ | V |
| | | YO0~9, CO0~9 | $VIH_{BT}$ | | 0.7 $VDDQ_{BT}$ | | 4 | V |
| | | | $VIL_{BT}$ | | -0.3 | | 0.3 $VDDQ_{BT}$ | V |
| | | VSI, HSI, GPIO0~3 | $VIH_{SS}$ | | 0.7 $VDDQ_{SS}$ | | 4 | V |
| | | | $VIL_{SS}$ | | -0.3 | | 0.3 $VDDQ_{SS}$ | V |
| | | GPIO20~GPIO31 | $VIH_{ICIO}$ | | 0.7 $VDDQ_{ICIO}$ | | 4 | V |
| | | | $VIL_{ICIO}$ | | -0.3 | | 0.3 $VDDQ_{ICIO}$ | V |
| Digital output voltage | | GPIO4~19, TX0,<br>SFDQ0~3, SFCKO, SFCSN | VOH | | VDDQ-0.2 | | | V |
| | | | VOL | | | | 0.2 | V |
| | | DCKO_Y, DCKO_C,<br>YO0~9, CO0~9 | $VOH_{BT}$ | | $VDDQ_{BT}$-0.2 | | | V |
| | | | $VOL_{BT}$ | | | | 0.2 | V |
| | | MCKO, VSI, HSI, GPIO0~3 | $VOH_{SS}$ | | $VDDQ_{SS}$-0.2 | | | V |
| | | | $VOL_{SS}$ | | | | 0.2 | V |
| | | GPIO20~GPIO31 | $VOH_{ICIO}$ | | $VDDQ_{ICIO}$-0.2 | | | V |
| | | | $VOL_{ICIO}$ | | | | 0.2 | V |
| Serial output Voltage (Common) | | SDIP, SDIM | $V_{CMO}$ | | | $AVDD_{SDI33}$ -$\triangle V_{SDO}$/2 | | V |

## 8.5. AC Electrical Characteristics

### 1) Main reference clock

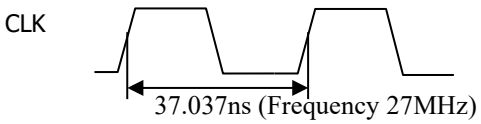



Figure 8-1. main clock description

### 2) Input LVDS data characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Differential motion skew time | $T_{SK}$ | | | 100 | ps |
| Duty ratio | $T_H/T_L$ | 45 | 50 | 55 | % |
| DDR clock frequency | f | | | | MHz |

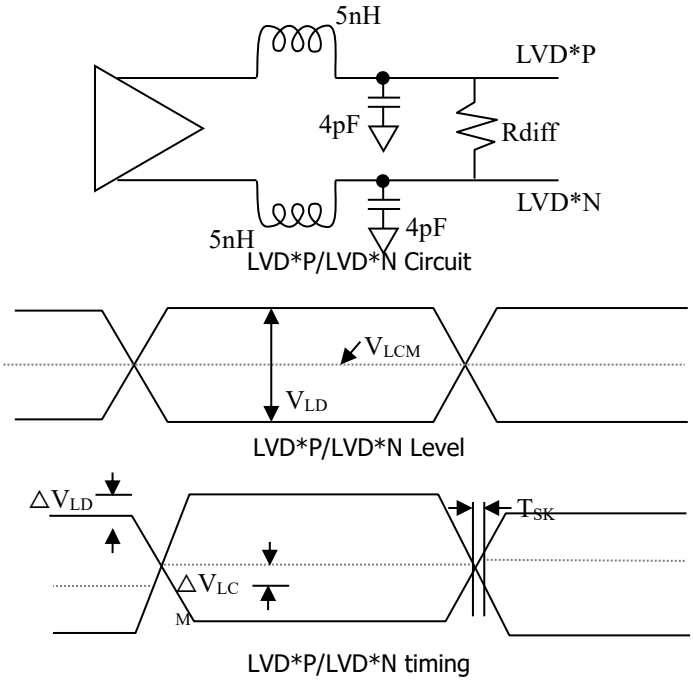



Figure 8-2. LVDS Timing diagram

### 3) Video output characteristics

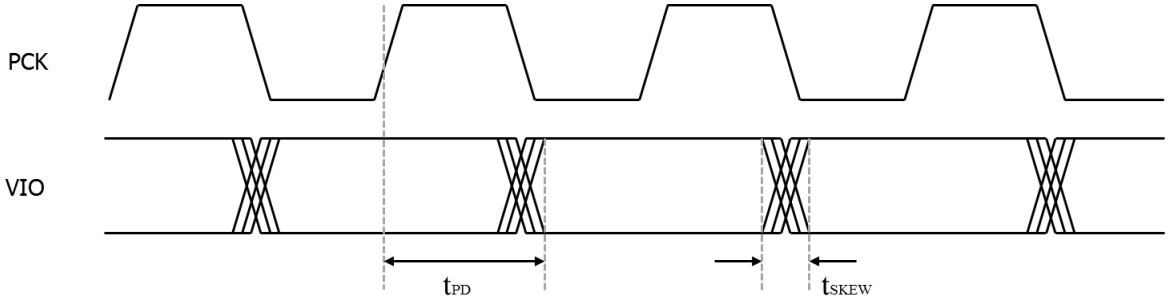



Figure 8-3. VD data output timing diagram

| Interface | Symbol | Definition | Min. | | Max. | | Unit |
|---|---|---|---|---|---|---|---|
| | | | VD_A | VD_B | VD_A | VD_B | |
| HD 30p SDR 10bit@148.5MHz | tPD | PCLK to Data | 1.04 | 1.04 | 3.33 | 3.18 | ns |
| | tSKEW | Skew | 0.10 | 0.10 | 0.26 | 0.33 | ns |
| HD 60p DDR 10bit@148.5MHz | tPD | PCLK to Data | 1.00 | 1.00 | 3.29 | 2.82 | ns |
| | tSKEW | Skew | 0.09 | 0.08 | 0.22 | 0.20 | ns |
| HD 60p SDR mode 20bit@148.5MHz | tPD | PCLK to Data | 1.09 | | 2.81 | | ns |
| | tSKEW | Skew | 0.1 | | 0.42 | | ns |

Table 8-1. VD data output timing value

## 4) I2S characteristics

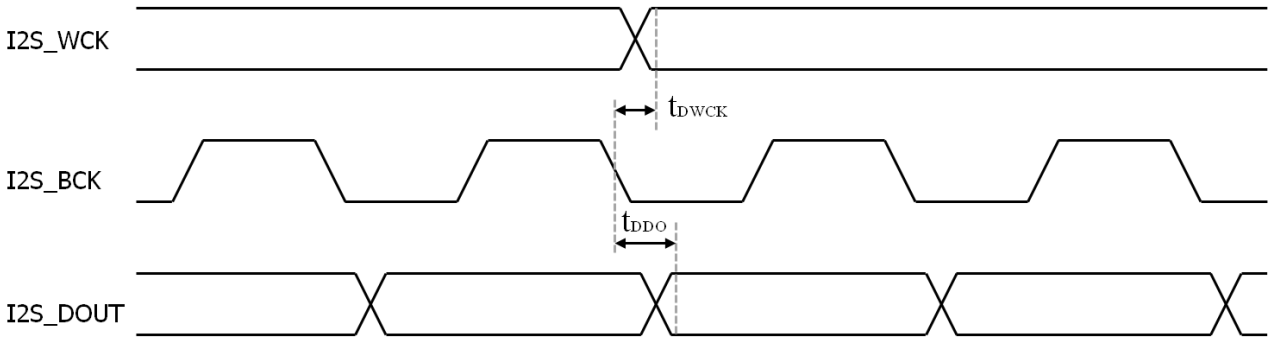



Figure 8-4. I2S timing diagram

| Symbol | Definition | Min. | Max. | Unit |
|---|---|---|---|---|
| tDWCK | I2S_WCK delay | 0.01 | 0.55 | ns |
| tDDO | I2S_DOUT delay | 0.75 | 3.84 | ns |

Table 8-2. I2S timing value

# 9. Power on Sequence

## 9.1. Power, Reset and Clock

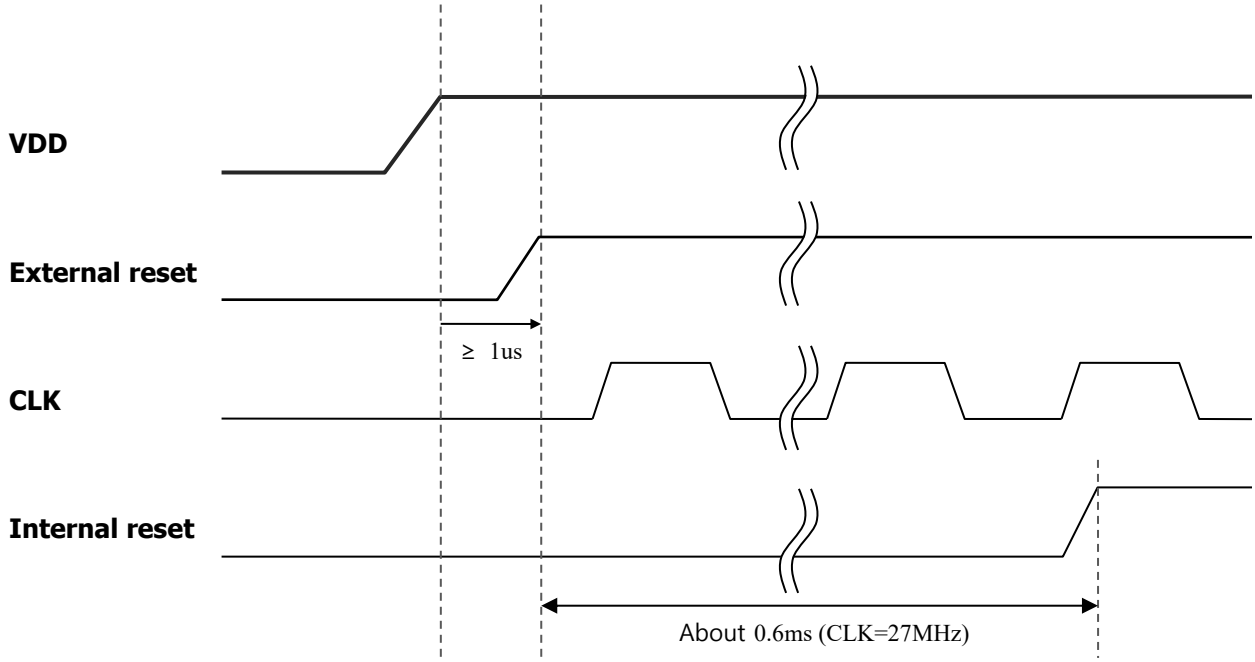



Figure 9-1. Reset sequence diagram

After power on, and when external reset is "High", CLK comes in and internal reset will be "high" after 1200 us (CLK at 27 MHz standard). All processes will work when the internal reset is high. The internal VDDC power is enabling after External VDDQ power up.

# 10. Power Consumption

*2M60p operation

| Power Group | Voltage(V) | Current(mA) | Power(mW) | Description |
|---|---|---|---|---|
| VDDC | 1.2 | 330 | 396 | Core |
| VDDQ | 3.3 | 1.38 | 4.554 | Normal IO |
| VDDQ_DDR | 1.8 | 67.6 | 121.68 | Internal DDR IO |
| VDDQ_BT | 3.3 | 46.3 | 152.79 | Parallel(BT1120) |
| VDDQ_ICIO | 3.3 | TBD | TBD | Inter connection |
| VDDQ_SS | 1.8 | 1.37 | 2.466 | Sensor I/F |
| AVDD_LV | 1.2 | 1 | 1.2 | |
| AVDD_LV33 | 3.3 | 6.2 | 20.46 | |
| AVDD_DAC | 2.5 | 22.4 | 56 | Internal DAC |
| AVDD_PLL | 1.2 | 8.1 | 9.72 | Internal PLL |
| AVDD_SDT | 1.2 | 10.6 | 12.72 | SDI Tx core |
| AVDD_SDT33 | 3.3 | 24.3 | 80.19 | SDI Tx |
| Total | | | 857.78 | - |

Note)

It is not based on all function operation.

It is an actual measurement value.

# 11. EX-SDI Overview

## 11.1. EX-SDI

Generally achievable distance is in inverse proportion to transmission rate. With RG59 cable, transmission distance is approximately 330m in 270Mbps, 160m in 1.485Gbps and 100m in 2.98Gbps.

EX-SDI V1.0 supports only 270Mbps–transmission with 20% image compression. This makes HD-SDI (1.485Gbsp data rate) go over 300m and go over low-end cable.

EX-SDI V2.0 supports not only 270Mbps but also 135Mbps, transmission distance is much longer than V1.0. The expected reach is over 500m with RG59 cable. Furthermore it's helpful to reduce difficulties to use low-end cable such UTP and 3C-2V.

EX-SDI V2.1 supports 2M60p/4M30p video resolution based on 270Mbps bandwidth and supports 4K video resolution based on 1.5Gbps bandwidth. Also compatible with EX-SDI V2.0 and below.

EX-SDI is a visually lossless codec based on JPEG standard. It's processing is simple as shown below figure.

It is composed of compress codec, domain conversion and codec rate controller.

Codec controller controls compression rate while studying optimal point of buffer. Optimal point is where total amount of compressed data is as much as empty buffer size by outputting data in buffer.

Therefore image quality relies on this controller. The PSNR is normally 40dB and more in normal source.

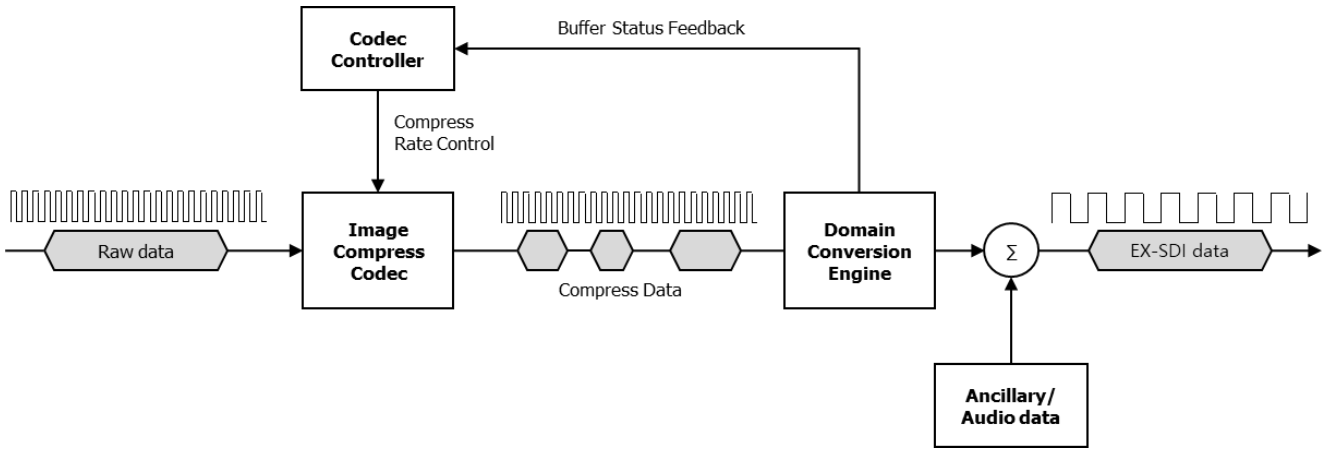



Figure 11-1. EX-SDI compress sequence

| EX-SDI | V1.0 | V2.0 | V2.1 | V3.0(TBD) | Channel Coding | Polarity Free | UCC/PoC |
|---|---|---|---|---|---|---|---|
| 135Mbps | | 720p30 | ← | ← | 8b/10b | X | O |
| | | 720p60 | ← | ← | | | |
| | | 1080p30 | ← | ← | | | |
| 135Mbps+ | | | 720p30 | ← | 8b/10b | X | O |
| | | | 720p60 | ← | | | |
| | | | 1080p30 | ← | | | |
| 270Mbps | 720p30 | ← | ← | ← | Scrambled NRZ | O | X |
| | 720p60 | ← | ← | ← | | | |
| | 1080p30 | ← | ← | ← | | | |
| | | | 1080p60 | ← | 8b/10b | X | O |
| | | | 1440p30 | ← | | | |
| | | | | 2160p30 | | | |
| | | | | 1080p120 | | | |
| 1.5Gbps | | | 2160p30 | ← | Scrambled NRZ | O | O |
| | | | | 2160p60 | 8b/10b | X | O |
| HD-SDI | O | O | X | X | | | |
| Tx device | → | → | → | EN781<br>EN772<br>EN773 | | | |
| | → | → | EN779/EN870 | | | | |
| | → | EN771 | | | | | |
| | EN773V | | | | | | |
| | EN778 | | | | | | |
| Rx device | → | → | → | EN351 | | | |
| | → | → | EN332T/S | | | | |
| | → | → | EN334S | | | | |
| | → | EN332 | | | | | |
| | → | EN334R | | | | | |
| | EN331 | | | | | | |

Table 11-1. EX-SDI generation

| EX-SDI TDM Ver. | V1.0 | V1.1 | Channel Coding | Polarity Free | UCC/PoC |
|---|---|---|---|---|---|
| 270Mbps | | 1080p30 4ch | 8b/10b | X | O |
| 1.5Gbps | 1080p30 8ch | ← | 8b/10b NRZ | O | O |
| | | 1080p60 4ch | 8b/10b | X | |
| | | 1440p30 4ch | | | |
| | | 2160p30 4ch | | | |
| Tx device | → EN332T | EN781 EN772 EN781 | P30 covers P29.97 and P25<br>P60 covers P59.94 and P50<br>1440P 4Mpix : 2560x1440<br>2160P 8Mpix 4K : 3840x2176 | | |
| Rx device | → EN332T EN334U | EN351 | | | |

Table 11-2. EX-SDI TDM generation

## 11.2. UCC (Upstream Communication Channel)

UCC is a function to control a camera in DVR side over Coax cable remotely.

The EN870 has a UCC modulator inside, which can modulate commonly used control signals (UART, Pelco…) with 0.5MHz ~ 10MHz carrier frequency. With an associated UCC filter, modulated data can go upstream to the camera over coax cable while video data is going downstream from the camera.

In addition, it has UART generator in itself. It can make maximum 16byte serial UART data and outputting it to UCC modulator module.

(Please see UCC guide document for more details)

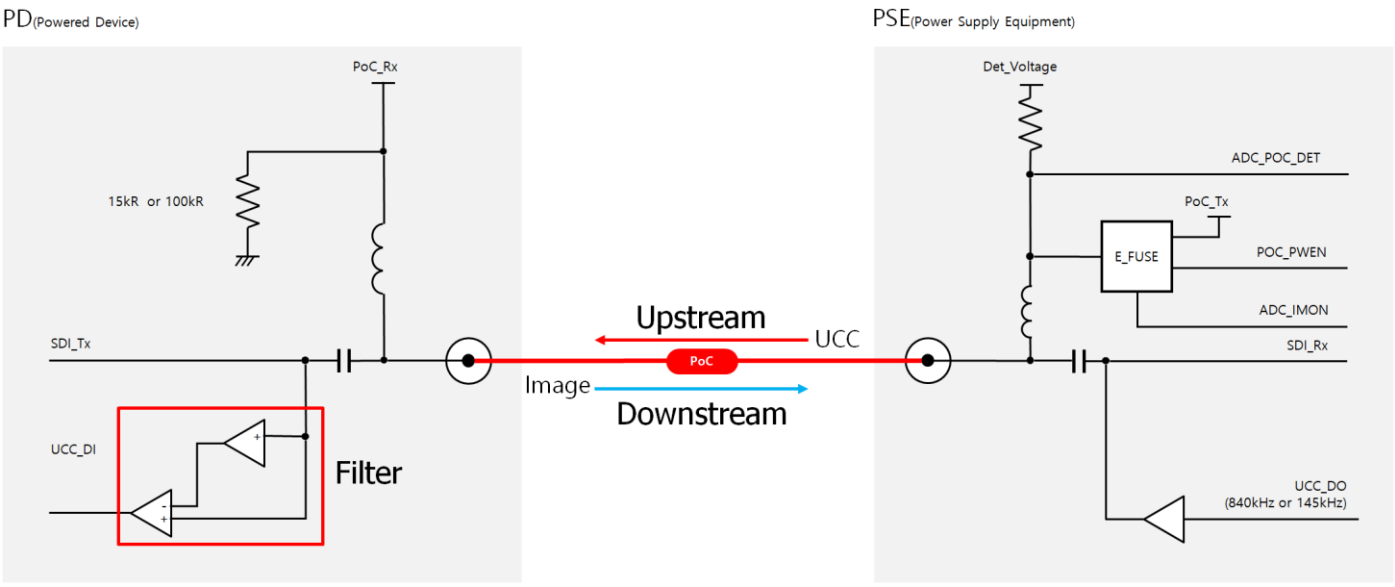



Figure 11-2. UCC & PoC application diagram

## 11.3. Channel coding

The SDI standard defines scrambled NRZ as a channel coding. Scrambling signal makes it statistically likely to have a low DC content for easier handling and have a greater number of transitions for easier clock recovery without any bit redundancy (Polynomial $G1(X) = X^9 + X^4 + 1$, $G2(X) = X + 1$).

In order to convert available signal from SDI to parallel data, NRZI-to-NRZ and descrambling processing must be applied before main processing.

The traditional scrambling method used in SDI has a few advantages like no redundancy and polarity-free. Although under normal condition the scrambled data has high transition with an even ratio of ones to zeros, some scrambled status meets too challenging conditions for the receiver to reconstruct SDI signal.

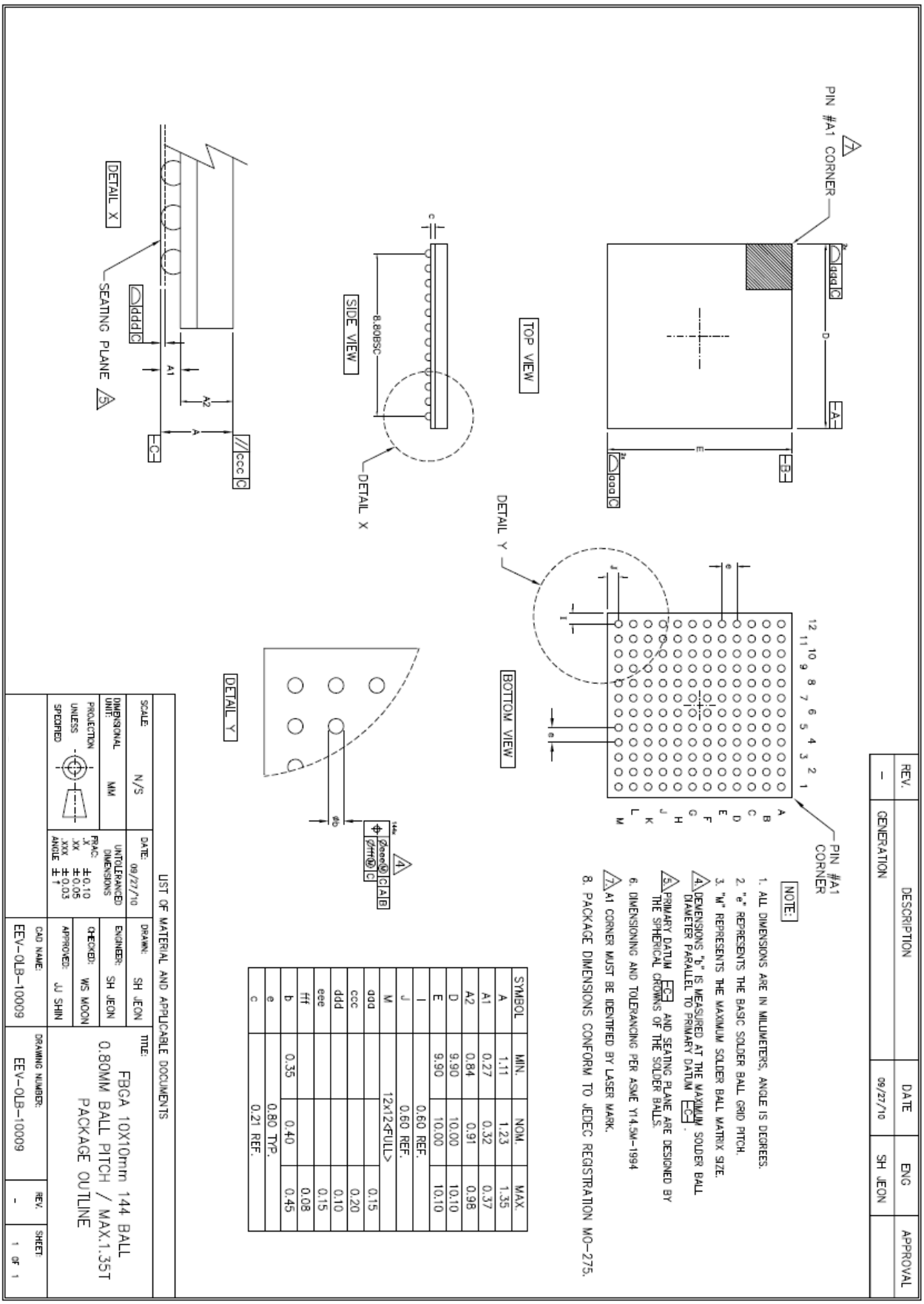
For more reliable communication, EX-SDI 2.0 adopted 8B/10B instead of the scrambled NRZ, even though it has 2 bit redundancy. This helps to achieve DC-balance to reduce the risk of data miss-acquisition in CDR of a receiver side.

| Mode | Data rate (bps) | Signal Encoding | Polarity free |
|---|---|---|---|
| HD-SDI | 1.485G | Scrambled NRZ | O |
| ~~3G-SDI~~ | ~~2.98G~~ | ~~Scrambled NRZ~~ | ~~O~~ |
| EX-SDI V1.0 | 270M | Scrambled NRZ | O |
| EX-SDI V2.0 | 135M | 8b/10b[1)] | X |
| EX-SDI 3G/4M/4K | 270M | 8b/10b[1)] | X |
| EX-SDI 4K V2.1 | 1.485G | Scrambled NRZ | O |
| EX-SDI TDM V1.0 | 1.485G | 8b/10b NRZ | O |
| EX-SDI TDM V1.1 | 270M | 8b/10b[1)] | X |

Note[1)]: EN870 is input polarity-switchable, but it's controlled manually.

Table 11-3. EX-SDI signal encoding and Polarity

# 12. Package Dimension




| REV. | DESCRIPTION | DATE | ENG | APPROVAL |
|---|---|---|---|---|
| – | GENERATION | 09/27/10 | SH JEON | |

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLE IS DEGREES.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE.
4. DIMENSIONS "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DESIGNED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
7. A1 CORNER MUST BE IDENTIFIED BY LASER MARK.
8. PACKAGE DIMENSIONS CONFORM TO JEDEC REGISTRATION MO–275.

| SYMBOL | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 1.11 | 1.23 | 1.35 |
| A1 | 0.27 | 0.32 | 0.37 |
| A2 | 0.84 | 0.91 | 0.98 |
| D | 9.90 | 10.00 | 10.10 |
| E | 9.90 | 10.00 | 10.10 |
| I | | 0.60 REF. | |
| J | | 0.60 REF. | |
| M | | 12x12<FULL> | |
| aaa | | | 0.15 |
| ccc | | | 0.20 |
| ddd | | | 0.10 |
| eee | | | 0.15 |
| fff | | | 0.08 |
| b | 0.35 | 0.40 | 0.45 |
| e | | 0.80 TYP. | |
| c | | 0.21 REF. | |

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

| | | | |
|---|---|---|---|
| SCALE: N/S | DATE: 09/27/10 | DRAWN: SH JEON | TITLE: FBGA 10X10mm 144 BALL 0.80MM BALL PITCH / MAX.1.35T PACKAGE OUTLINE |
| DIMENSIONAL UNIT: MM | UNTOLERANCED DIMENSIONS FRAC: ±.X ±0.10 .XX ±0.05 .XXX ±0.03 ANGLE ±1° | ENGINEER: SH JEON | |
| PROJECTION UNLESS SPECIFIED | | CHECKED: WS MOON | |
| | | APPROVED: JJ SHIN | |
| CAD NAME: EEV-QLB-10009 | | DRAWING NUMBER: EEV-QLB-10009 | REV. - |
| | | | SHEET: 1 OF 1 |