# ENH050Q1-320/450/600 Color TFT-LCD Module Features

## GENERAL DESCRIPTION

Panelview provides optically enhanced solutions to the standard Sharp LQ5AW136 color active matrix LCD module. The first enhancement is an index matching (IM) film lamination to the front surface of the display polarizer.

The IM film is available in two surface treatments - IM/Clear and IM/110 (a 10% diffusion).The second enhancement is the incorporation of a reflective polarizer (RP) to improve brightness by up to 40%. The third enhancement is the addition of prism films (RPp) further increasing the brightness of the display. The module accepts full color video signals conforming to the NTSC(M) and PAL(G-B) system standards.

It can withstand an intense environment, the online dimension is suitable for an automotive display, compact size, compatible with 2DIN size.

Panelview assumes no responsibility for any damage resulting from the use of the device which does not comply with the instructions and the precautions specified in these specification sheets. Panelview does assume the responsibility for the warranty of the enhanced product.

## FEATURES

- Dual mode type. [NTSC(M) and PAL(B-G) standards]
- MBK-PAL enables the 234-scanning lines panel to display a picture with virtually 273-scanning lines.
- TFT-active matrix-LCD drive system with high contrast.
- 74,800 pixels (RBG Stripe configurations and full color) 5" diagonal size.
- Slim, lightweight and compact
  1. Active area/Outline area=70%
  2. Thickness: 16.5mm
  3. Mass: 185g (Max)
- Built-in video interface circuit and control circuit responsive to two sets of standard RGB analog video signals.
- Reduced refleciton as a resuld of low reflectance Black-Matrix and Index Matching (IM) film lamination. IM is available in two surface treatments, IM/Clear (glossy) and IM/110 (10% diffusion).
- It is possible to use both the simultaneous and the independent time sampling.
- An external clock mode is available.
- Optical viewing angle: wide view angle (6 o'clock direction.) (Customer can use this module as a 12 o'clock viewing direction type by using a display rotating function to rotate right/left and up/down scanning direction electrically.)
- This module includes a high luminance edge light that is excellent at low temperature.
- It is possible to use the dimming frequency (PWM) for backlight.

## CONSTRUCTION AND OUTLINE

- Outline dimensions of TFT-LCD module: See Fig. 3
- The module consists of a TFT-LCD panel, driver IC's control PWB mounted with electronic circuits, edge light, frame, front and rear shielding cases. (Backlight driving DC/AC inverter is not built in the module.)

### MECHANICAL SPECIFICATIONS

| Parameter | Specifications | Units |
|---|---|---|
| Display Format | 74,800 | pixels |
| | 960 (W) x RGB x 234 (H) | dots |
| Active Area | 102.2 (W) x 74.8 (H) | mm |
| Screen Size (Diagonal) | 13 (5") | cm |
| Dot Pitch | 0.1065 (W) x 0.3195 (H) | mm |
| Dot Configuration | RGB Stripe configuration | - |
| Outline Dimension (1) | 126.8 (W) x 89.6 (H) x 16.5 (D) | mm |
| Mass | 185 (Max) | g |

Note: This measurement is typical, and see Fig. 3 for details.



*Original specifications created by Sharp.*

# INPUT TERMINALS AND THEIR DESCRIPTIONS

## TTL-LCD Panel Driving Section

(Hi means digital input voltage, Lo means GND.)

| Pin No. | Symbol | I/O | Description | Remarks |
|---|---|---|---|---|
| 1 | HSY | I, O | Input/Output horizontal sync. signal (low active) | (1) |
| 2 | VSY | I, O | Input/Output vertical sync. signal (low active) | (2) |
| 3 | PWM | O | Terminal for output PWM of dimming back light | (3) |
| 4 | NTP | I | Terminal for display mode change of NTSC and PAL | (4) |
| 5 | HRV | I | Turning the direction of horizontal scanning | (5) |
| 6 | VRV | I | Turning the direction of vertical scanning | (6) |
| 7 | VSW | I | Selection signal of two sets of video signals | (7) |
| 8 | SAM | I | Terminal for sampling mode change | (8) |
| 9 | $V_{CDC}$ | I | DC bias voltage adjusting terminal of common electrode driving signal | (9) |
| 10 | VSH | I | Positive power supply voltage | |
| 11 | VBS | I | Composite video signal of sync. seperator | (10) |
| 12 | BRT | I | Brightness adjusting terminal | (11) |
| 13 | VR1 | I | Color video signal (Red) 1 | Positive (On when VSW=Hi.) |
| 14 | VG1 | I | Color video signal (Green) 1 | ↑ |
| 15 | VB1 | I | Color video signal (Blue) 1 | ↑ |
| 16 | VSL | I | Negative power supply voltage | |
| 17 | VR2 | I | Color video signal (Red) 2 | Positive (On when VSW=Lo.) |
| 18 | VG2 | I | Color video signal (Green) 2 | ↑ |
| 19 | VB2 | I | Color video signal (Blue) 2 | ↑ |
| 20 | GND | I | Ground | |
| 21 | CKC | I | Change the input/output direction of CK, HSY and VSY. | (12) |
| 22 | CK | I, O | Input/Output clock signal | (13) |

Note:

1. If CKC='Hi', this terminal outputs horizontal sync. signal in phase with VBS.
   If CKC='Lo', this terminal will be external horizontal sync. input terminal.
2. If CKC='Hi', this terminal outputs vertical sync. signal in phase with VBS.
   If CKC='Lo', this terminal will be external vertical sync. input terminal.
3. PWM signal is used for the PWM dimming frequency and it is easy to get PWM signal dimming by combining both HSY and PWM signals. But use this PWM signal in case of input standard NTSC or PAL signal.
4. This terminal is to switch the display mode, and it is NTSC mode when NTP is 'High' and is PAL mode when NTP is 'Low'.
5. When this terminal is 'High', it will be normal and when it is 'Low', it will display reversely on the horizontal direction.
6. When this terminal is 'High', it will be normal and when it is 'Low', it will display reversely on the vertical direction.
7. This terminal is to switch input for groups of RGB color video signals, and Input 1 (No. 13 to 15) is selected when VSW is 'High' and Input 2 (No. 17 to 19) is selected when VSW is 'Low'.
8. This terminal switches to sampling mode. It is the independent data-sampling timing at RGB dot when SAM is 'High' and it is the simultaneous data-sampling timing at RGB dots when SAM is 'Low'.
9. This terminal is applicable to the DC bias voltage adjusting terminal of the common electrode driving signal. If power supply voltage is typical, it is not necessary to re-adjust it. So, Use it in the open condition. However, in the case that the power supply voltage is changed, or power supply voltage is reduced, adjust it externally to get the best contrast with a resistor that is added to this terminal, or semi-fixed resistor, VCDC in module. A recommended circuit is shown in Fig. 5.
10. The sync. signal which will be input, is negative polarity and is applicable to standard composite sync. signal, negative one in the same pulse level.
11. DC voltage supplied to this terminal, makes the brightness of the screen adjustable, which is the black level of the video signal. Although this is adjusted in the time of delivery to get the best display in the condition of the open terminal, it is also able to be re-adjusted externally with a resistor that can be added to this terminal, or a semi-fixed resistor, BRT, in module. A recommended circuit is shown in Fig. 5.
12. CKC-'Hi', CK.HSY.VSY terminals are output mode. CKC='Lo': CK. HSY. VSY terminals are input mode.
13. If CKC='Hi', this terminal outputs the clock for sure drivers. If CKC='Lo', this terminal will be the external clock input terminal.



*Original specifications created by Sharp.*

## FUNCTIONAL MACHINE AND INPUT/OUTPUT MODE

| | CKC="Hi" | | CKC="Lo" | |
|---|---|---|---|---|
| **Terminal** | **SAM="Hi"** | **SAM="Lo"** | **SAM="Hi"** | **SAM="Lo"** |
| HSY | Output | Output | Input | Input |
| VSY | Output | Output | Input | Input |
| CK | Output "Dot Clock" | Output "Pixel Clock" | Input "Dot Clock" | Input "Pixel Clock" |

## BACKLIGHT DRIVING SECTION

| Terminal | No. | Symbol | I/O | Function |
|---|---|---|---|---|
| CN1 | 1 | VL1 | I | Input terminal (Hi voltage side) [14] |
| | 2 | NC | - | Non connection |
| | 3 | VL2 | I | Input terminal (low voltage side) |

Note:
14. Low Voltage side of DC/AC inverter for backlight driving connects with Ground of inverter circuit.

## ABSOLUTE MAXIMUM RATINGS
## GND = OV, $t_A$ = 25°C

| Parameter | | Symbol | MIN | MAX | Unit |
|---|---|---|---|---|---|
| Positive power supply voltage | | $V_{SH}$ | -0.3 | +9.0 | V |
| Negative power supply voltage | | $V_{SL}$ | -6.0 | +0.3 | V |
| Analog input signals (1) | | $V_I$ | - | 2.0 | Vp-p |
| Digital input/output signals (2) | | $V_I$ | -0.3 | +5.4 | V |
| DC bias voltage of common electrode driving signal | | $V_{CDC}$ | $V_{SL}$ | $V_{SH}$ | V |
| Brightness adjusting terminal | | $V_{BRT}$ | 0 | +5.1 | V |
| Storage temperature (3) | | $t_{STG}$ | -30 | 85 | °C |
| Operating temperature (3, 4) | surface of panel | Top1 | -30 | 85 | °C |
| | environment | Top2 | -30 | 60 | °C |

Notes:
1. VBS, VR1, VG2, VB1, VR2, VG2, VB2 terminals (Video signal)
2. NTP, HRV, VRV, SAM, VSW, HSY, VSY, CKC, CK terminals
3. The temperature of all parts in module should not exceed this rating. Maximum wet-bulb temperature should be less than 58°C. No dew condensation.

# ELECTRICAL CHARACTERISTICS

## RECOMMENDED OPERATING CONDITIONS

TFT-LCD PANEL DRIVING SECTION
GND=0V, $t_A$=25°C

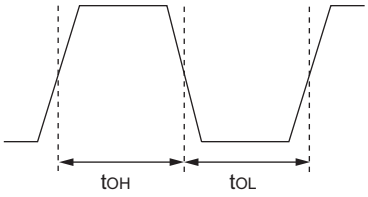
| Parameter | | | Symbol | MIN | TYP | MAX | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Positive power supply voltage | | | $V_{SH}$ | +7.8 | +8.0 | +8.2 | V | (1) |
| Negative power supply voltage | | | $V_{SL}$ | -5.2 | -5.0 | -4.8 | V | |
| Analog input voltage | Amplitude | | $V_{BS}$ | 0.7 | 1.0 | 2.0 | Vp-p | Input resistor is over 10kΩ. |
| | | | $V_I$ | - | 0.7 | - | Vp-p | (2) |
| | DC component | | $V_{IDC}$ | -1.0 | 0 | -1.0 | V | (3) |
| Digital Input voltage | High level | | $V_{IH}$ | -3.7 | - | +5.1 | V | Input resistor is over 10kΩ. (4) |
| | Low level | | $V_{IL}$ | 0 | - | +1.0 | V | |
| | Histeresis | | $V_H$ | 0.4 | - | - | V | |
| Digital output voltage | High level | | $V_{OH}$ | +4.0 | - | +5.5 | V | Load resister is over 60kΩ. (5) |
| | Low level | | $V_{OL}$ | 0 | - | +1.0 | V | |
| Output clock | Duty cycle | | Duty | 45/55 | 50/50 | 55/45 | - | CKC=High (6) |
| | Drive capability | | $I_{OH}$ | - | - | 0.25 | mA | $V_{OH}$=2.6V (7) |
| | | | $I_{OL}$ | -0.28 | - | - | mA | $V_{OL}$=2.3V |
| Input horizontal sync. component | freq. | NTSC | $f_H$ (N) | 15.13 | 15.73 | 16.33 | kHz | CKC=High (8) for VBS terminal |
| | | PAL | $f_H$ (P) | 15.03 | 15.63 | 16.23 | kHz | |
| | pulse width | NTSC | $t_{HI}$ (N) | 4.2 | 4.7 | 5.2 | µs | |
| | | PAL | $t_{HI}$ (P) | 4.2 | 4.7 | 5.2 | µs | |
| | rise time | | $tr_{HI1}$ | - | - | 0.5 | µs | |
| | fall time | | $tf_{HI1}$ | - | - | 0.5 | µs | |
| Input vertical sync. component | freq. | NTSC | $f_V$ (N) | $f_H$/284 | $f_H$/262 | $f_H$/258 | Hz | CKC=High, H=1/$f_H$ (9) for VBS terminal |
| | | PAL | $f_V$ (P) | $f_H$/344 | $f_H$/312 | $f_H$/304 | Hz | |
| | pulse width | NTSC | $t_{VI}$ (N) | - | 3H | - | µs | |
| | | PAL | $t_{VI}$ (P) | - | 2.5H | - | µs | |
| | rise time | | $tr_{VI1}$ | - | - | 0.5 | µs | |
| | fall time | | $tf_{VI1}$ | - | - | 0.5 | µs | |
| Input clock | frequency | | $f_{CLI}$ | 18.2 | 18.9 | 19.6 | MHz | SAM=High CKC=Low (10) |
| | | | $f_{CLI}$ | 6.0 | 6.8 | 7.6 | MHz | SAM=Low |
| | High width | | $t_{WH}$ | 20.0 | - | - | ns | for CK terminal |
| | Low width | | $t_{WL}$ | 20.0 | - | - | ns | |
| | rise time | | $tr_{CLI}$ | - | - | 5.0 | ns | |
| | fall time | | $tf_{CLI}$ | - | - | 5.0 | ns | |
| Input HSY (Horizontal sync.) | frequency | | $f_{HI}$ | $f_{CLI}$/1230 | $f_{CLI}$/1200 | $f_{CLI}$/1170 | Hz | SAM=High CKC=Low (11) |
| | | | $f_{HI}$ | $f_{CLI}$/465 | $f_{CLI}$/435 | $f_{CLI}$/405 | Hz | SAM=Low |
| | pulse width | | $t_{HI}$ | 1.0 | 4.7 | 8.4 | µs | for CK terminal |
| | rise time | | $tr_{HI1}$ | - | - | 0.05 | µs | |
| | fall time | | $tf_{HI1}$ | - | - | 0.05 | µs | |
| Input VSY (Vertical sync.) | frequency | | $f_{VI}$ | 50 | $f_{HI}$/262 | $f_{HI}$/258 | Hz | (12) CKC=Low |
| | pulse width | | $t_{VI}$ (P) | 1H | 3H | 5H | µs | for VSY terminal |
| | rise time | | $tr_{VI1}$ | - | - | 0.5 | µs | |
| | fall time | | $tf_{VI2}$ | - | - | 0.5 | µs | |
| Data set up time | | | $t_{SU1}$ | 25 | - | - | ns | (13) CKC=Low |
| Data hold time | | | $t_{HO1}$ | 25 | - | - | ns | |
| Data set up time | | | $t_{SU2}$ | 1.0 | - | - | µs | (14) |
| Data hold time | | | $t_{HO2}$ | 1.0 | - | - | µs | |

## TFT-LCD PANEL DRIVING SECTION

| Parameter | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| DC bias voltage for common electrode driving signal | $V_{CDC}$ | 0 | +2.0 | +3.0 | V | DC component (15) |
| Terminal voltage applicable to brightness | $V_{BRT}$ | +2.0 | +2.3 | +2.4 | V | |

Notes:

1. Power supply voltage should not be changed after adjusting $V_{CDC}$.
2. VR1, VG1, VB1, VR2, VG2, VB2 terminal (Video signal)
3. VBS, VR1, VG1, VB1, VR2, VG2, VB2 terminals
4. HSY, VSY, NTP, VSW, HRV, VRV, SAM CKC, CK terminal
5. HSY, VSY, CK terminals (output mode)
6. CK terminals (output mode)
7. Duty cycle is defined as follows.




Duty=$t_{OL}/t_{OH}$

8. VBS (horizontal sync. component)
9. VBS (vertical sync. component)
10. CK (input mode)
11. HSY (input mode)
12. VSY (input mode)
13. In case of cKC='Lo', it shows the phase different from HSY to CK. In that case, HSY will be taken at the rise timing of CK.
14. In case of CKC='Lo'. it shows the phase difference from VSY to HSY. In that case, VSY will be taken at the rise timing of HSY.
15. Adjsuting the optimal voltage on every module at the typical value of power supply voltage to get the maximum value of contrast. However, in the case that the power supply voltage is changed, for example the level of power supply voltage is reduced, adjust it externally to get the best contrast with a resistor you add to this terminal, or semifixed resistor, $V_{CDC}$, in module. A recommended circuit is shown in Fig. 5.

## BACKLIGHT DRIVING SECTION

| Parameter | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Lamp Voltage | $V_{L7}$ | 550 | 610 | 670 | Vrms | IL=6.5mArms |
| Lamp current | $I_L$ | 3.0 | 6.5 | 7.0 | mArms | normal operation |
| Lamp frequency | $f_L$ | 20 | - | 70 | KHz | |
| Kickoff voltage | $V_S$ | - | - | 1450 | Vrms | $t_A$ = +25°C |
| | | - | - | 1500 | Vrms | $t_A$ = -30°C |

## POWER COMSUMPTION
## $t_A$ = 25°C

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Positive supply current | $I_{SH}$ | $V_{SH}$ = +8.0V | - | 140 | 170 | mA | |
| Negative supply current | $I_{SL}$ | $V_{SL}$ = -5.0V | - | 55 | 70 | mA | |
| Total | $W_S$ | | - | 1.4 | 1.7 | W | (16) |
| Lamp power consumption | $W_L$ | normal driving | - | 4.0 | - | W | (17) |

16. Excluding backlight section
17. Reference data by calculation ($I_L$ x $V_L$ x 1: number of lump)

### Circuit Diagram

The circuit block diagram of TFT-LCD module is shown in Fig. 4.

BRT, VCDC, external adjusting recommended circuit is shown in Fig. 5.

Caution: Turn the power supply on or off (VSH and VSL) at the same time. Be careful to supply all power voltage before inputting signals.

### Input/Output Signal Waveforms (Fig. 6)

Caution: For the VBS signal, input standard composite video (or sync.) signal applicable to the operating mode which have NTSC (M) or PAL (B-G) and is selected by the NTP signal.

### Dimming Backlight by PWM Timing Chart

If using PWM mode, refer to the timing chart shown in Fig. 7.

## INPUT/OUTPUT SIGNAL TIMING CHART (FIG. 6)
## (CKC=HIGH, NTSC: $f_H$=15.7kHz, $f_V$=60Hz/PAL: $f_H$=15.6kHZ, $f_V$=50Hz)

| Parameter | | Symbol | Min. | Typ. | Max. | Unit | Reward |
|---|---|---|---|---|---|---|---|
| Horizontal sync. output pulse [HSY] | pulse width | $t_{HS2}$ | 3.2 | 3.9 | 4.6 | µs | f=$f_H$ (18) |
| | phase difference | $t_{PD}$ | 0.4 | 1.1 | 1.8 | µs | (19) |
| | rise time | $tr_{HO}$ | - | - | 0.5 | µs | $C_L$=10pF |
| | fall time | $tf_{HO}$ | - | - | 0.5 | µs | |
| Vertical sync. output pulse [VSY] | pulse width | $t_{VS}$ | - | 4H | - | µs | 1H=1/$f_H$ |
| | phase difference | $tv_{HO}$ | - | 11.0 | 28.0 | µs | (20) |
| | rise time | $tr_{VO}$ | - | - | 2.0 | µs | $C_L$=10pF |
| | fall time | $tf_{VO}$ | - | - | 2.0 | µs | |
| Vertical phase difference | odd field | $tp_{V1}$ | - | 1H | - | µs | 1H=1/$f_H$ |
| | even field | $tp_{V2}$ | - | 0.5H | - | µs | (21) |
| Clock output frequency [CK] | NTSC MODE | $f_{CLO}$ | - | fH x $\frac{1201}{2}$ | - | MHz | SAMC="Hi" |
| | PAL MODE | $f_{CLO}$ | - | fH x $\frac{1209}{2}$ | - | MHz | (22) |
| | NTSC MODE | $f_{CLO}$ | - | fH x $\frac{1201}{6}$ | - | MHz | SAMC="Lo" |
| | PAL MODE | $f_{CLO}$ | - | fH x $\frac{1209}{6}$ | - | MHz | (23) |

(Supply voltage conditions: VSH = +8.0V, VSL = 5.0V)

Notes:
18. Adjusted by variable resister (H-POS) in a module.
19. Variable by variable resister (H-POS) in a module.
    adjustment : tpd = 1, 1 ± 0.7 µs
20. Synchronized with HSY, based on falling timing of HSY.
21. VSY signal delays
22. Independent sampling mode.
23. Simultaneous sampling mode.

### Display Time Range

NTSC (M) mode (NTP=High, CKC=High)

Displaying the following range within video signals.

- Horizontally: 12.2 ~ 63 µs — from the falling edge of HSY. (SAM=High)
  12.3 ~ 62.9 µs — from the falling edge of HSY. (SAM-Low)
- Vertically: 20 ~ 253 H — from the falling edge of VSY.

### PAL(B-G) Mode (NTP-Low, CKC=High)

Displaying the following range within video signals.

- Horizontally: 13.0 ~ 63.8 µs — from the falling edge of HSY. (SAM=High)
  13.1 ~ 63.7 µs — from the falling edge of HSY. (SAM-Low)
- Vertically: 26 ~ 298 H — from the falling edge of VSY.

However, the video signals of

(14n+12)H, (14n+20) H/Even field.

(14n+17)H, (14n+23) H/Odd field (n=1, 2..., 20)

are not displayed on the module.

External Clock Mode (NTP=High, CKC='Lo')

- Horizontally: 205 ~ 1164 ck — from the falling edge of HSY. (SAM=High)
  84 ~ 403 ck — from the falling edge of HSY. (SAM-Low)
  (ck means input external clock.)
- Vertically: 20 ~ 253 H — from the falling edge

## OPTICAL CHARACTERISTICS

**$t_A$=25°C**

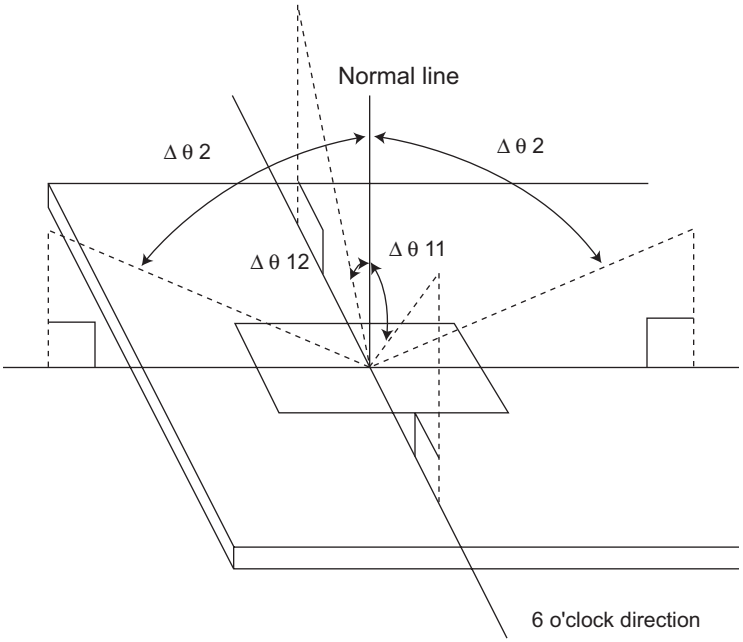
| Parameter | | Symbol | Condition | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Viewing Angle Range | | Δθ11 | CR≥5 | 60 | 65 | - | ° (degree) | (1,2) |
| | | Δθ12 | | 35 | 40 | - | ° (degree) | |
| | | Δθ2 | | 60 | 65 | - | ° (degree) | |
| Contrast Ratio | | CRmax | Optimal | 60 | - | - | - | (2,3) |
| Response Time | Rise | tr | θ = 0° | - | 30 | 60 | ms | (2,4) |
| | Fall | td | | - | 50 | 100 | ms | |
| Luminance | | Y | $I_L$=6.5mArms | 240 | 320 | - | cd/m$^2$ | (5) |
| White Chromaticity | | x | $I_L$=6.5mtVms | 0.263 | 0.313 | 0.363 | - | |
| | | y | $I_L$=6.5mArms | 0.279 | 0.329 | 0.379 | - | |
| Lamp Life Time | +25'C | - | Continuation | 10,000 | - | - | hour | (6) |
| | -30'C | - | Intermission | 2,000 | - | - | time | (7) |

DC/AC inverter for external connection shown in following. Harison Electric Co., Ltd, HIU-288.

Notes:

1. Viewing angle range is defined as follows.

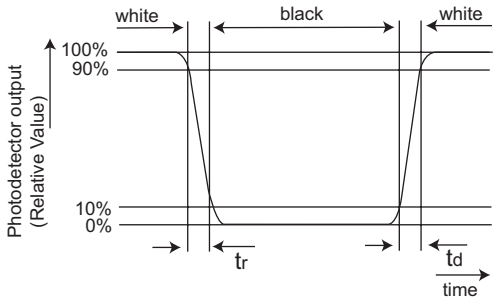
Fig. 1: Definition of Viewing Angle



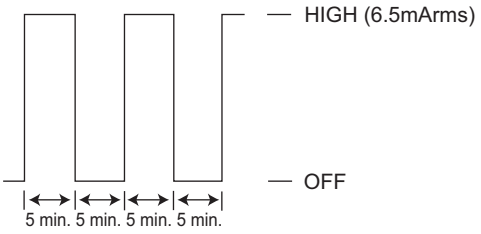

2. Applied voltage conditions:
   a. VCDC is adjusted so as to attain maximum contrast ratio.
   b. Brightness adjusting voltage (BRT) is open.
   c. Input video signal of standard black level and 100% white level.
3. Contrast ratio is defined as follows:

$$\text{Contrast ratio (CR)} = \frac{\text{Photodetector output with LCD being "white"}}{\text{Photodetector output with LCD being "black"}}$$

4. Response time is obtained by measuring the transition time of photodetector output, when input signals are applied so as to make the area "black" from "white" and "white" from "black".




5. Measured on th ecenter area of the panel at a viewing cone 1° by TOPCON luminance meter BM-7. (After 30 minutes operation) DC/AC inverter driving frequency : 49kHz
6. Lamp life time is defined as the time when either "a" or "b" occurs in the continuous operation under the condition of lamp current IL=3~7. 0mArms and PWM dimming 100%~5%. (tA=25°C)
   a. Brightness becomes 50% of the original value.
   b. Kick off voltage at tA=30°C exceeds maximum value, 1500Vrms.
7. The intermittent cycle is defined as a time when brightness becomes 50% of the original value under the condition of following cycle.
   Ambient temperature: -30°C



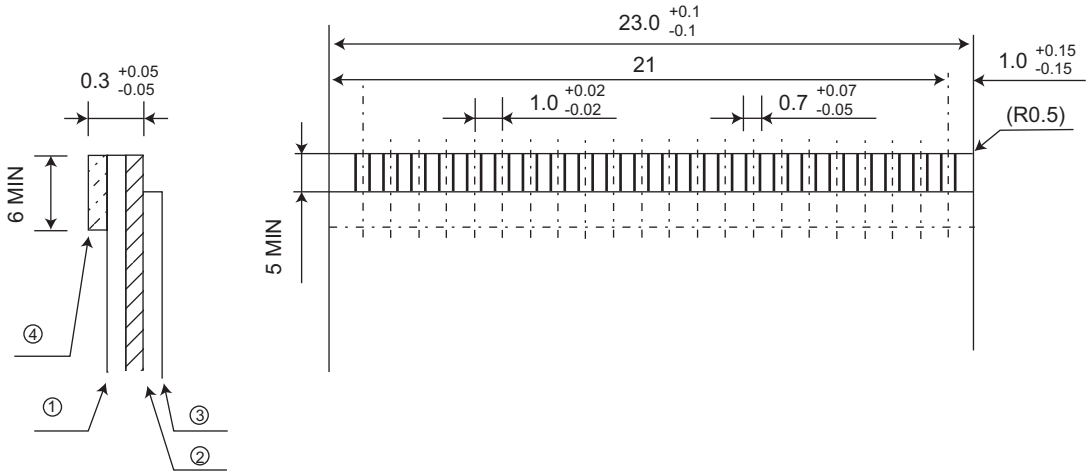
## MECHANICAL CHARACTERISTICS

By applying pressure on the active area it is possible to cause damage to the display.

### Input/Output Connectors Performance

Input/Output connectors for the operation of LCD module (FPC connector 22 pin)

- Applicable FPC Shown in Fig. 3.
- Terminal holding force: more than 0.9N/pin.
  (Each terminal is pulled out at a rate of
  25 ±3mm/min.)




| No. | Name | Materials |
|---|---|---|
| 1 | Base material | Polyimide or equivalent material (25µm thick) |
| 2 | Copper foil | Copper foil (35µm thick) Solder plated in 2 to 12µm |
| 3 | Cover lay | Polyimide or equivalent material |
| 4 | Reinforcing plate | Polyester polyimide or equivalent material (188µm thick) |

(Fig. 3) FPC applied to input/output connector (1.0mm pitch)

## I/O CONNECTOR OF BACKLIGHT DRIVING CIRCUIT

| Symbol | Used Connector | Corresponding connector | Manufacturer |
|---|---|---|---|
| CN1 | BHR=02(8.0)VS-1N | SM02(8.0)B-BHS-TB (wire to board) | JST |
| | | SM02(8.0)B-BHS-1N (wire to board) | JST |
| | | BHMR-03V(wire to wire) | JST |

## DISPLAY QUALITY

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standards.

## HANDLING INSTRUCTIONS

### Mounting the module

The TFT-LCD module is designed to be mounted on equipment using the mounting tabs in the four corners of the module at the rear side. When mounting the module, the M2.6 tapping screw (fastening torque is 0.3 through 0.5N•m) is recommended. Make certain to fix the module on the same plane. Avoid warping or twisting the module.

## PRECAUTIONS IN MOUNTING

Polarizer which is made of soft material and susceptible to flaws must handled carefully. A protective film (Laminator) is applied on the surface to protect it against scratches and dirt. It is recommended to peel off the laminator immediately before use, taking care of static electricity.

Precautions in peeling off the laminator

A) Working environment

When the laminator is peeled off, static electricity may cause dust to stick to the polarizer surface. To avoid this, the following working environment is desired.

a) Floor: Conductive treatment of 1MΩ or more on the title (conductive amt of conductive paint on the tile)

b) Clean room free from dust and with an adhansive mat on the doorway

c) Advisable humidity:50%~70%

Advisable temperature:15°C~27°C

d) Workers shall wear conductive shoes, conductive work clothes, conductive gloves and an earth band.

If the TFT-LCD module metal parts (shielding lid and rear case) become soiled, wipe them with a soft dry cloth.

Wipe off water spots of finger grease immediately.

Prolonged contact with water may cause discoloration or spots.

The TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on a hard surface. Handle with care.

Since CMOS LSI is used in this module, take care of static electricity and ground one's body when handling.

### Precautions in Adjusting Module

Variable resistor on the rear face of the module has been adjusted optimally before shipmetn. Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described here may not be satisfied.

### Caution of Product Design

1. The LCD module shall be protected against water by the waterproof cover.

### Others

1. Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours; liquid crystal is deteriorated by ultraviolet rays.
2. Store the module at a temperature near room temperature. When stored at lower than the rated storage temperature, liquid crystal solidifies, causing the panel to be damaged. When stored at higher than the rated storage temperature, liquid crystal turns into isotropic liquid and may not recover.
3. If LCD panel breaks, the liquid crystal could possibly escape from the panel. Since the liquid crystal is injurious, avoid contact with the eyes or mouth. Wash with soap immediately if contact with the liquid crystal occurs.
4. Observe all other precautionary requirements in handling general electronic components.

## SHIPPING REQUIREMENTS

Carton storage conditions:

Number of layers of carton in stack: 10 layers max

Environmental conditions:

| | |
|---|---|
| Temperature: | 0~40°C |
| Humidity: | 60%RH or less (at 40°C) |
| No dew condensation at low temperature and high humidity, | |
| Atmosphere | Harmful gases such as acid and alkali which corrode electronic components and wires must not be present. |
| Storage period | Approximately 3 months |
| Opening of package | To prevent TFT-LCD module from being damaged by static electricity, adjust the room humidity to 50%RH of higher and make certain one is grounded before opening the package. |

## RELIABILITY TEST

Reliability test conditions for the TFT-LCD module are shown on page 12.

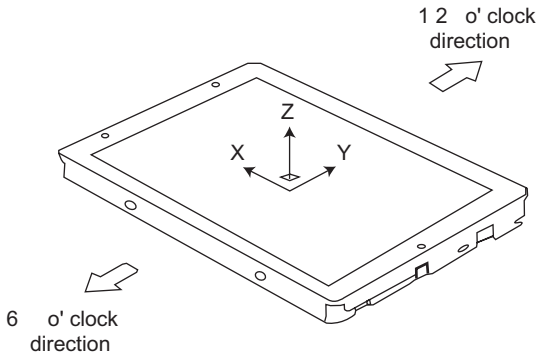
and should be strictly avoided. Image retention may occur when a fixed pattern is displayed for a long time.

## RELIABILITY TEST ITEMS FOR TFT-LCD MODULE

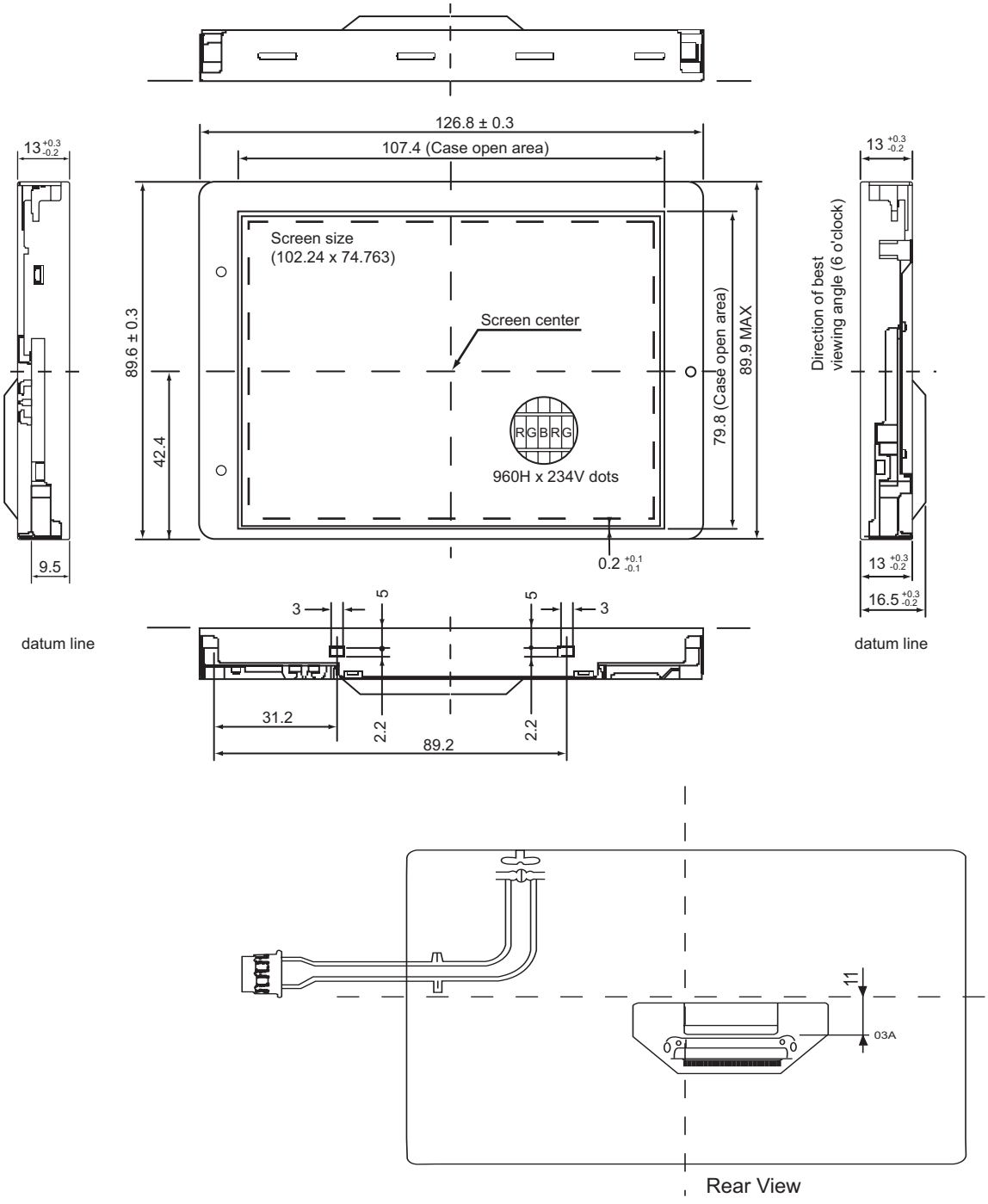
| No. | Test items | Test conditions | |
|---|---|---|---|
| 1 | High temperature storage test | $t_P$=-85°C | 240h |
| 2 | Low temperature storage test | $t_P$=-30°C | 240h |
| 3 | High temperature and high humidity operating test | $t_P$=-60°C, 90~95%RH | 240h |
| 4 | High temperature operating test | $t_P$=-85°C | 240h |
| 5 | Low temperature operating test | $t_P$=-30°C | 240h |
| 6 | Electrostatic discharge test | =200V • 200pF(OΩ) | Once for each terminal |
| 7 | Shock test | 980m/s$^2$ 6ms. | ±X, ±Y, ±Z 3 times for each direction |
| 8 | Vibration test | Frequency Range: 8~33.3Hz<br>Stroke: 1.3mm<br>Sweep: 33.3Hz~400Hz<br>Acceletation: 28.4m/s$^2$<br>Frequency: 15 minutes<br>2 hours for each direction of X, Z (1)<br>4 hours for direction of Y<br>(8 hours in total) | (JIS C0041. A-7 Condition C) |
| 9 | Heat shock test | -30°C~-85°C/200 cycles<br>(0.5h) (0.5h) | |

$t_P$=Panel temperature

Evaluation Result Criteria:
Note 1: Direction of X, Y, Z is defined as follows:



# OUTLINE DIMENSIONS



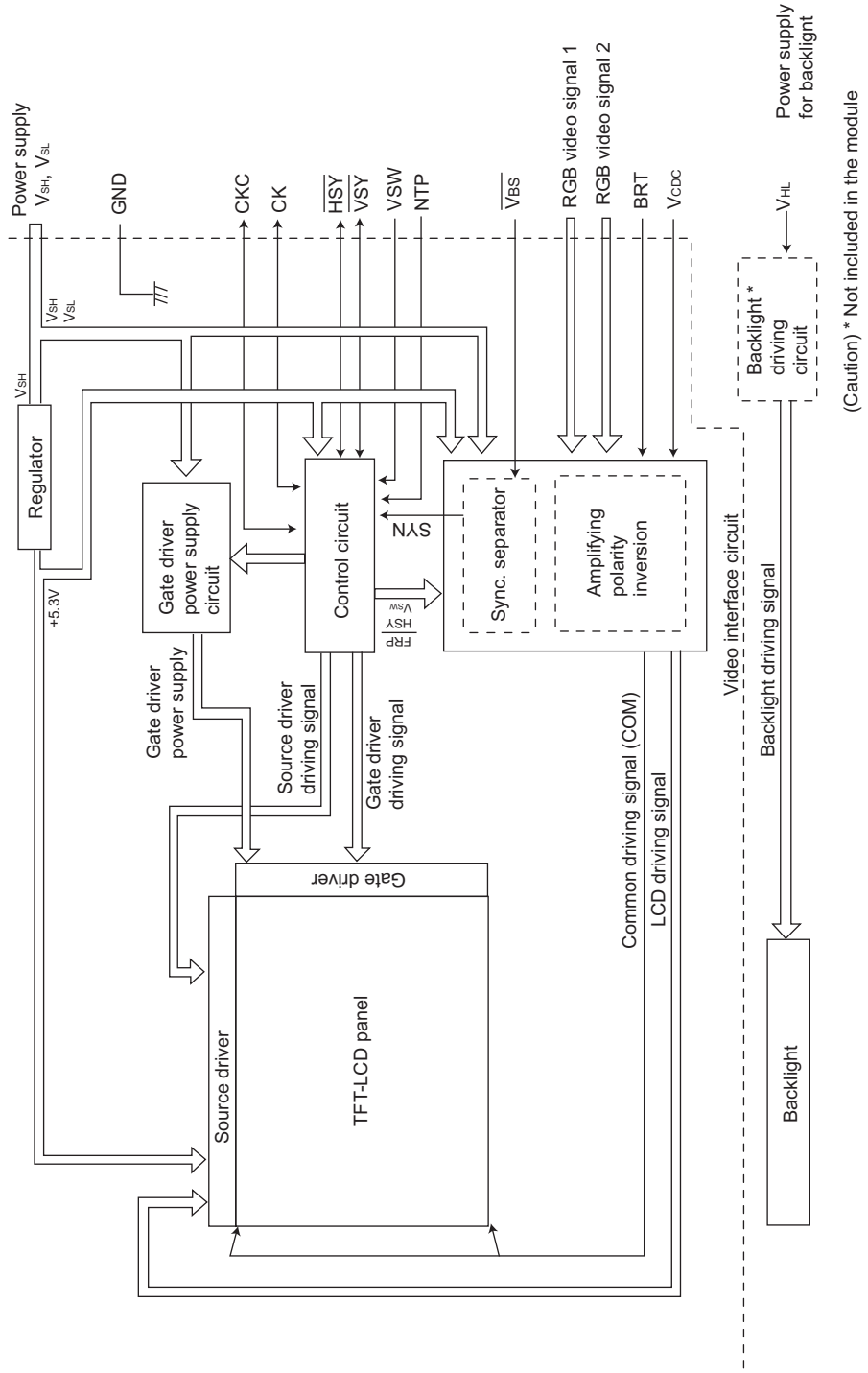



Fig. 4 Circuit block diagram of TFT-LCD module

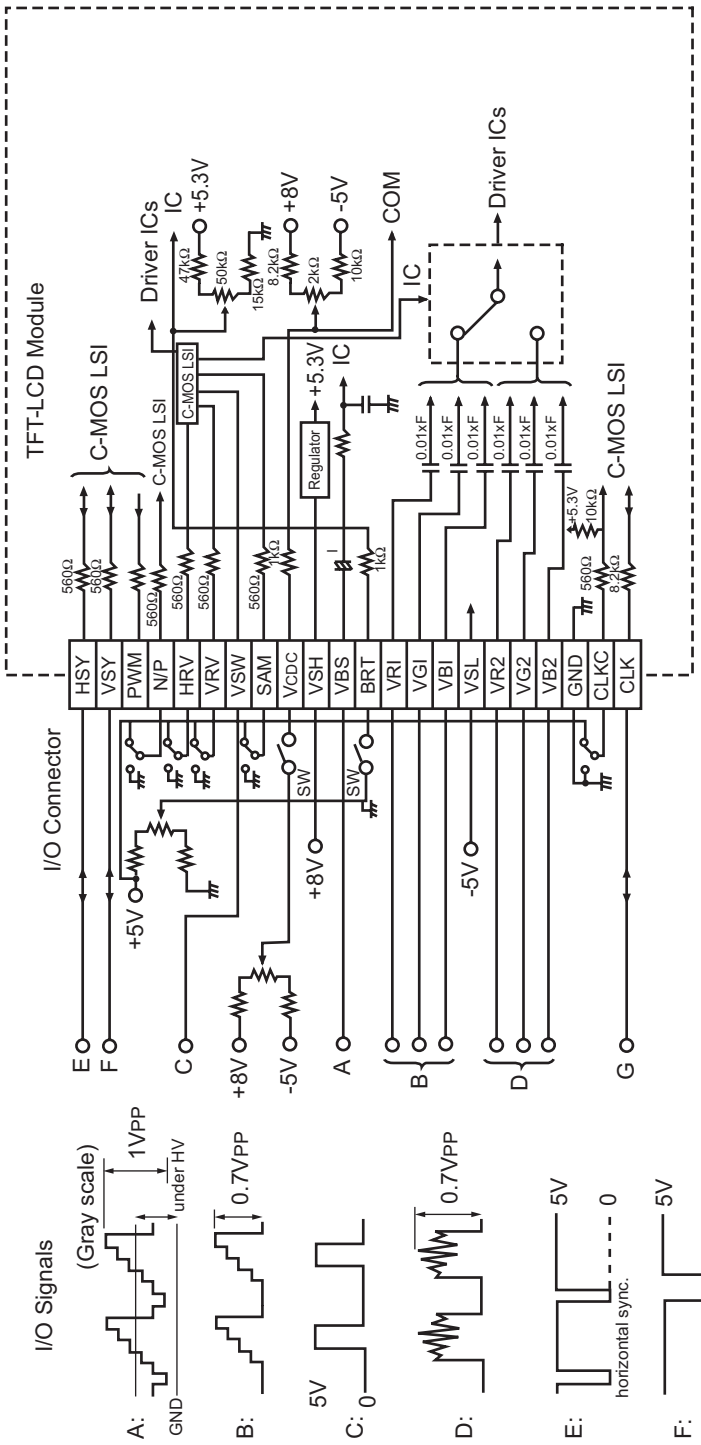



Fig. 5 Recommended Circuit

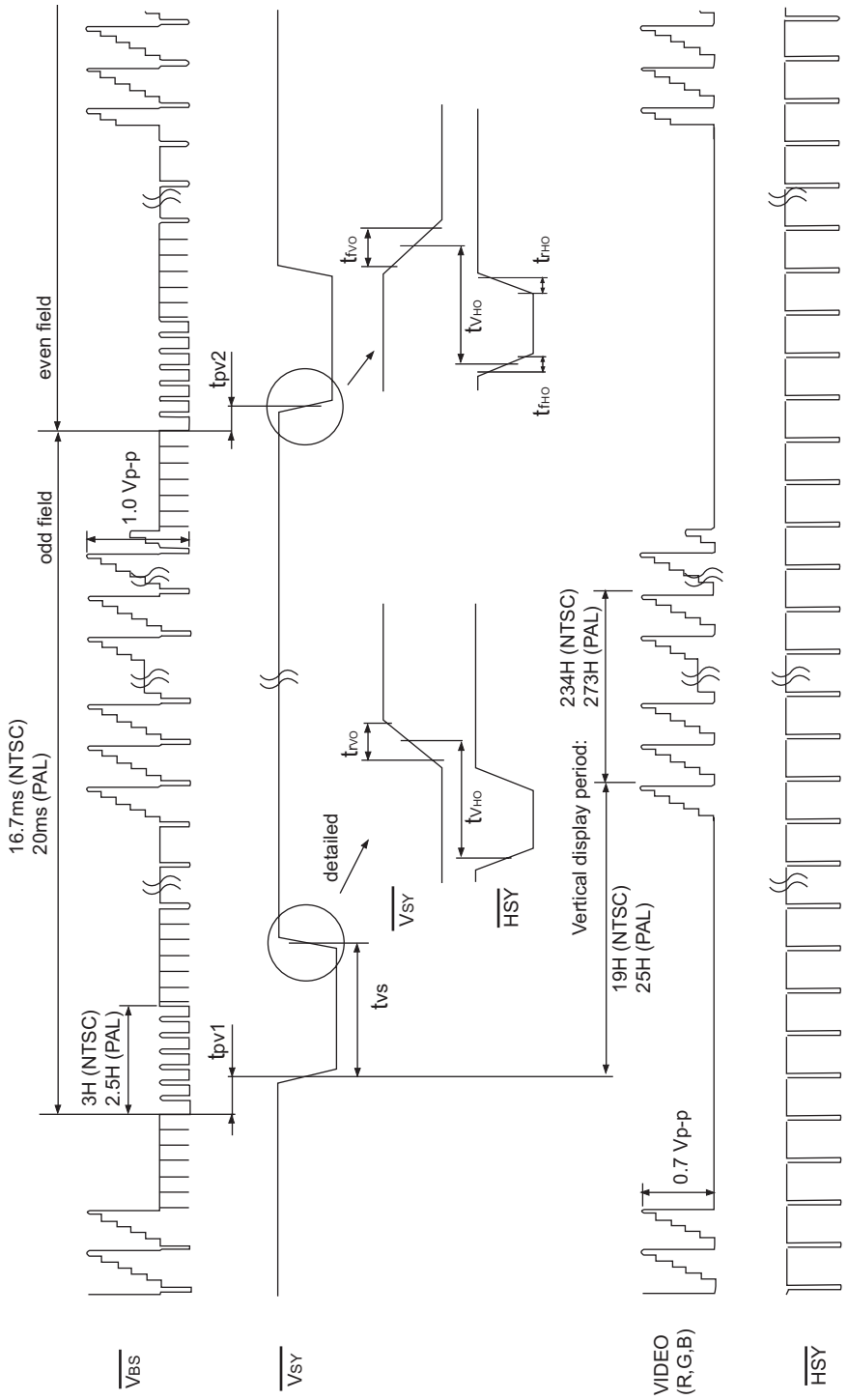



Fig. 6-A Input/Output signal waveforms (CKC= "High")

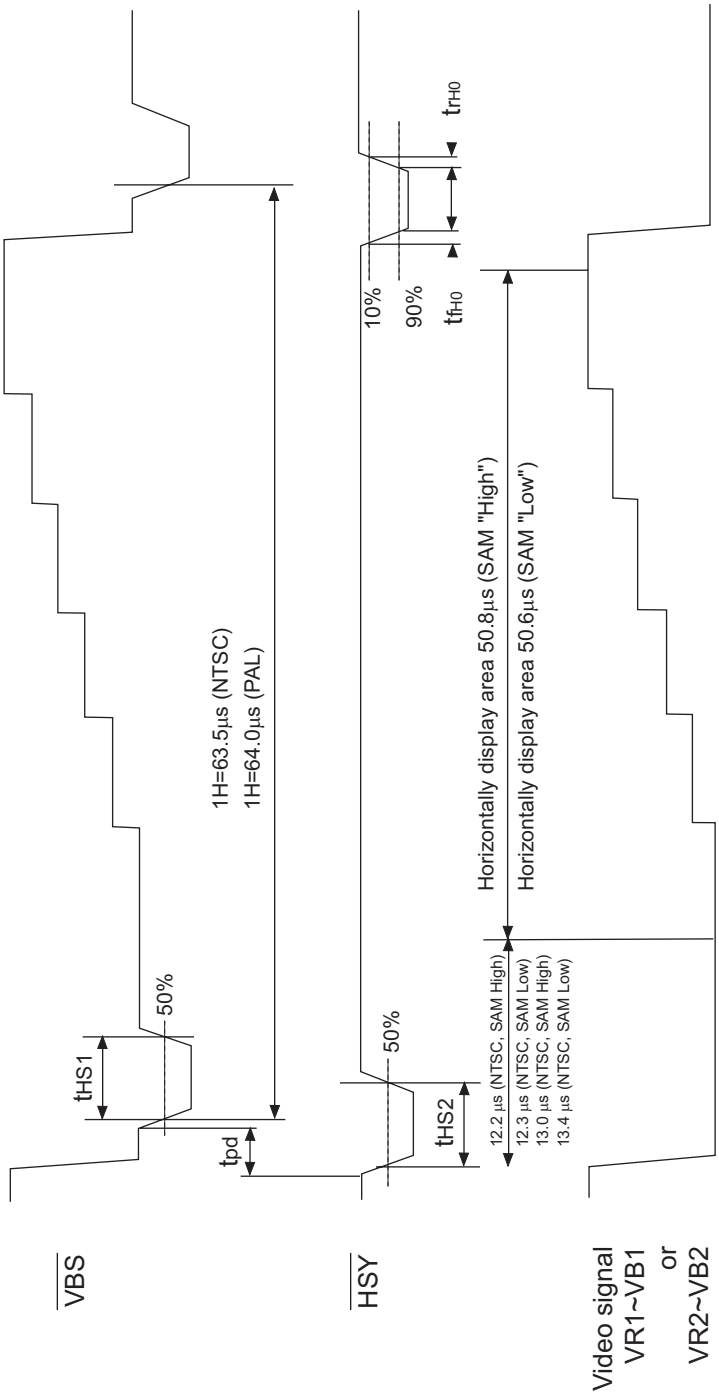



Fig. 6-B Input/Output signal waveforms (CKC="High")

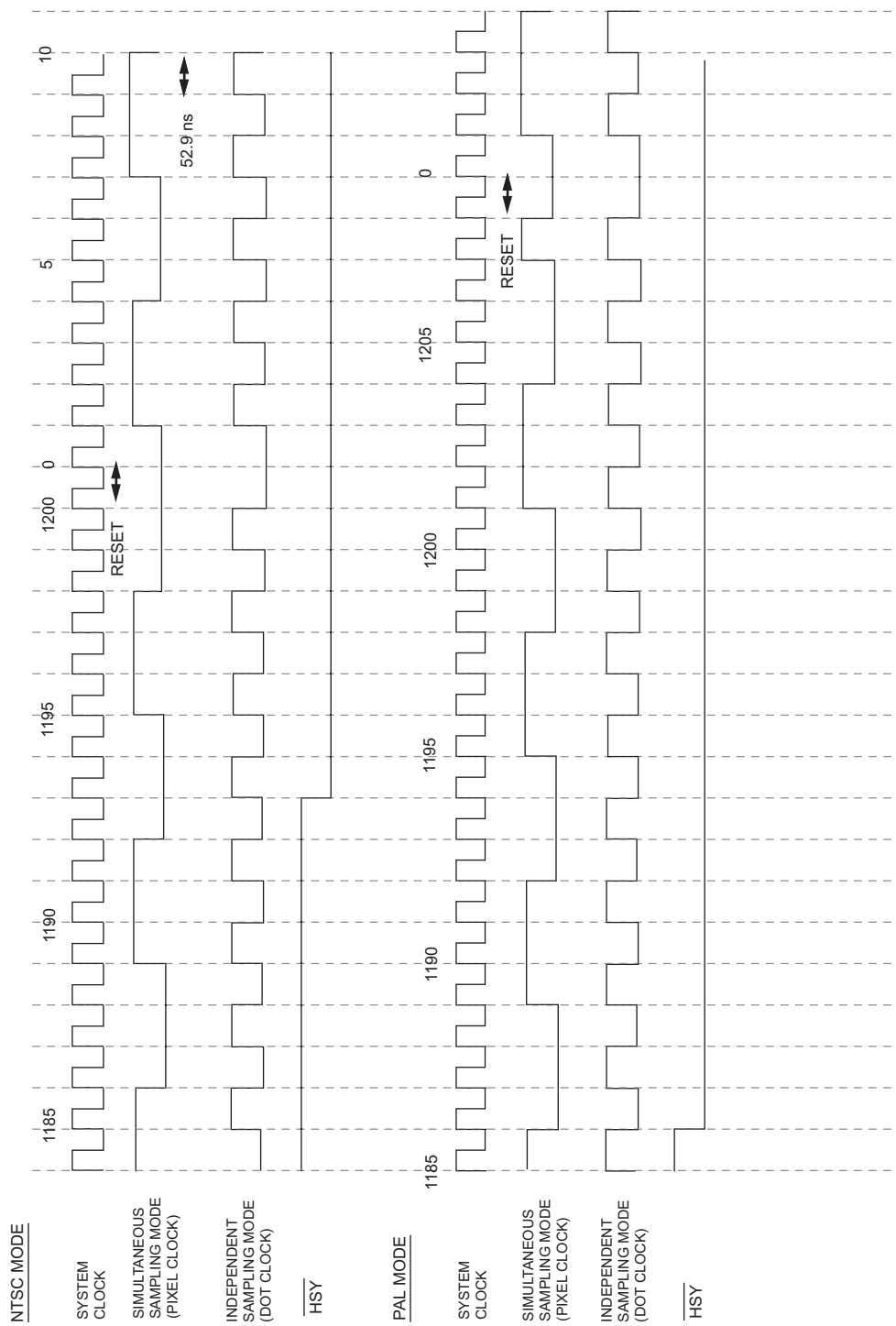



Fig. 6-C Input/Output signal waveforms (CLKC="High")

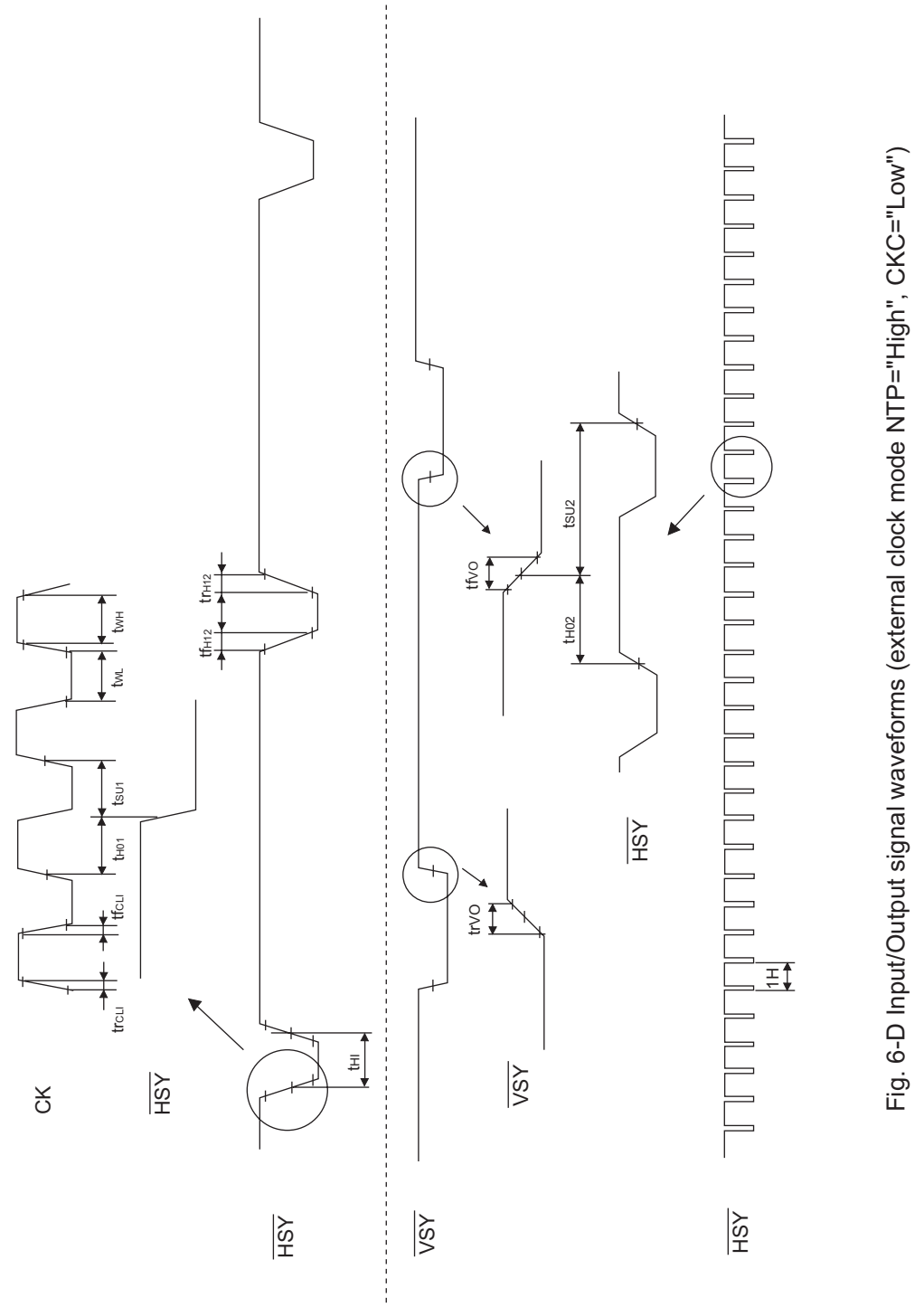



Fig. 6-D Input/Output signal waveforms (external clock mode NTP="High", CKC="Low")

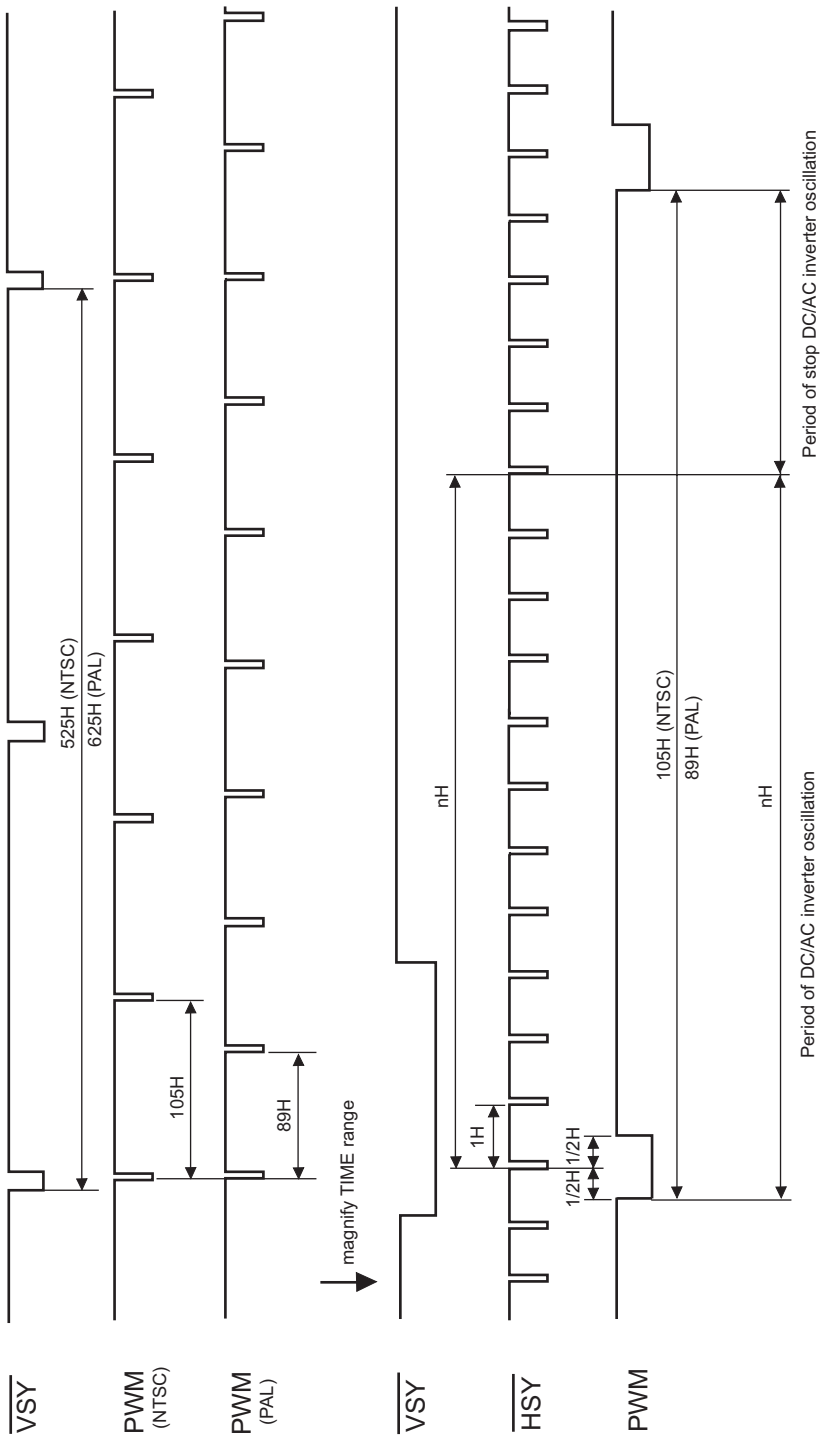
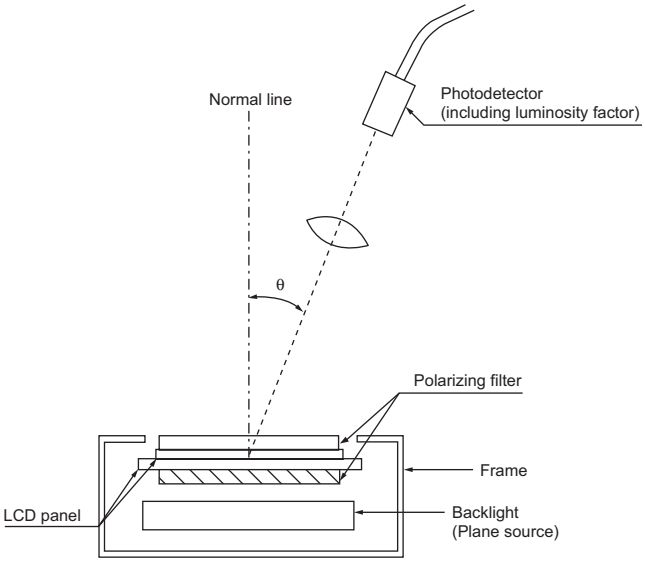



Fig. 7 PWM signal waveform for dimming backlight




Brightness: Less than 5000cd/m$^2$

Wave length: To be cut less than 400nm

Fig. 9 Optical characteristics

## ADJUSTING METHOD OF OPTIMUM COMMON ELECTRODE DC BIAS VOLTAGE

To obtain optimum DC bias voltage of common electrode driving signal (VCDC). Photo-electric devices are very effective, and the accuracy is within 0.1V. (In visual examination method, the accuracy is about 0.5V because of the difference amoung individuals.)

To gain optimum common electrode DC bias voltage, there is the following method which uses the photoelectric device.

(Measurement of flicker)

DC bias voltage is adjusted so as to minimize NTSC: 60Hz (30Hz) PAL: 50Hz (25Hz) flicker.

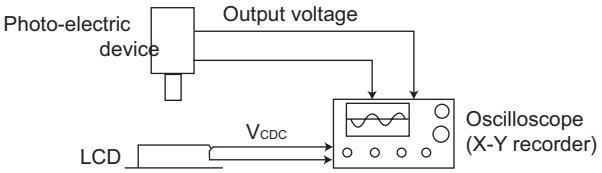
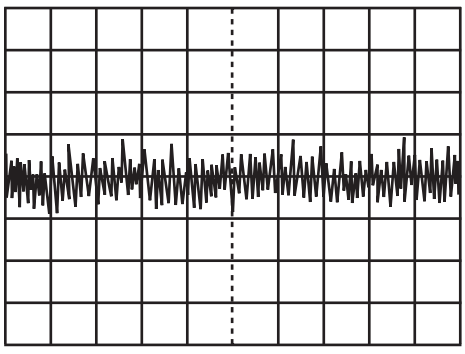


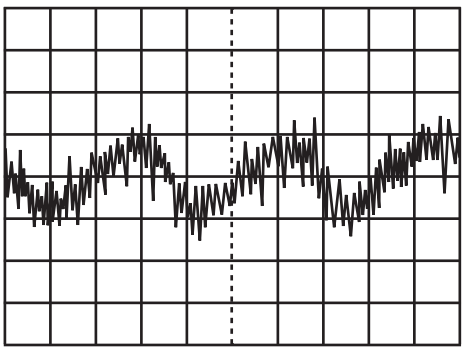

Fig. A Measurement system

Photo-electric output voltage is measured by an oscilloscope at a system shown in Fig. A.

DC bias voltage must be adjusted so as to minimize the NTSC:60Hz(30Hz) PAL:50Hz(25Hz) flicker with DC bias voltage changing slowly. (Fig. B)



DC bias: Optimum



DC bias: Optimum + 1V

Fig. B Waveforms of flicker